AMD Xilinx - XC3S400-5FTG256C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	896
Number of Logic Elements/Cells	8064
Total RAM Bits	294912
Number of I/O	173
Number of Gates	400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s400-5ftg256c

power, the configuration data is written to the FPGA using any of five different modes: Master Parallel, Slave Parallel, Master Serial, Slave Serial, and Boundary Scan (JTAG). The Master and Slave Parallel modes use an 8-bit-wide SelectMAP port.

The recommended memory for storing the configuration data is the low-cost Xilinx Platform Flash PROM family, which includes the XCF00S PROMs for serial configuration and the higher density XCF00P PROMs for parallel or serial configuration.

I/O Capabilities

The SelectIO feature of Spartan-3 devices supports eighteen single-ended standards and eight differential standards as listed in Table 2. Many standards support the DCI feature, which uses integrated terminations to eliminate unwanted signal reflections.

Table 2: **Signal Standards Supported by the Spartan-3 Family**

Standard Category	Description	V_{CCO} (V)	Class	Symbol (IOSTANDARD)	DCI Option
Single-Ended					
GTL	Gunning Transceiver Logic	N/A	Terminated	GTL	Yes
			Plus	GTLP	Yes
HSTL	High-Speed Transceiver Logic	1.5	I	HSTL_I	Yes
			III	HSTL_III	Yes
		1.8	I	HSTL_I_18	Yes
			II	HSTL_II_18	Yes
			III	HSTL_III_18	Yes
LVCMOS	Low-Voltage CMOS	1.2	N/A	LVCMOS12	No
		1.5	N/A	LVCMOS15	Yes
		1.8	N/A	LVCMOS18	Yes
		2.5	N/A	LVCMOS25	Yes
		3.3	N/A	LVCMOS33	Yes
LVTTL	Low-Voltage Transistor-Transistor Logic	3.3	N/A	LVTTL	No
PCI	Peripheral Component Interconnect	3.0	33 MHz(1)	PCI33_3	No
SSTL	Stub Series Terminated Logic	1.8	N/A (±6.7 mA)	SSTL18_I	Yes
			N/A (±13.4 mA)	SSTL18_II	No
		2.5	I	SSTL2_I	Yes
			II	SSTL2_II	Yes
Differential					
LDT (ULVDS)	Lightning Data Transport (HyperTransport™) Logic	2.5	N/A	LDT_25	No
LVDS	Low-Voltage Differential Signaling		Standard	LVDS_25	Yes
			Bus	BLVDS_25	No
			Extended Mode	LVDSEXT_25	Yes
LVPECL	Low-Voltage Positive Emitter-Coupled Logic	2.5	N/A	LVPECL_25	No
RSDS	Reduced-Swing Differential Signaling	2.5	N/A	RSDS_25	No
HSTL	Differential High-Speed Transceiver Logic	1.8	II	DIFF_HSTL_II_18	Yes
SSTL	Differential Stub Series Terminated Logic	2.5	II	DIFF_SSTL2_II	Yes

Notes:

1. 66 MHz PCI is not supported by the Xilinx IP core although PCI66_3 is an available I/O standard.

The DCI feature operates independently for each of the device's eight banks. Each bank has an 'N' reference pin (VRN) and a 'P' reference pin, (VRP), to calibrate driver and termination resistance. Only when using a DCI standard on a given bank do these two pins function as VRN and VRP. When not using a DCI standard, the two pins function as user I/Os. As shown in Figure 9, add an external reference resistor to pull the VRN pin up to V_{CCO} and another reference resistor to pull the VRP pin down to GND. Also see Figure 42, page 116. Both resistors have the same value—commonly 50Ω—with one-percent tolerance, which is either the characteristic impedance of the line or twice that, depending on the DCI standard in use. Standards having a symbol name that contains the letters "DV2" use a reference resistor value that is twice the line impedance. DCI adjusts the output driver impedance to match the reference resistors' value or half that, according to the standard. DCI always adjusts the on-chip termination resistors to directly match the reference resistors' value.

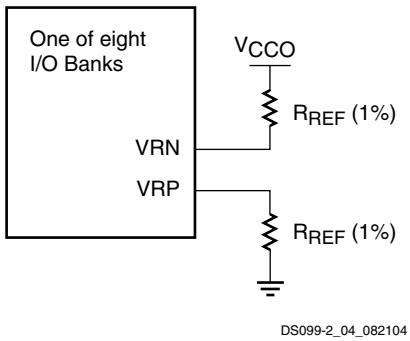

Figure 9: **Connection of Reference Resistors (R_{REF})**

The rules guiding the use of DCI standards on banks are as follows:

- No more than one DCI I/O standard with a Single Termination is allowed per bank.
- No more than one DCI I/O standard with a Split Termination is allowed per bank.
- Single Termination, Split Termination, Controlled- Impedance Driver, and Controlled-Impedance Driver with Half Impedance can co-exist in the same bank.

See also The Organization of IOBs into Banks, immediately below, and DCI: User I/O or Digitally Controlled Impedance Resistor Reference Input, page 115.

The Organization of IOBs into Banks

IOBs are allocated among eight banks, so that each side of the device has two banks, as shown in Figure 10. For all packages, each bank has independent V_{REF} lines. For example, V_{REF} Bank 3 lines are separate from the V_{REF} lines going to all other banks.

For the Very Thin Quad Flat Pack (VQ), Plastic Quad Flat Pack (PQ), Fine Pitch Thin Ball Grid Array (FT), and Fine Pitch Ball Grid Array (FG) packages, each bank has dedicated V_{CCO} lines. For example, the V_{CCO} Bank 7 lines are separate from the V_{CCO} lines going to all other banks. Thus, Spartan-3 devices in these packages support eight independent V_{CCO} supplies.

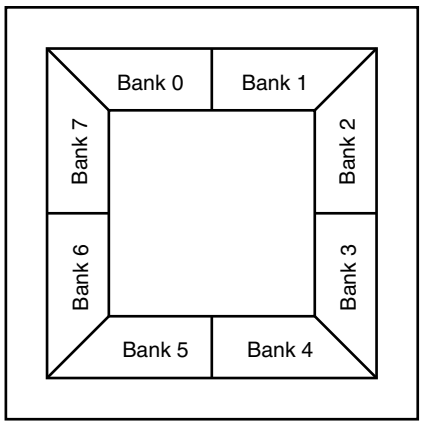

Figure 10: **Spartan-3 FPGA I/O Banks (Top View)**

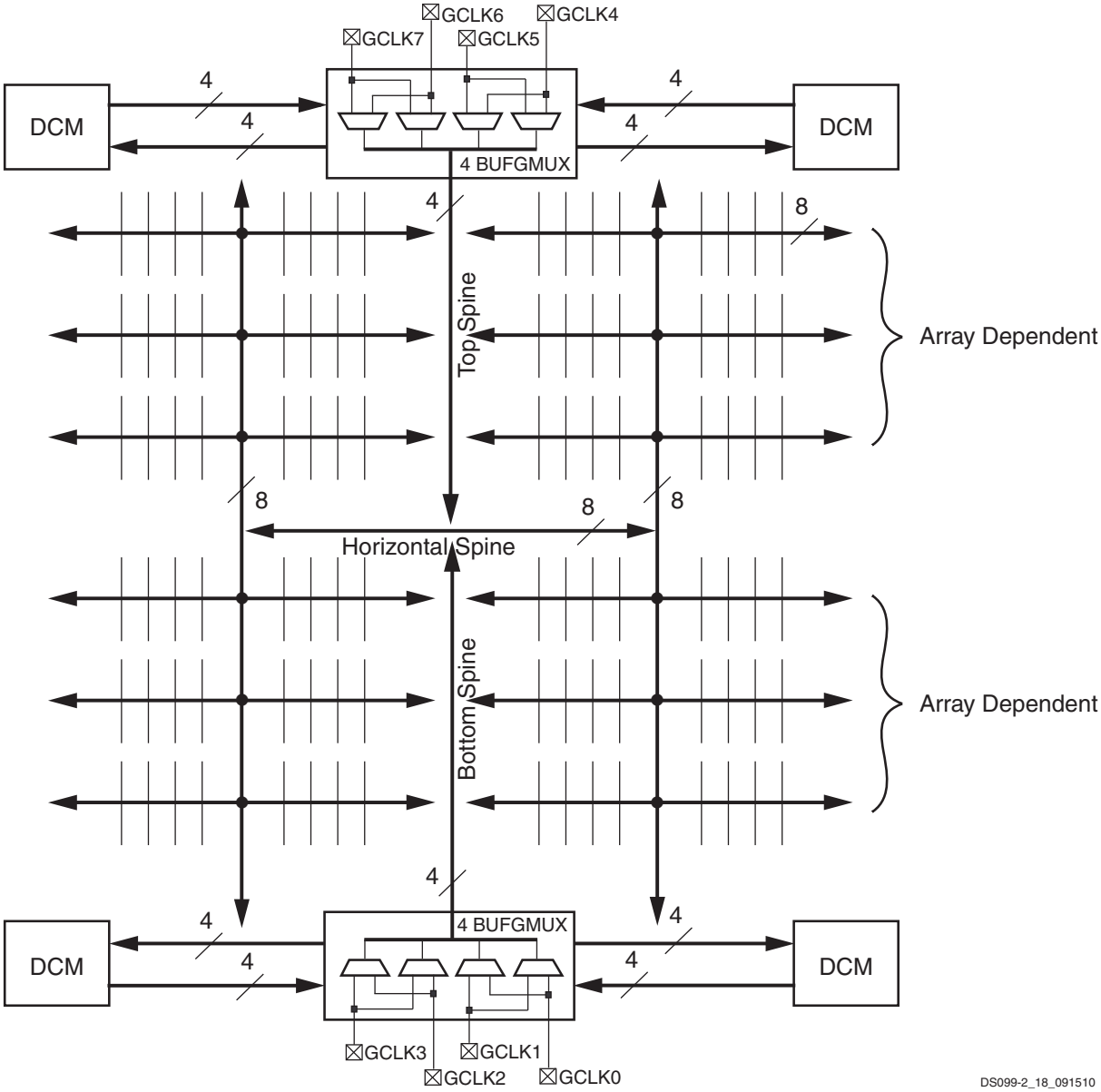

Figure 24: **Spartan-3 FPGAs Clock Network (Top View)**

The Standard Configuration Interface

Configuration signals belong to one of two different categories: Dedicated or Dual-Purpose. Which category determines which of the FPGA's power rails supplies the signal's driver and, thus, helps describe the electrical characteristics at the pin.

The Dedicated configuration pins include PROG_B, HSWAP_EN, TDI, TMS, TCK, TDO, CCLK, DONE, and M0-M2. These pins are powered by the V_{CCAUX} supply.

The Dual-Purpose configuration pins comprise INIT_B, DOUT, BUSY, RDWR_B, CS_B, and DIN/D0-D7. Each of these pins, according to its bank placement, uses the V_{CCO} lines for either Bank 4 (VCCO_4 on most packages, VCCO_BOTTOM on TQ144 and CP132 packages) or Bank 5 (VCCO_5). All the signals used in the serial configuration modes rely on VCCO_4 power. Signals used in the parallel configuration modes and Readback require from VCCO_5 as well as from VCCO_4.

Both the Dedicated signals described above and the Dual-Purpose signals constitute the configuration interface. The Dedicated pins, powered by the 2.5V V_{CCAUX} supply, always use the LVCMOS25 I/O standard. The Dual-Purpose signals, however, are powered by the VCCO_4 supply and also by the VCCO_5 supply in the Parallel configuration modes. The simplest configuration interface uses 2.5V for VCCO_4 and VCCO_5, if required. However, VCCO_4 and, if needed, VCCO_5 can be voltages other than 2.5V but then the configuration interface will have two voltage levels: 2.5V for V_{CCAUX} and a separate V_{CCO} supply. The Dual-Purpose signals default to the LVCMOS input and output levels for the associated V_{CCO} voltage supply.

3.3V-Tolerant Configuration Interface

A 3.3V-tolerant configuration interface simply requires adding a few external resistors as described in detail in XAPP453: *The 3.3V Configuration of Spartan-3 FPGAs*.

The 3.3V-tolerance is implemented as follows (a similar approach can be used for other supply voltage levels):

Apply 3.3V to VCCO_4 and, in some configuration modes, to VCCO_5 to power the Dual-Purpose configuration pins. This scales the output voltages and input thresholds associated with these pins so that they become 3.3V-compatible.

Apply 2.5V to V_{CCAUX} to power the Dedicated configuration pins. For 3.3V-tolerance, the Dedicated inputs require series resistors to limit the incoming current to 10 mA or less. The Dedicated outputs have reduced noise margin when the FPGA drives a High logic level into another device's 3.3V receiver. Choose a power regulator or supply that can tolerate reverse current on the V_{CCAUX} lines.

Configuration Modes

Spartan-3 FPGAs support the following five configuration modes:

- Slave Serial mode
- Master Serial mode
- Slave Parallel (SelectMAP) mode
- Master Parallel (SelectMAP) mode
- Boundary-Scan (JTAG) mode (IEEE 1532/IEEE 1149.1)

Slave Serial Mode

In Slave Serial mode, the FPGA receives configuration data in bit-serial form from a serial PROM or other serial source of configuration data. The FPGA on the far right of Figure 26 is set for the Slave Serial mode. The CCLK pin on the FPGA is an input in this mode. The serial bitstream must be set up at the DIN input pin a short time before each rising edge of the externally generated CCLK.

Multiple FPGAs can be daisy-chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed internally to the DOUT pin. The data on the DOUT pin changes on the falling edge of CCLK.

Initial Spartan-3 FPGA mask revisions have a limit on how fast the V_{CCO} supply can ramp. The minimum allowed V_{CCO} ramp rate appears as T_{CCO} in Table 30, page 60. The minimum rate is affected by the package inductance. Consequently, the ball grid array and chip-scale packages (CP132, FT256, FG456, FG676, and FG900) allow a faster ramp rate than the quad-flat packages (VQ100, TQ144, and PQ208).

Configuration Data Retention, Brown-Out

The FPGA's configuration data is stored in robust CMOS configuration latches. The data in these latches is retained even when the voltages drop to the minimum levels necessary to preserve RAM contents. This is specified in Table 31, page 60.

If, after configuration, the V_{CCAUX} or V_{CCINT} supply drops below its data retention voltage, clear the current device configuration using one of the following methods:

- Force the V_{CCAUX} or V_{CCINT} supply voltage below the minimum Power On Reset (POR) voltage threshold Table 29, page 59).
- Assert PROG_B Low.

The POR circuit does not monitor the VCCO_4 supply after configuration. Consequently, dropping the VCCO_4 voltage does not reset the device by triggering a Power-On Reset (POR) event.

No Internal Charge Pumps or Free-Running Oscillators

Some system applications are sensitive to sources of analog noise. Spartan-3 FPGA circuitry is fully static and does not employ internal charge pumps.

The CCLK configuration clock is active during the FPGA configuration process. After configuration completes, the CCLK oscillator is automatically disabled unless the Bitstream Generator (BitGen) option ***Persist=Yes***. See Module 4: Table 80, page 125.

Spartan-3 FPGAs optionally support a featured called Digitally Controlled Impedance (DCI). When used in an application, the DCI logic uses an internal oscillator. The DCI logic is only enabled if the FPGA application specifies an I/O standard that requires DCI (LVDCI_33, LVDCI_25, etc.). If DCI is not used, the associated internal oscillator is also disabled.

In summary, unless an application uses the ***Persist=Yes*** option or specifies a DCI I/O standard, an FPGA with no external switching remains fully static.

DC Electrical Characteristics

In this section, specifications may be designated as Advance, Preliminary, or Production. These terms are defined as follows:

- **Advance:** Initial estimates are based on simulation, early characterization, and/or extrapolation from the characteristics of other families. Values are subject to change. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur. Use as estimates, not for production.
- **Preliminary:** Based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reported delays is greatly reduced compared to Advance data. Use as estimates, not for production.
- **Production:** These specifications are approved only after silicon has been characterized over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Parameter values are considered stable with no future changes expected.

  Production-quality systems must only use FPGA designs compiled with a Production status speed file. FPGA designs using a less mature speed file designation should only be used during system prototyping or preproduction qualification. FPGA designs with speed files designated as Advance or Preliminary should not be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the latest Xilinx ISE® software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **The following applies unless otherwise noted: The parameter values published in this module apply to all Spartan®-3 devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.** All parameters representing voltages are measured with respect to GND.

Mask and Fab Revisions

Some specifications list different values for one or more mask or fab revisions, indicated by the device top marking (see Package Marking, page 5). The revision differences involve the power ramp rates, differential DC specifications, and DCM characteristics. The most recent revision (mask rev E and GQ fab/geometry code) is errata-free with improved specifications than earlier revisions.

Mask rev E with fab rev GQ has been shipping since 2005 (see XCN05009) and has been 100% of Xilinx Spartan-3 device shipments since 2006. SCD 0974 was provided to ensure the receipt of the rev E silicon, but it is no longer needed. Parts ordered under the SCD appended “0974” to the standard part number. For example, “XC3S50-4VQ100C” became “XC3S50-4VQ100C0974”.

Table 28: **Absolute Maximum Ratings**

Symbol	Description	Conditions		Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND			–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage relative to GND			–0.5	3.00	V
V_{CCO}	Output driver supply voltage relative to GND			–0.5	3.75	V
V_{REF}	Input reference voltage relative to GND			–0.5	V_{CCO} + 0.5	V
V_{IN}	Voltage applied to all User I/O pins and Dual-Purpose pins relative to GND(2,4)	Driver in a high-impedance state	Commercial	–0.95	4.4	V
			Industrial	–0.85	4.3	
	Voltage applied to all Dedicated pins relative to GND(3)		All temp. ranges	–0.5	V_{CCAUX} + 0.5	V

Table 36: **DC Characteristics of User I/Os Using Single-Ended Standards**

Signal Standard (IOSTANDARD) and Current Drive Attribute (mA)		Test Conditions		Logic Level Characteristics	
		I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
GTL		32	–	0.4	–
GTL_DCI		Note 3	Note 3		
GTLP		36	–	0.6	–
GTLP_DCI		Note 3	Note 3		
HSLVDCI_15		Note 3	Note 3	0.4	V_{CCO} – 0.4
HSLVDCI_18					
HSLVDCI_25					
HSLVDCI_33					
HSTL_I		8	–8	0.4	V_{CCO} – 0.4
HSTL_I_DCI		Note 3	Note 3		
HSTL_III		24	–8	0.4	V_{CCO} – 0.4
HSTL_III_DCI		Note 3	Note 3		
HSTL_I_18		8	–8	0.4	V_{CCO} – 0.4
HSTL_I_DCI_18		Note 3	Note 3		
HSTL_II_18		16	–16	0.4	V_{CCO} – 0.4
HSTL_II_DCI_18		Note 3	Note 3		
HSTL_III_18		24	–8	0.4	V_{CCO} – 0.4
HSTL_III_DCI_18		Note 3	Note 3		
LVCMOS12(4)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
LVCMOS15(4)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
LVDCI_15, LVDCI_DV2_15		Note 3	Note 3		
LVCMOS18(4)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
LVDCI_18, LVDCI_DV2_18		Note 3	Note 3		
LVCMOS25(4,5)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24	24	–24		
LVDCI_25, LVDCI_DV2_25		Note 3	Note 3		

Switching Characteristics

All Spartan-3 devices are available in two speed grades: –4 and the higher performance –5. Switching characteristics in this document may be designated as Advance, Preliminary, or Production. Each category is defined as follows:

Advance: These specifications are based on simulations only and are typically available soon after establishing FPGA specifications. Although speed grades with this designation are considered relatively stable and conservative, some under-reported delays may still occur.

Preliminary: These specifications are based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting preliminary delays is greatly reduced compared to Advance data.

Production: These specifications are approved once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Production-quality systems must use FPGA designs compiled using a Production status speed file. FPGAs designs using a less mature speed file designation may only be used during system prototyping or preproduction qualification. FPGA designs using Advance or Preliminary status speed files should never be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the Xilinx ISE software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

Xilinx ISE Software Updates: http://www.xilinx.com/support/download/index.htm

All specified limits are representative of worst-case supply voltage and junction temperature conditions. Unless otherwise noted, the following applies: Parameter values apply to all Spartan-3 devices. All parameters representing voltages are measured with respect to GND.

Selected timing parameters and their representative values are included below either because they are important as general design requirements or they indicate fundamental device performance characteristics. The Spartan-3 FPGA v1.38 speed files are the original source for many but not all of the values. The v1.38 speed files are available in Xilinx Integrated Software Environment (ISE) software version 8.2i.

The speed grade designations for these files are shown in Table 39. For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

Table 39: **Spartan-3 FPGA Speed Grade Designations (ISE v8.2i or Later)**

Device	Advance	Preliminary	Production
XC3S50			-4, -5 (v1.37 and later)
XC3S200			
XC3S400			
XC3S1000			
XC3S1500			
XC3S2000			
XC3S4000			
XC3S5000			-4, -5 (v1.38 and later)

Table 47: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS18	Slow	2 mA	5.49	6.31	ns
		4 mA	3.45	3.97	ns
		6 mA	2.84	3.26	ns
		8 mA	2.62	3.01	ns
		12 mA	2.11	2.43	ns
		16 mA	2.07	2.38	ns
	Fast	2 mA	2.50	2.88	ns
		4 mA	1.15	1.32	ns
		6 mA	0.96	1.10	ns
		8 mA	0.87	1.01	ns
		12 mA	0.79	0.91	ns
		16 mA	0.76	0.87	ns
LVDCI_18			0.81	0.94	ns
LVDCI_DV2_18			0.67	0.77	ns
LVCMOS25	Slow	2 mA	6.43	7.39	ns
		4 mA	4.15	4.77	ns
		6 mA	3.38	3.89	ns
		8 mA	2.99	3.44	ns
		12 mA	2.53	2.91	ns
		16 mA	2.50	2.87	ns
		24 mA	2.22	2.55	ns
	Fast	2 mA	3.27	3.76	ns
		4 mA	1.87	2.15	ns
		6 mA	0.32	0.37	ns
		8 mA	0.19	0.22	ns
		12 mA	0	0	ns
		16 mA	–0.02	–0.01	ns
		24 mA	–0.04	–0.02	ns
LVDCI_25			0.27	0.31	ns
LVDCI_DV2_25			0.16	0.19	ns

Table 70: **Spartan-3 FPGA Pin Definitions *(Cont'd)***

Pin Name	Direction	Description
TDI	Input	**JTAG Test Data Input:** TDI is the serial data input for all JTAG instruction and data registers. This pin has an internal pull-up resistor to VCCAUX during configuration.
TMS	Input	**JTAG Test Mode Select:** The serial TMS input controls the operation of the JTAG port. This pin has an internal pull-up resistor to VCCAUX during configuration.
TDO	Output	**JTAG Test Data Output:** TDO is the serial data output for all JTAG instruction and data registers. This pin has an internal pull-up resistor to VCCAUX during configuration.
VCCO: I/O bank output voltage supply pins		
VCCO_#	Supply	**Power Supply for Output Buffer Drivers (per bank):** These pins power the output drivers within a specific I/O bank.
VCCAUX: Auxiliary voltage supply pins		
VCCAUX	Supply	**Power Supply for Auxiliary Circuits:** +2.5V power pins for auxiliary circuits, including the Digital Clock Managers (DCMs), the dedicated configuration pins (CONFIG), and the dedicated JTAG pins. All VCCAUX pins must be connected.
VCCINT: Internal core voltage supply pins		
VCCINT	Supply	**Power Supply for Internal Core Logic:** +1.2V power pins for the internal logic. All pins must be connected.
GND: Ground supply pins		
GND	Supply	**Ground:** Ground pins, which are connected to the power supply's return path. All pins must be connected.
N.C.: Unconnected package pins		
N.C.		**Unconnected Package Pin:** These package pins are unconnected.

Notes:

1. All unused inputs and bidirectional pins must be tied either High or Low. For unused enable inputs, apply the level that disables the associated function. One common approach is to activate internal pull-up or pull-down resistors. An alternative approach is to externally connect the pin to either VCCO or GND.
2. All outputs are of the totem-pole type — i.e., they can drive High as well as Low logic levels — except for the cases where "Open Drain" is indicated. The latter can only drive a Low logic level and require a pull-up resistor to produce a High logic level.

Detailed, Functional Pin Descriptions

I/O Type: Unrestricted, General-purpose I/O Pins

After configuration, I/O-type pins are inputs, outputs, bidirectional I/O, three-state outputs, open-drain outputs, or open-source outputs, as defined in the application

Pins labeled "IO" support all SelectIO™ interface signal standards except differential standards. A given device at most only has a few of these pins.

A majority of the general-purpose I/O pins are labeled in the format "IO_Lxxy_#". These pins support all SelectIO signal standards, including the differential standards such as LVDS, ULVDS, BLVDS, RSDS, or LDT.

For additional information, see IOBs, page 10

Package Thermal Characteristics

The power dissipated by an FPGA application has implications on package selection and system design. The power consumed by a Spartan-3 FPGA is reported using either the XPower Estimator (XPE) or the XPower Analyzer integrated in the Xilinx ISE development software. Table 86 provides the thermal characteristics for the various Spartan-3 device/package offerings.

The junction-to-case thermal resistance (θ_{JC}) indicates the difference between the temperature measured on the package body (case) and the die junction temperature per watt of power consumption. The junction-to-board (θ_{JB}) value similarly reports the difference between the board and junction temperature. The junction-to-ambient (θ_{JA}) value reports the temperature difference per watt between the ambient environment and the junction temperature. The θ_{JA} value is reported at different air velocities, measured in linear feet per minute (LFM). The "Still Air (0 LFM)" column shows the θ_{JA} value in a system without a fan. The thermal resistance drops with increasing air flow.

Table 86: **Spartan-3 FPGA Package Thermal Characteristics**

Package	Device	Junction-to-Case (θ_{JC})	Junction-to-Board (θ_{JB})	Junction-to-Ambient (θ_{JA}) at Different Air Flows				Units
				Still Air (0 LFM)	250 LFM	500 LFM	750 LFM	
VQ(G)100	XC3S50	12.0	–	46.2	38.4	35.8	34.9	°C/Watt
	XC3S200	10.0	–	40.5	33.7	31.3	30.5	°C/Watt
CP(G)132(1)	XC3S50	14.5	32.8	53.0	46.4	44.0	42.5	°C/Watt
TQ(G)144	XC3S50	7.6	–	41.0	31.9	27.2	25.6	°C/Watt
	XC3S200	6.6	–	34.5	26.9	23.0	21.6	°C/Watt
	XC3S400	6.1	–	32.8	25.5	21.8	20.4	°C/Watt
PQ(G)208	XC3S50	10.6	–	37.4	27.6	24.4	22.6	°C/Watt
	XC3S200	8.6	–	36.2	26.7	23.6	21.9	°C/Watt
	XC3S400	7.5	–	35.4	26.1	23.1	21.4	°C/Watt
FT(G)256	XC3S200	9.9	22.9	31.7	25.6	24.5	24.2	°C/Watt
	XC3S400	7.9	19.0	28.4	22.8	21.5	21.0	°C/Watt
	XC3S1000	5.6	14.7	24.8	19.2	18.0	17.5	°C/Watt
FG(G)320	XC3S400	8.9	13.9	24.4	19.0	17.8	17.0	°C/Watt
	XC3S1000	7.8	11.8	22.3	17.0	15.8	15.0	°C/Watt
	XC3S1500	6.7	9.8	20.3	15.18	13.8	13.1	°C/Watt
FG(G)456	XC3S400	8.4	13.6	20.8	15.1	13.9	13.4	°C/Watt
	XC3S1000	6.4	10.6	19.3	13.4	12.3	11.7	°C/Watt
	XC3S1500	4.9	8.3	18.3	12.4	11.2	10.7	°C/Watt
	XC3S2000	3.7	6.5	17.7	11.7	10.5	10.0	°C/Watt
FG(G)676	XC3S1000	6.0	10.4	17.9	13.7	12.6	12.0	°C/Watt
	XC3S1500	4.9	8.8	16.8	12.4	11.3	10.7	°C/Watt
	XC3S2000	4.1	7.9	15.6	11.1	9.9	9.3	°C/Watt
	XC3S4000	3.6	7.0	15.0	10.5	9.3	8.7	°C/Watt
	XC3S5000	3.4	6.3	14.7	10.3	9.1	8.5	°C/Watt
FG(G)900	XC3S2000	3.7	7.0	14.3	10.3	9.3	8.8	°C/Watt
	XC3S4000	3.3	6.4	13.6	9.7	8.7	8.2	°C/Watt
	XC3S5000	2.9	5.9	13.1	9.2	8.1	7.6	°C/Watt

Table 96: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S200, XC3S400, XC3S1000 Pin Name	FT256 Pin Number	Type
4	IO_L28N_4	P11	I/O
4	IO_L28P_4	R11	I/O
4	IO_L29N_4	M10	I/O
4	IO_L29P_4	N10	I/O
4	IO_L30N_4/D2	P10	DUAL
4	IO_L30P_4/D3	R10	DUAL
4	IO_L31N_4/INIT_B	N9	DUAL
4	IO_L31P_4/DOUT/BUSY	P9	DUAL
4	IO_L32N_4/GCLK1	R9	GCLK
4	IO_L32P_4/GCLK0	T9	GCLK
4	VCCO_4	L9	VCCO
4	VCCO_4	L10	VCCO
4	VCCO_4	M9	VCCO
5	IO	N5	I/O
5	IO	P7	I/O
5	IO	T5	I/O
5	IO/VREF_5	T8	VREF
5	IO_L01N_5/RDWR_B	T3	DUAL
5	IO_L01P_5/CS_B	R3	DUAL
5	IO_L10N_5/VRP_5	T4	DCI
5	IO_L10P_5/VRN_5	R4	DCI
5	IO_L27N_5/VREF_5	R5	VREF
5	IO_L27P_5	P5	I/O
5	IO_L28N_5/D6	N6	DUAL
5	IO_L28P_5/D7	M6	DUAL
5	IO_L29N_5	R6	I/O
5	IO_L29P_5/VREF_5	P6	VREF
5	IO_L30N_5	N7	I/O
5	IO_L30P_5	M7	I/O
5	IO_L31N_5/D4	T7	DUAL
5	IO_L31P_5/D5	R7	DUAL
5	IO_L32N_5/GCLK3	P8	GCLK
5	IO_L32P_5/GCLK2	N8	GCLK
5	VCCO_5	L7	VCCO
5	VCCO_5	L8	VCCO
5	VCCO_5	M8	VCCO
6	IO	K1	I/O
6	IO_L01N_6/VRP_6	R1	DCI
6	IO_L01P_6/VRN_6	P1	DCI
6	IO_L16N_6	P2	I/O

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
1	N.C. (◆)	IO_L18P_1	IO_L18P_1	IO_L18P_1	IO[3]	C18	I/O
1	IO_L19N_1	IO_L19N_1	IO_L19N_1	IO_L19N_1	IO_L19N_1	F17	I/O
1	IO_L19P_1	IO_L19P_1	IO_L19P_1	IO_L19P_1	IO_L19P_1	G17	I/O
1	IO_L22N_1	IO_L22N_1	IO_L22N_1	IO_L22N_1	IO_L22N_1	D17	I/O
1	IO_L22P_1	IO_L22P_1	IO_L22P_1	IO_L22P_1	IO_L22P_1	E17	I/O
1	N.C. (◆)	IO_L23N_1	IO_L23N_1	IO_L23N_1	IO_L23N_1	A17	I/O
1	N.C. (◆)	IO_L23P_1	IO_L23P_1	IO_L23P_1	IO_L23P_1	B17	I/O
1	IO_L24N_1	IO_L24N_1	IO_L24N_1	IO_L24N_1	IO_L24N_1	G16	I/O
1	IO_L24P_1	IO_L24P_1	IO_L24P_1	IO_L24P_1	IO_L24P_1	H16	I/O
1	IO_L25N_1	IO_L25N_1	IO_L25N_1	IO_L25N_1	IO_L25N_1	E16	I/O
1	IO_L25P_1	IO_L25P_1	IO_L25P_1	IO_L25P_1	IO_L25P_1	F16	I/O
1	N.C. (◆)	IO_L26N_1	IO_L26N_1	IO_L26N_1	IO_L26N_1	A16	I/O
1	N.C. (◆)	IO_L26P_1	IO_L26P_1	IO_L26P_1	IO_L26P_1	B16	I/O
1	IO_L27N_1	IO_L27N_1	IO_L27N_1	IO_L27N_1	IO_L27N_1	G15	I/O
1	IO_L27P_1	IO_L27P_1	IO_L27P_1	IO_L27P_1	IO_L27P_1	H15	I/O
1	IO_L28N_1	IO_L28N_1	IO_L28N_1	IO_L28N_1	IO_L28N_1	E15	I/O
1	IO_L28P_1	IO_L28P_1	IO_L28P_1	IO_L28P_1	IO_L28P_1	F15	I/O
1	IO_L29N_1	IO_L29N_1	IO_L29N_1	IO_L29N_1	IO_L29N_1	A15	I/O
1	IO_L29P_1	IO_L29P_1	IO_L29P_1	IO_L29P_1	IO_L29P_1	B15	I/O
1	IO_L30N_1	IO_L30N_1	IO_L30N_1	IO_L30N_1	IO_L30N_1	G14	I/O
1	IO_L30P_1	IO_L30P_1	IO_L30P_1	IO_L30P_1	IO_L30P_1	H14	I/O
1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	D14	VREF
1	IO_L31P_1	IO_L31P_1	IO_L31P_1	IO_L31P_1	IO_L31P_1	E14	I/O
1	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	B14	GCLK
1	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	C14	GCLK
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	C16	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	C20	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	H17	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	H18	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	J14	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	J15	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	J16	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	K14	VCCO
2	N.C. (◆)	N.C. (■)	IO	IO	IO	F22	I/O
2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	C25	DCI
2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	C26	DCI
2	IO_L02N_2	IO_L02N_2	IO_L02N_2	IO_L02N_2	IO_L02N_2	E23	I/O
2	IO_L02P_2	IO_L02P_2	IO_L02P_2	IO_L02P_2	IO_L02P_2	E24	I/O
2	IO_L03N_2/VREF_2	IO_L03N_2/VREF_2[1]	IO_L03N_2/VREF_2	IO_L03N_2/VREF_2	IO_L03N_2/VREF_2	D25	VREF[1]
2	IO_L03P_2	IO_L03P_2	IO_L03P_2	IO_L03P_2	IO_L03P_2	D26	I/O
2	N.C. (◆)	IO_L05N_2	IO_L05N_2	IO_L05N_2	IO_L05N_2	E25	I/O
2	N.C. (◆)	IO_L05P_2	IO_L05P_2	IO_L05P_2	IO_L05P_2	E26	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
0	IO_L10N_0	IO_L10N_0	J9	I/O
0	IO_L10P_0	IO_L10P_0	H9	I/O
0	IO_L11N_0	IO_L11N_0	G10	I/O
0	IO_L11P_0	IO_L11P_0	F10	I/O
0	IO_L12N_0	IO_L12N_0	C10	I/O
0	IO_L12P_0	IO_L12P_0	B10	I/O
0	IO_L13N_0	IO_L13N_0	J10	I/O
0	IO_L13P_0	IO_L13P_0	K11	I/O
0	IO_L14N_0	IO_L14N_0	H11	I/O
0	IO_L14P_0	IO_L14P_0	G11	I/O
0	IO_L15N_0	IO_L15N_0	F11	I/O
0	IO_L15P_0	IO_L15P_0	E11	I/O
0	IO_L16N_0	IO_L16N_0	D11	I/O
0	IO_L16P_0	IO_L16P_0	C11	I/O
0	IO_L17N_0	IO_L17N_0	B11	I/O
0	IO_L17P_0	IO_L17P_0	A11	I/O
0	IO_L18N_0	IO_L18N_0	K12	I/O
0	IO_L18P_0	IO_L18P_0	J12	I/O
0	IO_L19N_0	IO_L19N_0	H12	I/O
0	IO_L19P_0	IO_L19P_0	G12	I/O
0	IO_L20N_0	IO_L20N_0	F12	I/O
0	IO_L20P_0	IO_L20P_0	E12	I/O
0	IO_L21N_0	IO_L21N_0	D12	I/O
0	IO_L21P_0	IO_L21P_0	C12	I/O
0	IO_L22N_0	IO_L22N_0	B12	I/O
0	IO_L22P_0	IO_L22P_0	A12	I/O
0	IO_L23N_0	IO_L23N_0	J13	I/O
0	IO_L23P_0	IO_L23P_0	H13	I/O
0	IO_L24N_0	IO_L24N_0	F13	I/O
0	IO_L24P_0	IO_L24P_0	E13	I/O
0	IO_L25N_0	IO_L25N_0	B13	I/O
0	IO_L25P_0	IO_L25P_0	A13	I/O
0	IO_L26N_0	IO_L26N_0	K14	I/O
0	IO_L26P_0/VREF_0	IO_L26P_0/VREF_0	J14	VREF
0	IO_L27N_0	IO_L27N_0	G14	I/O
0	IO_L27P_0	IO_L27P_0	F14	I/O
0	IO_L28N_0	IO_L28N_0	C14	I/O
0	IO_L28P_0	IO_L28P_0	B14	I/O
0	IO_L29N_0	IO_L29N_0	J15	I/O
0	IO_L29P_0	IO_L29P_0	H15	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
1	IO_L25P_1	IO_L25P_1	D19	I/O
1	IO_L26N_1	IO_L26N_1	A19	I/O
1	IO_L26P_1	IO_L26P_1	B19	I/O
1	IO_L27N_1	IO_L27N_1	F17	I/O
1	IO_L27P_1	IO_L27P_1	G17	I/O
1	IO_L28N_1	IO_L28N_1	B17	I/O
1	IO_L28P_1	IO_L28P_1	C17	I/O
1	IO_L29N_1	IO_L29N_1	J16	I/O
1	IO_L29P_1	IO_L29P_1	K16	I/O
1	IO_L30N_1	IO_L30N_1	G16	I/O
1	IO_L30P_1	IO_L30P_1	H16	I/O
1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	D16	VREF
1	IO_L31P_1	IO_L31P_1	E16	I/O
1	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	B16	GCLK
1	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	C16	GCLK
1	N.C. (◆)	IO_L37N_1	H18	I/O
1	N.C. (◆)	IO_L37P_1	J18	I/O
1	N.C. (◆)	IO_L38N_1	D18	I/O
1	N.C. (◆)	IO_L38P_1	E18	I/O
1	N.C. (◆)	IO_L39N_1	A18	I/O
1	N.C. (◆)	IO_L39P_1	B18	I/O
1	N.C. (◆)	IO_L40N_1	K17	I/O
1	N.C. (◆)	IO_L40P_1	K18	I/O
1	VCCO_1	VCCO_1	L17	VCCO
1	VCCO_1	VCCO_1	C18	VCCO
1	VCCO_1	VCCO_1	G18	VCCO
1	VCCO_1	VCCO_1	L18	VCCO
1	VCCO_1	VCCO_1	L19	VCCO
1	VCCO_1	VCCO_1	J20	VCCO
1	VCCO_1	VCCO_1	C22	VCCO
1	VCCO_1	VCCO_1	G22	VCCO
1	VCCO_1	VCCO_1	E24	VCCO
1	VCCO_1	VCCO_1	C26	VCCO
2	IO	IO	J25	I/O
2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	C29	DCI
2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	C30	DCI
2	IO_L02N_2	IO_L02N_2	D27	I/O
2	IO_L02P_2	IO_L02P_2	D28	I/O
2	IO_L03N_2/VREF_2	IO_L03N_2/VREF_2	D29	VREF
2	IO_L03P_2	IO_L03P_2	D30	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
2	IO_L28N_2	IO_L28N_2	M26	I/O
2	IO_L28P_2	IO_L28P_2	N25	I/O
2	IO_L29N_2	IO_L29N_2	N26	I/O
2	IO_L29P_2	IO_L29P_2	N27	I/O
2	IO_L31N_2	IO_L31N_2	N29	I/O
2	IO_L31P_2	IO_L31P_2	N30	I/O
2	IO_L32N_2	IO_L32N_2	P21	I/O
2	IO_L32P_2	IO_L32P_2	P22	I/O
2	IO_L33N_2	IO_L33N_2	P24	I/O
2	IO_L33P_2	IO_L33P_2	P25	I/O
2	IO_L34N_2/VREF_2	IO_L34N_2/VREF_2	P28	VREF
2	IO_L34P_2	IO_L34P_2	P29	I/O
2	IO_L35N_2	IO_L35N_2	R21	I/O
2	IO_L35P_2	IO_L35P_2	R22	I/O
2	IO_L37N_2	IO_L37N_2	R23	I/O
2	IO_L37P_2	IO_L37P_2	R24	I/O
2	IO_L38N_2	IO_L38N_2	R25	I/O
2	IO_L38P_2	IO_L38P_2	R26	I/O
2	IO_L39N_2	IO_L39N_2	R27	I/O
2	IO_L39P_2	IO_L39P_2	R28	I/O
2	IO_L40N_2	IO_L40N_2	R29	I/O
2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	R30	VREF
2	N.C. (◆)	IO_L41N_2	E27	I/O
2	N.C. (◆)	IO_L41P_2	F26	I/O
2	N.C. (◆)	IO_L45N_2	K28	I/O
2	N.C. (◆)	IO_L45P_2	K29	I/O
2	N.C. (◆)	IO_L46N_2	K21	I/O
2	N.C. (◆)	IO_L46P_2	L21	I/O
2	N.C. (◆)	IO_L47N_2	L23	I/O
2	N.C. (◆)	IO_L47P_2	L24	I/O
2	N.C. (◆)	IO_L50N_2	M29	I/O
2	N.C. (◆)	IO_L50P_2	M30	I/O
2	VCCO_2	VCCO_2	M20	VCCO
2	VCCO_2	VCCO_2	N20	VCCO
2	VCCO_2	VCCO_2	P20	VCCO
2	VCCO_2	VCCO_2	L22	VCCO
2	VCCO_2	VCCO_2	J24	VCCO
2	VCCO_2	VCCO_2	N24	VCCO
2	VCCO_2	VCCO_2	G26	VCCO
2	VCCO_2	VCCO_2	E28	VCCO

FG1156: 1156-lead Fine-pitch Ball Grid Array

Note: The FG(G)1156 package is discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

The 1,156-lead fine-pitch ball grid array package, FG1156, supports two different Spartan-3 devices, namely the XC3S4000 and the XC3S5000. The XC3S4000, however, has fewer I/O pins, which consequently results in 73 unconnected pins on the FG1156 package, labeled as "N.C." In Table 110 and Figure 53, these unconnected pins are indicated with a black diamond symbol (◆).

The XC3S5000 has a single unconnected package pin, ball AK31, which is also unconnected for the XC3S4000.

All the package pins appear in Table 110 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

On ball L29 in I/O Bank 2, the unconnected pin on the XC3S4000 maps to a VREF-type pin on the XC3S5000. If the other VREF_2 pins all connect to a voltage reference to support a special I/O standard, then also connect the N.C. pin on the XC3S4000 to the same VREF_2 voltage.

Pinout Table

Table 110: **FG1156 Package Pinout**

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
0	IO	IO	B9	I/O
0	IO	IO	E17	I/O
0	IO	IO	F6	I/O
0	IO	IO	F8	I/O
0	IO	IO	G12	I/O
0	IO	IO	H8	I/O
0	IO	IO	H9	I/O
0	IO	IO	J11	I/O
0	N.C. (◆)	IO	J9	I/O
0	N.C. (◆)	IO	K11	I/O
0	IO	IO	K13	I/O
0	IO	IO	K16	I/O
0	IO	IO	K17	I/O
0	IO	IO	L13	I/O
0	IO	IO	L16	I/O
0	IO	IO	L17	I/O
0	IO/VREF_0	IO/VREF_0	D5	VREF
0	IO/VREF_0	IO/VREF_0	E10	VREF
0	IO/VREF_0	IO/VREF_0	J14	VREF
0	IO/VREF_0	IO/VREF_0	L15	VREF
0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	B3	DCI
0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	A3	DCI
0	IO_L02N_0	IO_L02N_0	B4	I/O
0	IO_L02P_0	IO_L02P_0	A4	I/O
0	IO_L03N_0	IO_L03N_0	C5	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
N/A	GND	GND	AA18	GND
N/A	GND	GND	AA19	GND
N/A	GND	GND	AA20	GND
N/A	GND	GND	AA21	GND
N/A	GND	GND	AB1	GND
N/A	GND	GND	AB17	GND
N/A	GND	GND	AB18	GND
N/A	GND	GND	AB26	GND
N/A	GND	GND	AB30	GND
N/A	GND	GND	AB34	GND
N/A	GND	GND	AB5	GND
N/A	GND	GND	AB9	GND
N/A	GND	GND	AD3	GND
N/A	GND	GND	AD32	GND
N/A	GND	GND	AE10	GND
N/A	GND	GND	AE25	GND
N/A	GND	GND	AF1	GND
N/A	GND	GND	AF13	GND
N/A	GND	GND	AF16	GND
N/A	GND	GND	AF19	GND
N/A	GND	GND	AF22	GND
N/A	GND	GND	AF30	GND
N/A	GND	GND	AF34	GND
N/A	GND	GND	AF5	GND
N/A	GND	GND	AH28	GND
N/A	GND	GND	AH7	GND
N/A	GND	GND	AK1	GND
N/A	GND	GND	AK13	GND
N/A	GND	GND	AK16	GND
N/A	GND	GND	AK19	GND
N/A	GND	GND	AK22	GND
N/A	GND	GND	AK26	GND
N/A	GND	GND	AK30	GND
N/A	GND	GND	AK34	GND
N/A	GND	GND	AK5	GND
N/A	GND	GND	AK9	GND
N/A	GND	GND	AM11	GND
N/A	GND	GND	AM24	GND
N/A	GND	GND	AM3	GND
N/A	GND	GND	AM32	GND

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
N/A	GND	GND	Y14	GND
N/A	GND	GND	Y15	GND
N/A	GND	GND	Y16	GND
N/A	GND	GND	Y17	GND
N/A	GND	GND	Y18	GND
N/A	GND	GND	Y19	GND
N/A	GND	GND	Y20	GND
N/A	GND	GND	Y21	GND
N/A	N.C. (◆)	N.C. (■)	AK31	N.C.
N/A	VCCAUX	VCCAUX	AD30	VCCAUX
N/A	VCCAUX	VCCAUX	AD5	VCCAUX
N/A	VCCAUX	VCCAUX	AG16	VCCAUX
N/A	VCCAUX	VCCAUX	AG19	VCCAUX
N/A	VCCAUX	VCCAUX	AJ30	VCCAUX
N/A	VCCAUX	VCCAUX	AJ5	VCCAUX
N/A	VCCAUX	VCCAUX	AK11	VCCAUX
N/A	VCCAUX	VCCAUX	AK15	VCCAUX
N/A	VCCAUX	VCCAUX	AK20	VCCAUX
N/A	VCCAUX	VCCAUX	AK24	VCCAUX
N/A	VCCAUX	VCCAUX	AK29	VCCAUX
N/A	VCCAUX	VCCAUX	AK6	VCCAUX
N/A	VCCAUX	VCCAUX	E11	VCCAUX
N/A	VCCAUX	VCCAUX	E15	VCCAUX
N/A	VCCAUX	VCCAUX	E20	VCCAUX
N/A	VCCAUX	VCCAUX	E24	VCCAUX
N/A	VCCAUX	VCCAUX	E29	VCCAUX
N/A	VCCAUX	VCCAUX	E6	VCCAUX
N/A	VCCAUX	VCCAUX	F30	VCCAUX
N/A	VCCAUX	VCCAUX	F5	VCCAUX
N/A	VCCAUX	VCCAUX	H16	VCCAUX
N/A	VCCAUX	VCCAUX	H19	VCCAUX
N/A	VCCAUX	VCCAUX	L30	VCCAUX
N/A	VCCAUX	VCCAUX	L5	VCCAUX
N/A	VCCAUX	VCCAUX	R30	VCCAUX
N/A	VCCAUX	VCCAUX	R5	VCCAUX
N/A	VCCAUX	VCCAUX	T27	VCCAUX
N/A	VCCAUX	VCCAUX	T8	VCCAUX
N/A	VCCAUX	VCCAUX	W27	VCCAUX
N/A	VCCAUX	VCCAUX	W8	VCCAUX
N/A	VCCAUX	VCCAUX	Y30	VCCAUX

Date	Version	Description
11/30/07	2.3	Added XC3S5000 FG(G)676 package. Noted that the FG(G)1156 package is being discontinued. Updated Table 86 with latest thermal characteristics data.
06/25/08	2.4	Updated formatting and links.
12/04/09	2.5	Added link to UG332 in CCLK: Configuration Clock. Noted that the CP132, CPG132, FG1156, and FGG1156 packages are being discontinued in Table 81, Table 83, Table 84, Table 85, and Table 86. Updated CP132: 132-Ball Chip-Scale Package to indicate that the CP132 and CPG132 packages are being discontinued.
10/29/12	3.0	Added Notice of Disclaimer. Per XCN07022, updated the FG1156 and FGG1156 package discussion throughout document including in Table 81, Table 83, Table 84, Table 85, and Table 86. Per XCN08011, updated CP132 and CPG132 package discussion throughout document including in Table 81, Table 83, Table 84, Table 85, and Table 86. This product is not recommended for new designs.

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