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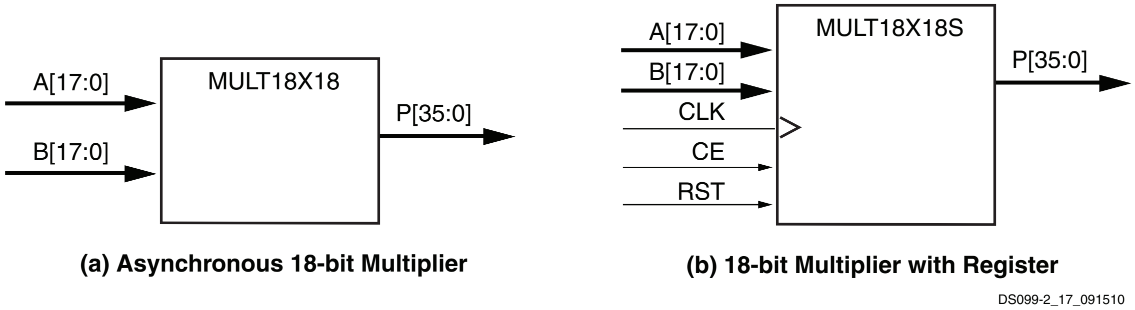
## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 896 |
| Number of Logic Elements/Cells | 8064 |
| Total RAM Bits | 294912 |
| Number of I/O | 141 |
| Number of Gates | 400000 |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 208-BFQFP |
| Supplier Device Package | 208-PQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc3s400-5pq208c |



**(a) Asynchronous 18-bit Multiplier**

**(b) 18-bit Multiplier with Register**

*Figure 18:* **Embedded Multiplier Primitives**

*Table 15:* **Embedded Multiplier Primitives Descriptions**

| Signal Name | Direction | Function |
|---|---|---|
| A[17:0] | Input | Apply one 18-bit multiplicand to these inputs. The MULT18X18S primitive requires a setup time before the enabled rising edge of CLK. |
| B[17:0] | Input | Apply the other 18-bit multiplicand to these inputs. The MULT18X18S primitive requires a setup time before the enabled rising edge of CLK. |
| P[35:0] | Output | The output on the P bus is a 36-bit product of the multiplicands A and B. In the case of the MULT18X18S primitive, an enabled rising CLK edge updates the P bus. |
| CLK | Input(1) | CLK is only an input to the MULT18X18S primitive. The clock signal applied to this input, when enabled by CE, updates the output register that drives the P bus. |
| CE | Input(1) | CE is only an input to the MULT18X18S primitive. Enable for the CLK signal. Asserting this input enables the CLK signal to update the P bus. |
| RST | Input(1) | RST is only an input to the MULT18X18S primitive. Asserting this input resets the output register on an enabled, rising CLK edge, forcing the P bus to all zeroes. |

**Notes:**

1. The control signals CLK, CE and RST have the option of inverted polarity.

## Digital Clock Manager (DCM)

Spartan-3 devices provide flexible, complete control over clock frequency, phase shift and skew through the use of the DCM feature. To accomplish this, the DCM employs a Delay-Locked Loop (DLL), a fully digital control system that uses feedback to maintain clock signal characteristics with a high degree of precision despite normal variations in operating temperature and voltage. This section provides a fundamental description of the DCM. For further information, refer to the chapter entitled “Using Digital Clock Managers” in UG331.

Each member of the Spartan-3 family has four DCMs, except the smallest, the XC3S50, which has two DCMs. The DCMs are located at the ends of the outermost Block RAM column(s). See Figure 1, page 3. The Digital Clock Manager is placed in a design as the “DCM” primitive.

The DCM supports three major functions:

- **Clock-skew Elimination:** Clock skew describes the extent to which clock signals may, under normal circumstances, deviate from zero-phase alignment. It occurs when slight differences in path delays cause the clock signal to arrive at different points on the die at different times. This clock skew can increase set-up and hold time requirements as well as clock-to-out time, which may be undesirable in applications operating at a high frequency, when timing is critical. The DCM eliminates clock skew by aligning the output clock signal it generates with another version of the clock signal that is fed back. As a result, the two clock signals establish a zero-phase relationship. This effectively cancels out clock distribution delays that may lie in the signal path leading from the clock output of the DCM to its feedback input.
- **Frequency Synthesis:** Provided with an input clock signal, the DCM can generate a wide range of different output clock frequencies. This is accomplished by either multiplying and/or dividing the frequency of the input clock signal by any of several different factors.

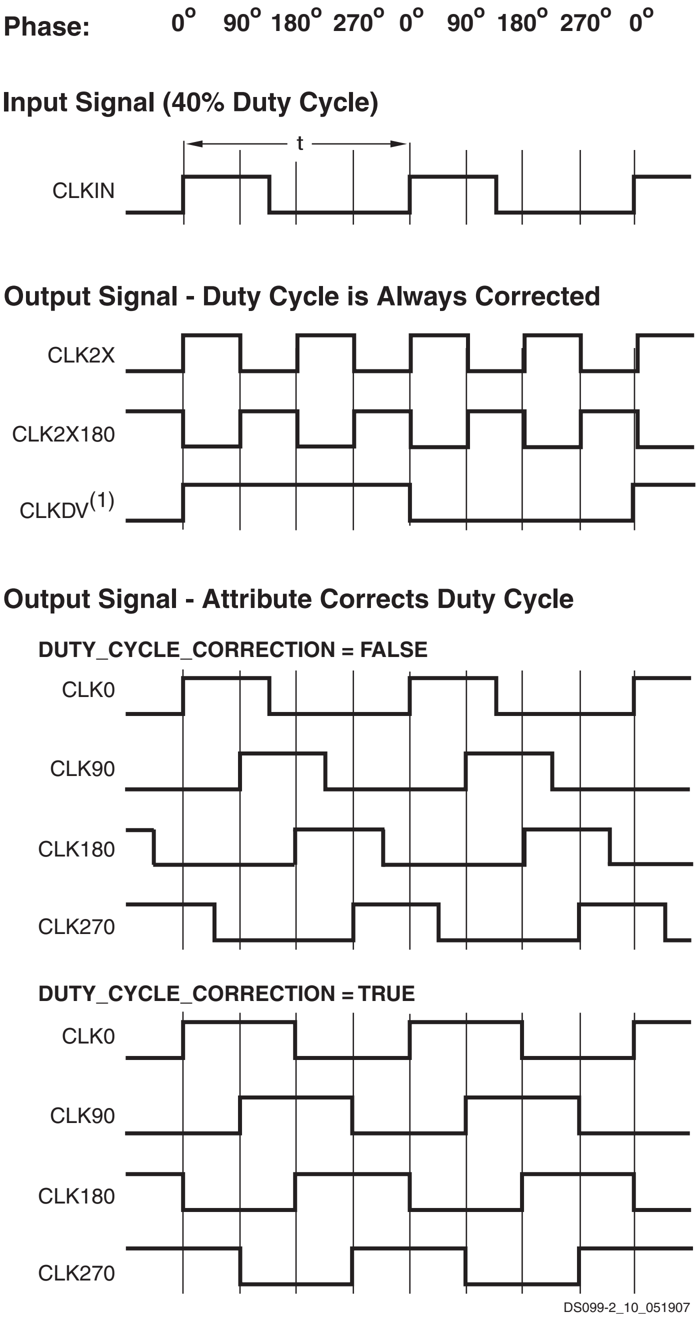


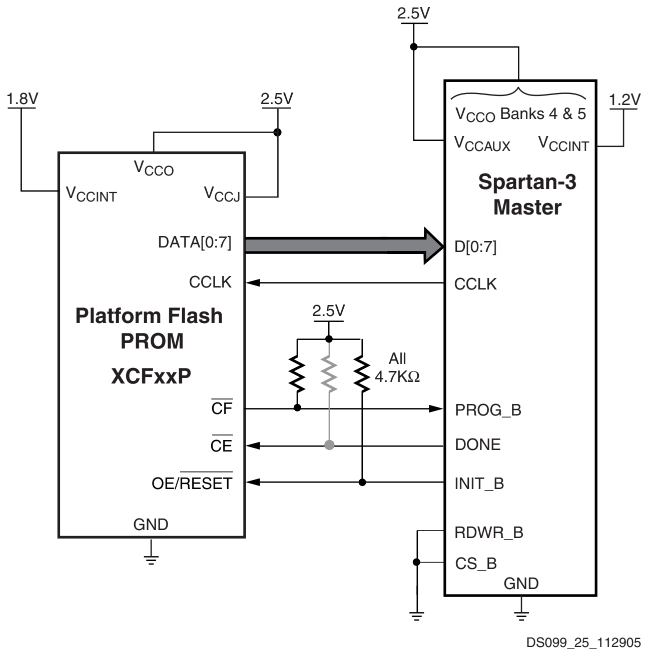
*Figure 22:* **Characteristics of the DLL Clock Outputs**

## Digital Frequency Synthesizer (DFS)

The DFS component generates clock signals the frequency of which is a product of the clock frequency at the CLKIN input and a ratio of two user-determined integers. Because of the wide range of possible output frequencies such a ratio permits, the DFS feature provides still further flexibility than the DLL's basic synthesis options as described in the preceding section. The DFS component's two dedicated outputs, CLKFX and CLKFX180, are defined in Table 19.

The signal at the CLKFX180 output is essentially an inversion of the CLKFX signal. These two outputs always exhibit a 50% duty cycle. This is true even when the CLKIN signal does not. These DFS clock outputs are driven at the same time as the DLL's seven clock outputs.

The numerator of the ratio is the integer value assigned to the attribute CLKFX_MULTIPLY and the denominator is the integer value assigned to the attribute CLKFX_DIVIDE. These attributes are described in Table 18.



**Notes:**

1. There are two ways to use the DONE line. First, one may set the BitGen option DriveDone to "Yes" only for the last FPGA to be configured in the chain shown above (or for the single FPGA as may be the case). This enables the DONE pin to drive High; thus, no pull-up resistor is necessary. DriveDone is set to "No" for the remaining FPGAs in the chain. Second, DriveDone can be set to "No" for all FPGAs. Then all DONE lines are open-drain and require the pull-up resistor shown in grey. In most cases, a value between 3.3KΩ to 4.7KΩ is sufficient. However, when using DONE synchronously with a long chain of FPGAs, cumulative capacitance may necessitate lower resistor values (e.g. down to 330Ω) in order to ensure a rise time within one clock cycle.

*Figure 28:* **Connection Diagram for Master Parallel Configuration**

## Master Parallel Mode

In this mode, the FPGA configures from byte-wide data, and the FPGA supplies the CCLK configuration clock. In Master configuration modes, CCLK behaves as a bidirectional I/O pin. Timing is similar to the Slave Parallel mode except that CCLK is supplied by the FPGA. The device connections are shown in Figure 28.

## Boundary-Scan (JTAG) Mode

In Boundary-Scan mode, dedicated pins are used for configuring the FPGA. The configuration is done entirely through the IEEE 1149.1 Test Access Port (TAP). FPGA configuration using the Boundary-Scan mode is compatible with the IEEE Std 1149.1-1993 standard and IEEE Std 1532 for In-System Configurable (ISC) devices.

Configuration through the boundary-scan port is always available, regardless of the selected configuration mode. In some cases, however, the mode pin setting may affect proper programming of the device due to various interactions. For example, if the mode pins are set to Master Serial or Master Parallel mode, and the associated PROM is already programmed with a valid configuration image, then there is potential for configuration interference between the JTAG and PROM data. Selecting the Boundary-Scan mode disables the other modes and is the most reliable mode when programming via JTAG.

## Configuration Sequence

The configuration of Spartan-3 devices is a three-stage process that occurs after Power-On Reset or the assertion of PROG_B. POR occurs after the $V_{CCINT}$, $V_{CCAUX}$, and $V_{CCO}$ Bank 4 supplies have reached their respective maximum input threshold levels (see Table 29, page 59). After POR, the three-stage process begins.

First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process. A flow diagram for the configuration sequence of the Serial and Parallel modes is shown in Figure 29. The flow diagram for the Boundary-Scan configuration sequence appears in Figure 30.

*Table 44:* **Input Timing Adjustments for IOB *(Cont'd)***

| Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD) | Add the Adjustment Below | | Units |
|---|---|---|---|
| | Speed Grade | | |
| | -5 | -4 | |
| LVCMOS15 | 0.42 | 0.49 | ns |
| LVDCI_15 | 0.38 | 0.43 | ns |
| LVDCI_DV2_15 | 0.38 | 0.44 | ns |
| LVCMOS18 | 0.24 | 0.28 | ns |
| LVDCI_18 | 0.29 | 0.33 | ns |
| LVDCI_DV2_18 | 0.28 | 0.33 | ns |
| LVCMOS25 | 0 | 0 | ns |
| LVDCI_25 | 0.05 | 0.05 | ns |
| LVDCI_DV2_25 | 0.04 | 0.04 | ns |
| LVCMOS33, LVDCI_33, LVDCI_DV2_33 | –0.05 | –0.02 | ns |
| LVTTL | 0.18 | 0.21 | ns |
| PCI33_3 | 0.20 | 0.22 | ns |
| SSTL18_I, SSTL18_I_DCI | 0.39 | 0.45 | ns |
| SSTL18_II | 0.39 | 0.45 | ns |
| SSTL2_I, SSTL2_I_DCI | 0.40 | 0.46 | ns |
| SSTL2_II, SSTL2_II_DCI | 0.36 | 0.41 | ns |
| **Differential Standards** | | | |
| LDT_25 (ULVDS_25) | 0.76 | 0.88 | ns |
| LVDS_25, LVDS_25_DCI | 0.65 | 0.75 | ns |
| BLVDS_25 | 0.34 | 0.39 | ns |
| LVDSEXT_25, LVDSEXT_25_DCI | 0.80 | 0.92 | ns |
| LVPECL_25 | 0.18 | 0.21 | ns |
| RSDS_25 | 0.43 | 0.50 | ns |
| DIFF_HSTL_II_18, DIFF_HSTL_II_18_DCI | 0.34 | 0.39 | ns |
| DIFF_SSTL2_II, DIFF_SSTL2_II_DCI | 0.65 | 0.75 | ns |

**Notes:**

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32, Table 35, and Table 37.
2. These adjustments are used to convert input path times originally specified for the LVCMOS25 standard to times that correspond to other signal standards.

*Table 47:* **Output Timing Adjustments for IOB *(Cont'd)***

| Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD) | | | Add the Adjustment Below | | Units |
|---|---|---|---|---|---|
| | | | Speed Grade | | |
| | | | -5 | -4 | |
| LVCMOS18 | Slow | 2 mA | 5.49 | 6.31 | ns |
| | | 4 mA | 3.45 | 3.97 | ns |
| | | 6 mA | 2.84 | 3.26 | ns |
| | | 8 mA | 2.62 | 3.01 | ns |
| | | 12 mA | 2.11 | 2.43 | ns |
| | | 16 mA | 2.07 | 2.38 | ns |
| | Fast | 2 mA | 2.50 | 2.88 | ns |
| | | 4 mA | 1.15 | 1.32 | ns |
| | | 6 mA | 0.96 | 1.10 | ns |
| | | 8 mA | 0.87 | 1.01 | ns |
| | | 12 mA | 0.79 | 0.91 | ns |
| | | 16 mA | 0.76 | 0.87 | ns |
| LVDCI_18 | | | 0.81 | 0.94 | ns |
| LVDCI_DV2_18 | | | 0.67 | 0.77 | ns |
| LVCMOS25 | Slow | 2 mA | 6.43 | 7.39 | ns |
| | | 4 mA | 4.15 | 4.77 | ns |
| | | 6 mA | 3.38 | 3.89 | ns |
| | | 8 mA | 2.99 | 3.44 | ns |
| | | 12 mA | 2.53 | 2.91 | ns |
| | | 16 mA | 2.50 | 2.87 | ns |
| | | 24 mA | 2.22 | 2.55 | ns |
| | Fast | 2 mA | 3.27 | 3.76 | ns |
| | | 4 mA | 1.87 | 2.15 | ns |
| | | 6 mA | 0.32 | 0.37 | ns |
| | | 8 mA | 0.19 | 0.22 | ns |
| | | 12 mA | 0 | 0 | ns |
| | | 16 mA | –0.02 | –0.01 | ns |
| | | 24 mA | –0.04 | –0.02 | ns |
| LVDCI_25 | | | 0.27 | 0.31 | ns |
| LVDCI_DV2_25 | | | 0.16 | 0.19 | ns |

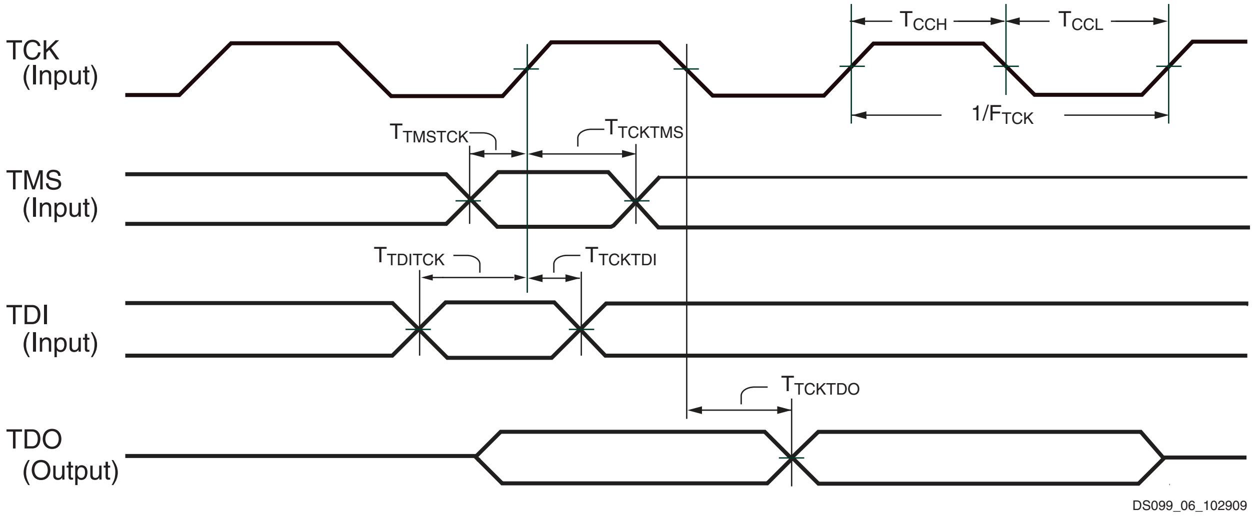


*Figure 39:* **JTAG Waveforms**

*Table 68:* **Timing for the JTAG Test Access Port**

| **Symbol** | **Description** | | **All Speed Grades** | | **Units** |
|---|---|---|---|---|---|
| | | | **Min** | **Max** | |
| **Clock-to-Output Times** | | | | | |
| $T_{TCKTDO}$ | The time from the falling transition on the TCK pin to data appearing at the TDO pin | | 1.0 | 11.0 | ns |
| **Setup Times** | | | | | |
| $T_{TDITCK}$ | The time from the setup of data at the TDI pin to the rising transition at the TCK pin | | 7.0 | – | ns |
| $T_{TMSTCK}$ | The time from the setup of a logic level at the TMS pin to the rising transition at the TCK pin | | 7.0 | – | ns |
| **Hold Times** | | | | | |
| $T_{TCKTDI}$ | The time from the rising transition at the TCK pin to the point when data is last held at the TDI pin | | 0 | – | ns |
| $T_{TCKTMS}$ | The time from the rising transition at the TCK pin to the point when a logic level is last held at the TMS pin | | 0 | – | ns |
| **Clock Timing** | | | | | |
| $T_{TCKH}$ | TCK pin High pulse width | | 5 | ∞ | ns |
| $T_{TCKL}$ | TCK pin Low pulse width | | 5 | ∞ | ns |
| $F_{TCK}$ | Frequency of the TCK signal | JTAG Configuration | 0 | 33 | MHz |
| | | Boundary-Scan | 0 | 25 | MHz |

**Notes:**

1. The numbers in this table are based on the operating conditions set forth in Table 32.

*Table 69:* **Types of Pins on Spartan-3 FPGAs *(Cont'd)***

| Pin Type/ Color Code | Description | Pin Name |
|---|---|---|
| VREF | Dual-purpose pin that is either a user-I/O pin or, along with all other VREF pins in the same bank, provides a reference voltage input for certain I/O standards. If used for a reference voltage within a bank, all VREF pins within the bank must be connected. | IO/VREF_#<br>IO_Lxxy_#/VREF_# |
| GND | Dedicated ground pin. The number of GND pins depends on the package used. All must be connected. | GND |
| VCCAUX | Dedicated auxiliary power supply pin. The number of VCCAUX pins depends on the package used. All must be connected to +2.5V. | VCCAUX |
| VCCINT | Dedicated internal core logic power supply pin. The number of VCCINT pins depends on the package used. All must be connected to +1.2V. | VCCINT |
| VCCO | Dedicated I/O bank, output buffer power supply pin. Along with other VCCO pins in the same bank, this pin supplies power to the output buffers within the I/O bank and sets the input threshold voltage for some I/O standards. | VCCO_#<br>**CP132 and TQ144 Packages Only:**<br>VCCO_LEFT, VCCO_TOP, VCCO_RIGHT, VCCO_BOTTOM |
| GCLK | Dual-purpose pin that is either a user-I/O pin or an input to a specific global buffer input. Every package has eight dedicated GCLK pins. | IO_Lxxy_#/GCLK0,<br>IO_Lxxy_#/GCLK1,<br>IO_Lxxy_#/GCLK2,<br>IO_Lxxy_#/GCLK3,<br>IO_Lxxy_#/GCLK4,<br>IO_Lxxy_#/GCLK5,<br>IO_Lxxy_#/GCLK6,<br>IO_Lxxy_#/GCLK7 |
| N.C. | This package pin is not connected in this specific device/package combination but may be connected in larger devices in the same package. | N.C. |

**Notes:**

1. # = I/O bank number, an integer between 0 and 7.

I/Os with Lxxy_# are part of a differential output pair. 'L' indicates differential output capability. The "xx" field is a two-digit integer, unique to each bank that identifies a differential pin-pair. The 'y' field is either 'P' for the true signal or 'N' for the inverted signal in the differential pair. The '#' field is the I/O bank number.

## Pin Definitions

Table 70 provides a brief description of each pin listed in the Spartan-3 FPGA pinout tables and package footprint diagrams. Pins are categorized by their pin type, as listed in Table 69. See Detailed, Functional Pin Descriptions for more information.

## Package Overview

Table 81 shows the 10 low-cost, space-saving production package styles for the Spartan-3 family. Each package style is available as a standard and an environmentally-friendly lead-free (Pb-free) option. The Pb-free packages include an extra ‘G’ in the package style name. For example, the standard "VQ100" package becomes "VQG100" when ordered as the Pb-free option. The mechanical dimensions of the standard and Pb-free packages are similar, as shown in the mechanical drawings provided in Table 83.

Not all Spartan-3 device densities are available in all packages. However, for a specific package there is a common footprint that supports the various devices available in that package. See the footprint diagrams that follow.

*Table 81:* **Spartan-3 Family Package Options**

| Package | Leads | Type | Maximum I/O | Pitch (mm) | Footprint (mm) | Height (mm) |
|---|---|---|---|---|---|---|
| VQ100 / VQG100 | 100 | Very-thin Quad Flat Pack | 63 | 0.5 | 16 x 16 | 1.20 |
| CP132 / CPG132(1) | 132 | Chip-Scale Package | 89 | 0.5 | 8 x 8 | 1.10 |
| TQ144 / TQG144 | 144 | Thin Quad Flat Pack | 97 | 0.5 | 22 x 22 | 1.60 |
| PQ208 / PQG208 | 208 | Quad Flat Pack | 141 | 0.5 | 30.6 x 30.6 | 4.10 |
| FT256 / FTG256 | 256 | Fine-pitch, Thin Ball Grid Array | 173 | 1.0 | 17 x 17 | 1.55 |
| FG320 / FGG320 | 320 | Fine-pitch Ball Grid Array | 221 | 1.0 | 19 x 19 | 2.00 |
| FG456 / FGG456 | 456 | Fine-pitch Ball Grid Array | 333 | 1.0 | 23 x 23 | 2.60 |
| FG676 / FGG676 | 676 | Fine-pitch Ball Grid Array | 489 | 1.0 | 27 x 27 | 2.60 |
| FG900 / FGG900 | 900 | Fine-pitch Ball Grid Array | 633 | 1.0 | 31 x 31 | 2.60 |
| FG1156 / FGG1156(1) | 1156 | Fine-pitch Ball Grid Array | 784 | 1.0 | 35 x 35 | 2.60 |

**Notes:**

1. The CP132, CPG132, FG1156, and FGG1156 packages are discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

## Selecting the Right Package Option

Spartan-3 FPGAs are available in both quad-flat pack (QFP) and ball grid array (BGA) packaging options. While QFP packaging offers the lowest absolute cost, the BGA packages are superior in almost every other aspect, as summarized in Table 82. Consequently, Xilinx recommends using BGA packaging whenever possible.

*Table 82:* **Comparing Spartan-3 Device Packaging Options**

| Characteristic | Quad Flat-Pack (QFP) | Ball Grid Array (BGA) |
|---|---|---|
| Maximum User I/O | 141 | 633 |
| Packing Density (Logic/Area) | Good | Better |
| Signal Integrity | Fair | Better |
| Simultaneous Switching Output (SSO) Support | Limited | Better |
| Thermal Dissipation | Fair | Better |
| Minimum Printed Circuit Board (PCB) Layers | 4 | 6 |
| Hand Assembly/Rework | Possible | Very Difficult |

## TQ144: 144-lead Thin Quad Flat Package

The XC3S50, the XC3S200, and the XC3S400 are available in the 144-lead thin quad flat package, TQ144. All devices share a common footprint for this package as shown in Table 91 and Figure 46.

The TQ144 package only has four separate VCCO inputs, unlike the BGA packages, which have eight separate VCCO inputs. The TQ144 package has a separate VCCO input for the top, bottom, left, and right. However, there are still eight separate I/O banks, as shown in Table 91 and Figure 46. Banks 0 and 1 share the VCCO_TOP input, Banks 2 and 3 share the VCCO_RIGHT input, Banks 4 and 5 share the VCCO_BOTTOM input, and Banks 6 and 7 share the VCCO_LEFT input.

All the package pins appear in Table 91 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

### Pinout Table

*Table 91:* **TQ144 Package Pinout**

| Bank | XC3S50, XC3S200, XC3S400 Pin Name | TQ144 Pin Number | Type |
|---|---|---|---|
| 0 | IO_L01N_0/VRP_0 | P141 | DCI |
| 0 | IO_L01P_0/VRN_0 | P140 | DCI |
| 0 | IO_L27N_0 | P137 | I/O |
| 0 | IO_L27P_0 | P135 | I/O |
| 0 | IO_L30N_0 | P132 | I/O |
| 0 | IO_L30P_0 | P131 | I/O |
| 0 | IO_L31N_0 | P130 | I/O |
| 0 | IO_L31P_0/VREF_0 | P129 | VREF |
| 0 | IO_L32N_0/GCLK7 | P128 | GCLK |
| 0 | IO_L32P_0/GCLK6 | P127 | GCLK |
| 1 | IO | P116 | I/O |
| 1 | IO_L01N_1/VRP_1 | P113 | DCI |
| 1 | IO_L01P_1/VRN_1 | P112 | DCI |
| 1 | IO_L28N_1 | P119 | I/O |
| 1 | IO_L28P_1 | P118 | I/O |
| 1 | IO_L31N_1/VREF_1 | P123 | VREF |
| 1 | IO_L31P_1 | P122 | I/O |
| 1 | IO_L32N_1/GCLK5 | P125 | GCLK |
| 1 | IO_L32P_1/GCLK4 | P124 | GCLK |
| 2 | IO_L01N_2/VRP_2 | P108 | DCI |
| 2 | IO_L01P_2/VRN_2 | P107 | DCI |
| 2 | IO_L20N_2 | P105 | I/O |
| 2 | IO_L20P_2 | P104 | I/O |
| 2 | IO_L21N_2 | P103 | I/O |
| 2 | IO_L21P_2 | P102 | I/O |
| 2 | IO_L22N_2 | P100 | I/O |
| 2 | IO_L22P_2 | P99 | I/O |

*Table 93:* **PQ208 Package Pinout *(Cont'd)***

| Bank | XC3S50 Pin Name | XC3S200, XC3S400 Pin Names | PQ208 Pin Number | Type |
|---|---|---|---|---|
| 3 | IO_L20P_3 | IO_L20P_3 | P114 | I/O |
| 3 | IO_L21N_3 | IO_L21N_3 | P117 | I/O |
| 3 | IO_L21P_3 | IO_L21P_3 | P116 | I/O |
| 3 | IO_L22N_3 | IO_L22N_3 | P120 | I/O |
| 3 | IO_L22P_3 | IO_L22P_3 | P119 | I/O |
| 3 | IO_L23N_3 | IO_L23N_3 | P123 | I/O |
| 3 | IO_L23P_3/VREF_3 | IO_L23P_3/VREF_3 | P122 | VREF |
| 3 | IO_L24N_3 | IO_L24N_3 | P125 | I/O |
| 3 | IO_L24P_3 | IO_L24P_3 | P124 | I/O |
| 3 | N.C. (◆) | IO_L39N_3 | P128 | I/O |
| 3 | N.C. (◆) | IO_L39P_3 | P126 | I/O |
| 3 | IO_L40N_3/VREF_3 | IO_L40N_3/VREF_3 | P131 | VREF |
| 3 | IO_L40P_3 | IO_L40P_3 | P130 | I/O |
| 3 | VCCO_3 | VCCO_3 | P110 | VCCO |
| 3 | VCCO_3 | VCCO_3 | P127 | VCCO |
| 4 | IO | IO | P93 | I/O |
| 4 | N.C. (◆) | IO | P97 | I/O |
| 4 | IO/VREF_4 | IO/VREF_4 | P85 | VREF |
| 4 | N.C. (◆) | IO/VREF_4 | P96 | VREF |
| 4 | IO/VREF_4 | IO/VREF_4 | P102 | VREF |
| 4 | IO_L01N_4/VRP_4 | IO_L01N_4/VRP_4 | P101 | DCI |
| 4 | IO_L01P_4/VRN_4 | IO_L01P_4/VRN_4 | P100 | DCI |
| 4 | IO_L25N_4 | IO_L25N_4 | P95 | I/O |
| 4 | IO_L25P_4 | IO_L25P_4 | P94 | I/O |
| 4 | IO_L27N_4/DIN/D0 | IO_L27N_4/DIN/D0 | P92 | DUAL |
| 4 | IO_L27P_4/D1 | IO_L27P_4/D1 | P90 | DUAL |
| 4 | IO_L30N_4/D2 | IO_L30N_4/D2 | P87 | DUAL |
| 4 | IO_L30P_4/D3 | IO_L30P_4/D3 | P86 | DUAL |
| 4 | IO_L31N_4/INIT_B | IO_L31N_4/INIT_B | P83 | DUAL |
| 4 | IO_L31P_4/DOUT/BUSY | IO_L31P_4/DOUT/BUSY | P81 | DUAL |
| 4 | IO_L32N_4/GCLK1 | IO_L32N_4/GCLK1 | P80 | GCLK |
| 4 | IO_L32P_4/GCLK0 | IO_L32P_4/GCLK0 | P79 | GCLK |
| 4 | VCCO_4 | VCCO_4 | P84 | VCCO |
| 4 | VCCO_4 | VCCO_4 | P98 | VCCO |
| 5 | IO | IO | P63 | I/O |
| 5 | IO | IO | P71 | I/O |
| 5 | IO/VREF_5 | IO/VREF_5 | P78 | VREF |
| 5 | IO_L01N_5/RDWR_B | IO_L01N_5/RDWR_B | P58 | DUAL |
| 5 | IO_L01P_5/CS_B | IO_L01P_5/CS_B | P57 | DUAL |
| 5 | IO_L10N_5/VRP_5 | IO_L10N_5/VRP_5 | P62 | DCI |

*Table 96:* **FT256 Package Pinout *(Cont'd)***

| Bank | XC3S200, XC3S400, XC3S1000 Pin Name | FT256 Pin Number | Type |
|---|---|---|---|
| 6 | IO_L16P_6 | N3 | I/O |
| 6 | IO_L17N_6 | N2 | I/O |
| 6 | IO_L17P_6/VREF_6 | N1 | VREF |
| 6 | IO_L19N_6 | M4 | I/O |
| 6 | IO_L19P_6 | M3 | I/O |
| 6 | IO_L20N_6 | M2 | I/O |
| 6 | IO_L20P_6 | M1 | I/O |
| 6 | IO_L21N_6 | L5 | I/O |
| 6 | IO_L21P_6 | L4 | I/O |
| 6 | IO_L22N_6 | L3 | I/O |
| 6 | IO_L22P_6 | L2 | I/O |
| 6 | IO_L23N_6 | K5 | I/O |
| 6 | IO_L23P_6 | K4 | I/O |
| 6 | IO_L24N_6/VREF_6 | K3 | VREF |
| 6 | IO_L24P_6 | K2 | I/O |
| 6 | IO_L39N_6 | J4 | I/O |
| 6 | IO_L39P_6 | J3 | I/O |
| 6 | IO_L40N_6 | J2 | I/O |
| 6 | IO_L40P_6/VREF_6 | J1 | VREF |
| 6 | VCCO_6 | J5 | VCCO |
| 6 | VCCO_6 | J6 | VCCO |
| 6 | VCCO_6 | K6 | VCCO |
| 7 | IO | G2 | I/O |
| 7 | IO_L01N_7/VRP_7 | C1 | DCI |
| 7 | IO_L01P_7/VRN_7 | B1 | DCI |
| 7 | IO_L16N_7 | C2 | I/O |
| 7 | IO_L16P_7/VREF_7 | C3 | VREF |
| 7 | IO_L17N_7 | D1 | I/O |
| 7 | IO_L17P_7 | D2 | I/O |
| 7 | IO_L19N_7/VREF_7 | E3 | VREF |
| 7 | IO_L19P_7 | D3 | I/O |
| 7 | IO_L20N_7 | E1 | I/O |
| 7 | IO_L20P_7 | E2 | I/O |
| 7 | IO_L21N_7 | F4 | I/O |
| 7 | IO_L21P_7 | E4 | I/O |
| 7 | IO_L22N_7 | F2 | I/O |
| 7 | IO_L22P_7 | F3 | I/O |
| 7 | IO_L23N_7 | G5 | I/O |
| 7 | IO_L23P_7 | F5 | I/O |
| 7 | IO_L24N_7 | G3 | I/O |

*Table 96:* **FT256 Package Pinout *(Cont'd)***

| Bank | XC3S200, XC3S400, XC3S1000 Pin Name | FT256 Pin Number | Type |
|---|---|---|---|
| 7 | IO_L24P_7 | G4 | I/O |
| 7 | IO_L39N_7 | H3 | I/O |
| 7 | IO_L39P_7 | H4 | I/O |
| 7 | IO_L40N_7/VREF_7 | H1 | VREF |
| 7 | IO_L40P_7 | G1 | I/O |
| 7 | VCCO_7 | G6 | VCCO |
| 7 | VCCO_7 | H5 | VCCO |
| 7 | VCCO_7 | H6 | VCCO |
| N/A | GND | A1 | GND |
| N/A | GND | A16 | GND |
| N/A | GND | B2 | GND |
| N/A | GND | B9 | GND |
| N/A | GND | B15 | GND |
| N/A | GND | F6 | GND |
| N/A | GND | F11 | GND |
| N/A | GND | G7 | GND |
| N/A | GND | G8 | GND |
| N/A | GND | G9 | GND |
| N/A | GND | G10 | GND |
| N/A | GND | H2 | GND |
| N/A | GND | H7 | GND |
| N/A | GND | H8 | GND |
| N/A | GND | H9 | GND |
| N/A | GND | H10 | GND |
| N/A | GND | J7 | GND |
| N/A | GND | J8 | GND |
| N/A | GND | J9 | GND |
| N/A | GND | J10 | GND |
| N/A | GND | J15 | GND |
| N/A | GND | K7 | GND |
| N/A | GND | K8 | GND |
| N/A | GND | K9 | GND |
| N/A | GND | K10 | GND |
| N/A | GND | L6 | GND |
| N/A | GND | L11 | GND |
| N/A | GND | R2 | GND |
| N/A | GND | R8 | GND |
| N/A | GND | R15 | GND |
| N/A | GND | T1 | GND |

*Table 98:* **FG320 Package Pinout *(Cont'd)***

| Bank | XC3S400, XC3S1000, XC3S1500 Pin Name | FG320 Pin Number | Type |
|---|---|---|---|
| N/A | VCCINT | N6 | VCCINT |
| N/A | VCCINT | N7 | VCCINT |
| VCCAUX | CCLK | T15 | CONFIG |
| VCCAUX | DONE | R15 | CONFIG |
| VCCAUX | HSWAP_EN | E6 | CONFIG |
| VCCAUX | M0 | P5 | CONFIG |
| VCCAUX | M1 | U3 | CONFIG |
| VCCAUX | M2 | R4 | CONFIG |
| VCCAUX | PROG_B | E5 | CONFIG |
| VCCAUX | TCK | E14 | JTAG |
| VCCAUX | TDI | D4 | JTAG |
| VCCAUX | TDO | D15 | JTAG |
| VCCAUX | TMS | B16 | JTAG |

## User I/Os by Bank

Table 99 indicates how the available user-I/O pins are distributed between the eight I/O banks on the FG320 package.

*Table 99:* **User I/Os Per Bank in FG320 Package**

| Package Edge | I/O Bank | Maximum I/O | Maximum LVDS Pairs | All Possible I/O Pins by Type | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | I/O | DUAL | DCI | VREF | GCLK |
| Top | 0 | 26 | 11 | 19 | 0 | 2 | 3 | 2 |
| | 1 | 26 | 11 | 19 | 0 | 2 | 3 | 2 |
| Right | 2 | 29 | 14 | 23 | 0 | 2 | 4 | 0 |
| | 3 | 29 | 14 | 23 | 0 | 2 | 4 | 0 |
| Bottom | 4 | 27 | 11 | 13 | 6 | 2 | 4 | 2 |
| | 5 | 26 | 11 | 13 | 6 | 2 | 3 | 2 |
| Left | 6 | 29 | 14 | 23 | 0 | 2 | 4 | 0 |
| | 7 | 29 | 14 | 23 | 0 | 2 | 4 | 0 |

*Table 103:* **FG676 Package Pinout *(Cont'd)***

| Bank | XC3S1000 Pin Name | XC3S1500 Pin Name | XC3S2000 Pin Name | XC3S4000 Pin Name | XC3S5000 Pin Name | FG676 Pin Number | Type |
|---|---|---|---|---|---|---|---|
| 6 | IO_L20N_6 | IO_L20N_6 | IO_L20N_6 | IO_L20N_6 | IO_L20N_6 | V7 | I/O |
| 6 | IO_L20P_6 | IO_L20P_6 | IO_L20P_6 | IO_L20P_6 | IO_L20P_6 | U7 | I/O |
| 6 | IO_L21N_6 | IO_L21N_6 | IO_L21N_6 | IO_L21N_6 | IO_L21N_6 | V5 | I/O |
| 6 | IO_L21P_6 | IO_L21P_6 | IO_L21P_6 | IO_L21P_6 | IO_L21P_6 | V4 | I/O |
| 6 | IO_L22N_6 | IO_L22N_6 | IO_L22N_6 | IO_L22N_6 | IO_L22N_6 | V3 | I/O |
| 6 | IO_L22P_6 | IO_L22P_6 | IO_L22P_6 | IO_L22P_6 | IO_L22P_6 | V2 | I/O |
| 6 | IO_L23N_6 | IO_L23N_6 | IO_L23N_6 | IO_L23N_6 | IO_L23N_6 | U6 | I/O |
| 6 | IO_L23P_6 | IO_L23P_6 | IO_L23P_6 | IO_L23P_6 | IO_L23P_6 | U5 | I/O |
| 6 | IO_L24N_6/VREF_6 | IO_L24N_6/VREF_6 | IO_L24N_6/VREF_6 | IO_L24N_6/VREF_6 | IO_L24N_6/VREF_6 | U4 | VREF |
| 6 | IO_L24P_6 | IO_L24P_6 | IO_L24P_6 | IO_L24P_6 | IO_L24P_6 | U3 | I/O |
| 6 | IO_L26N_6 | IO_L26N_6 | IO_L26N_6 | IO_L26N_6 | IO_L26N_6 | U2 | I/O |
| 6 | IO_L26P_6 | IO_L26P_6 | IO_L26P_6 | IO_L26P_6 | IO_L26P_6 | U1 | I/O |
| 6 | IO_L27N_6 | IO_L27N_6 | IO_L27N_6 | IO_L27N_6 | IO_L27N_6 | T8 | I/O |
| 6 | IO_L27P_6 | IO_L27P_6 | IO_L27P_6 | IO_L27P_6 | IO_L27P_6 | T7 | I/O |
| 6 | IO_L28N_6 | IO_L28N_6 | IO_L28N_6 | IO_L28N_6 | IO_L28N_6 | T6 | I/O |
| 6 | IO_L28P_6 | IO_L28P_6 | IO_L28P_6 | IO_L28P_6 | IO_L28P_6 | T5 | I/O |
| 6 | IO_L29N_6 | IO_L29N_6 | IO_L29N_6 | IO_L29N_6 | IO_L29N_6 | T2 | I/O |
| 6 | IO_L29P_6 | IO_L29P_6 | IO_L29P_6 | IO_L29P_6 | IO_L29P_6 | T1 | I/O |
| 6 | IO_L31N_6 | IO_L31N_6 | IO_L31N_6 | IO_L31N_6 | IO_L31N_6 | R8 | I/O |
| 6 | IO_L31P_6 | IO_L31P_6 | IO_L31P_6 | IO_L31P_6 | IO_L31P_6 | R7 | I/O |
| 6 | IO_L32N_6 | IO_L32N_6 | IO_L32N_6 | IO_L32N_6 | IO_L32N_6 | R6 | I/O |
| 6 | IO_L32P_6 | IO_L32P_6 | IO_L32P_6 | IO_L32P_6 | IO_L32P_6 | R5 | I/O |
| 6 | IO_L33N_6 | IO_L33N_6 | IO_L33N_6 | IO_L33N_6 | IO_L33N_6 | T4 | I/O |
| 6 | IO_L33P_6 | IO_L33P_6 | IO_L33P_6 | IO_L33P_6 | IO_L33P_6 | R3 | I/O |
| 6 | IO_L34N_6/VREF_6 | IO_L34N_6/VREF_6 | IO_L34N_6/VREF_6 | IO_L34N_6/VREF_6 | IO_L34N_6/VREF_6 | R2 | VREF |
| 6 | IO_L34P_6 | IO_L34P_6 | IO_L34P_6 | IO_L34P_6 | IO_L34P_6 | R1 | I/O |
| 6 | IO_L35N_6 | IO_L35N_6 | IO_L35N_6 | IO_L35N_6 | IO_L35N_6 | P8 | I/O |
| 6 | IO_L35P_6 | IO_L35P_6 | IO_L35P_6 | IO_L35P_6 | IO_L35P_6 | P7 | I/O |
| 6 | IO_L38N_6 | IO_L38N_6 | IO_L38N_6 | IO_L38N_6 | IO_L38N_6 | P6 | I/O |
| 6 | IO_L38P_6 | IO_L38P_6 | IO_L38P_6 | IO_L38P_6 | IO_L38P_6 | P5 | I/O |
| 6 | IO_L39N_6 | IO_L39N_6 | IO_L39N_6 | IO_L39N_6 | IO_L39N_6 | P4 | I/O |
| 6 | IO_L39P_6 | IO_L39P_6 | IO_L39P_6 | IO_L39P_6 | IO_L39P_6 | P3 | I/O |
| 6 | IO_L40N_6 | IO_L40N_6 | IO_L40N_6 | IO_L40N_6 | IO_L40N_6 | P2 | I/O |
| 6 | IO_L40P_6/VREF_6 | IO_L40P_6/VREF_6 | IO_L40P_6/VREF_6 | IO_L40P_6/VREF_6 | IO_L40P_6/VREF_6 | P1 | VREF |
| 6 | VCCO_6 | VCCO_6 | VCCO_6 | VCCO_6 | VCCO_6 | P9 | VCCO |
| 6 | VCCO_6 | VCCO_6 | VCCO_6 | VCCO_6 | VCCO_6 | P10 | VCCO |
| 6 | VCCO_6 | VCCO_6 | VCCO_6 | VCCO_6 | VCCO_6 | R9 | VCCO |
| 6 | VCCO_6 | VCCO_6 | VCCO_6 | VCCO_6 | VCCO_6 | T3 | VCCO |
| 6 | VCCO_6 | VCCO_6 | VCCO_6 | VCCO_6 | VCCO_6 | T9 | VCCO |
| 6 | VCCO_6 | VCCO_6 | VCCO_6 | VCCO_6 | VCCO_6 | U8 | VCCO |
| 6 | VCCO_6 | VCCO_6 | VCCO_6 | VCCO_6 | VCCO_6 | V8 | VCCO |
| 6 | VCCO_6 | VCCO_6 | VCCO_6 | VCCO_6 | VCCO_6 | Y3 | VCCO |
| 7 | IO_L01N_7/VRP_7 | IO_L01N_7/VRP_7 | IO_L01N_7/VRP_7 | IO_L01N_7/VRP_7 | IO_L01N_7/VRP_7 | F5 | DCI |

*Table 107:* **FG900 Package Pinout *(Cont'd)***

| Bank | XC3S2000 Pin Name | XC3S4000, XC3S5000 Pin Name | FG900 Pin Number | Type |
|---|---|---|---|---|
| 1 | IO_L25P_1 | IO_L25P_1 | D19 | I/O |
| 1 | IO_L26N_1 | IO_L26N_1 | A19 | I/O |
| 1 | IO_L26P_1 | IO_L26P_1 | B19 | I/O |
| 1 | IO_L27N_1 | IO_L27N_1 | F17 | I/O |
| 1 | IO_L27P_1 | IO_L27P_1 | G17 | I/O |
| 1 | IO_L28N_1 | IO_L28N_1 | B17 | I/O |
| 1 | IO_L28P_1 | IO_L28P_1 | C17 | I/O |
| 1 | IO_L29N_1 | IO_L29N_1 | J16 | I/O |
| 1 | IO_L29P_1 | IO_L29P_1 | K16 | I/O |
| 1 | IO_L30N_1 | IO_L30N_1 | G16 | I/O |
| 1 | IO_L30P_1 | IO_L30P_1 | H16 | I/O |
| 1 | IO_L31N_1/VREF_1 | IO_L31N_1/VREF_1 | D16 | VREF |
| 1 | IO_L31P_1 | IO_L31P_1 | E16 | I/O |
| 1 | IO_L32N_1/GCLK5 | IO_L32N_1/GCLK5 | B16 | GCLK |
| 1 | IO_L32P_1/GCLK4 | IO_L32P_1/GCLK4 | C16 | GCLK |
| 1 | N.C. (◆) | IO_L37N_1 | H18 | I/O |
| 1 | N.C. (◆) | IO_L37P_1 | J18 | I/O |
| 1 | N.C. (◆) | IO_L38N_1 | D18 | I/O |
| 1 | N.C. (◆) | IO_L38P_1 | E18 | I/O |
| 1 | N.C. (◆) | IO_L39N_1 | A18 | I/O |
| 1 | N.C. (◆) | IO_L39P_1 | B18 | I/O |
| 1 | N.C. (◆) | IO_L40N_1 | K17 | I/O |
| 1 | N.C. (◆) | IO_L40P_1 | K18 | I/O |
| 1 | VCCO_1 | VCCO_1 | L17 | VCCO |
| 1 | VCCO_1 | VCCO_1 | C18 | VCCO |
| 1 | VCCO_1 | VCCO_1 | G18 | VCCO |
| 1 | VCCO_1 | VCCO_1 | L18 | VCCO |
| 1 | VCCO_1 | VCCO_1 | L19 | VCCO |
| 1 | VCCO_1 | VCCO_1 | J20 | VCCO |
| 1 | VCCO_1 | VCCO_1 | C22 | VCCO |
| 1 | VCCO_1 | VCCO_1 | G22 | VCCO |
| 1 | VCCO_1 | VCCO_1 | E24 | VCCO |
| 1 | VCCO_1 | VCCO_1 | C26 | VCCO |
| 2 | IO | IO | J25 | I/O |
| 2 | IO_L01N_2/VRP_2 | IO_L01N_2/VRP_2 | C29 | DCI |
| 2 | IO_L01P_2/VRN_2 | IO_L01P_2/VRN_2 | C30 | DCI |
| 2 | IO_L02N_2 | IO_L02N_2 | D27 | I/O |
| 2 | IO_L02P_2 | IO_L02P_2 | D28 | I/O |
| 2 | IO_L03N_2/VREF_2 | IO_L03N_2/VREF_2 | D29 | VREF |
| 2 | IO_L03P_2 | IO_L03P_2 | D30 | I/O |

*Table 110:* **FG1156 Package Pinout *(Cont'd)***

| Bank | XC3S4000 Pin Name | XC3S5000 Pin Name | FG1156 Pin Number | Type |
|---|---|---|---|---|
| 1 | VCCO_1 | VCCO_1 | M22 | VCCO |
| 2 | IO | IO | G33 | I/O |
| 2 | IO | IO | G34 | I/O |
| 2 | IO | IO | U25 | I/O |
| 2 | IO | IO | U26 | I/O |
| 2 | IO_L01N_2/VRP_2 | IO_L01N_2/VRP_2 | C33 | DCI |
| 2 | IO_L01P_2/VRN_2 | IO_L01P_2/VRN_2 | C34 | DCI |
| 2 | IO_L02N_2 | IO_L02N_2 | D33 | I/O |
| 2 | IO_L02P_2 | IO_L02P_2 | D34 | I/O |
| 2 | IO_L03N_2/VREF_2 | IO_L03N_2/VREF_2 | E32 | VREF |
| 2 | IO_L03P_2 | IO_L03P_2 | E33 | I/O |
| 2 | IO_L04N_2 | IO_L04N_2 | F31 | I/O |
| 2 | IO_L04P_2 | IO_L04P_2 | F32 | I/O |
| 2 | IO_L05N_2 | IO_L05N_2 | G29 | I/O |
| 2 | IO_L05P_2 | IO_L05P_2 | G30 | I/O |
| 2 | IO_L06N_2 | IO_L06N_2 | H29 | I/O |
| 2 | IO_L06P_2 | IO_L06P_2 | H30 | I/O |
| 2 | IO_L07N_2 | IO_L07N_2 | H33 | I/O |
| 2 | IO_L07P_2 | IO_L07P_2 | H34 | I/O |
| 2 | IO_L08N_2 | IO_L08N_2 | J28 | I/O |
| 2 | IO_L08P_2 | IO_L08P_2 | J29 | I/O |
| 2 | IO_L09N_2/VREF_2 | IO_L09N_2/VREF_2 | H31 | VREF |
| 2 | IO_L09P_2 | IO_L09P_2 | J31 | I/O |
| 2 | IO_L10N_2 | IO_L10N_2 | J32 | I/O |
| 2 | IO_L10P_2 | IO_L10P_2 | J33 | I/O |
| 2 | IO_L11N_2 | IO_L11N_2 | J27 | I/O |
| 2 | IO_L11P_2 | IO_L11P_2 | K26 | I/O |
| 2 | IO_L12N_2 | IO_L12N_2 | K27 | I/O |
| 2 | IO_L12P_2 | IO_L12P_2 | K28 | I/O |
| 2 | IO_L13N_2 | IO_L13N_2 | K29 | I/O |
| 2 | IO_L13P_2/VREF_2 | IO_L13P_2/VREF_2 | K30 | VREF |
| 2 | IO_L14N_2 | IO_L14N_2 | K31 | I/O |
| 2 | IO_L14P_2 | IO_L14P_2 | K32 | I/O |
| 2 | IO_L15N_2 | IO_L15N_2 | K33 | I/O |
| 2 | IO_L15P_2 | IO_L15P_2 | K34 | I/O |
| 2 | IO_L16N_2 | IO_L16N_2 | L25 | I/O |
| 2 | IO_L16P_2 | IO_L16P_2 | L26 | I/O |
| 2 | N.C. (◆) | IO_L17N_2 | L28 | I/O |
| 2 | N.C. (◆) | IO_L17P_2/VREF_2 | L29 | VREF |

*Table 110:* **FG1156 Package Pinout *(Cont'd)***

| Bank | XC3S4000 Pin Name | XC3S5000 Pin Name | FG1156 Pin Number | Type |
|---|---|---|---|---|
| 7 | IO_L45P_7 | IO_L45P_7 | M2 | I/O |
| 7 | IO_L46N_7 | IO_L46N_7 | N7 | I/O |
| 7 | IO_L46P_7 | IO_L46P_7 | N8 | I/O |
| 7 | N.C. (◆) | IO_L47N_7 | P9 | I/O |
| 7 | N.C. (◆) | IO_L47P_7 | P10 | I/O |
| 7 | IO_L49N_7 | IO_L49N_7 | P1 | I/O |
| 7 | IO_L49P_7 | IO_L49P_7 | P2 | I/O |
| 7 | IO_L50N_7 | IO_L50N_7 | R10 | I/O |
| 7 | IO_L50P_7 | IO_L50P_7 | R11 | I/O |
| 7 | N.C. (◆) | IO_L51N_7 | U11 | I/O |
| 7 | N.C. (◆) | IO_L51P_7 | T11 | I/O |
| 7 | VCCO_7 | VCCO_7 | D3 | VCCO |
| 7 | VCCO_7 | VCCO_7 | H3 | VCCO |
| 7 | VCCO_7 | VCCO_7 | H7 | VCCO |
| 7 | VCCO_7 | VCCO_7 | L4 | VCCO |
| 7 | VCCO_7 | VCCO_7 | L8 | VCCO |
| 7 | VCCO_7 | VCCO_7 | N12 | VCCO |
| 7 | VCCO_7 | VCCO_7 | N2 | VCCO |
| 7 | VCCO_7 | VCCO_7 | N6 | VCCO |
| 7 | VCCO_7 | VCCO_7 | P12 | VCCO |
| 7 | VCCO_7 | VCCO_7 | R12 | VCCO |
| 7 | VCCO_7 | VCCO_7 | R8 | VCCO |
| 7 | VCCO_7 | VCCO_7 | T12 | VCCO |
| 7 | VCCO_7 | VCCO_7 | T4 | VCCO |
| N/A | GND | GND | A1 | GND |
| N/A | GND | GND | A13 | GND |
| N/A | GND | GND | A16 | GND |
| N/A | GND | GND | A19 | GND |
| N/A | GND | GND | A2 | GND |
| N/A | GND | GND | A22 | GND |
| N/A | GND | GND | A26 | GND |
| N/A | GND | GND | A30 | GND |
| N/A | GND | GND | A33 | GND |
| N/A | GND | GND | A34 | GND |
| N/A | GND | GND | A5 | GND |
| N/A | GND | GND | A9 | GND |
| N/A | GND | GND | AA14 | GND |
| N/A | GND | GND | AA15 | GND |
| N/A | GND | GND | AA16 | GND |
| N/A | GND | GND | AA17 | GND |

*Table 110:* **FG1156 Package Pinout *(Cont'd)***

| Bank | XC3S4000 Pin Name | XC3S5000 Pin Name | FG1156 Pin Number | Type |
|---|---|---|---|---|
| N/A | GND | GND | AA18 | GND |
| N/A | GND | GND | AA19 | GND |
| N/A | GND | GND | AA20 | GND |
| N/A | GND | GND | AA21 | GND |
| N/A | GND | GND | AB1 | GND |
| N/A | GND | GND | AB17 | GND |
| N/A | GND | GND | AB18 | GND |
| N/A | GND | GND | AB26 | GND |
| N/A | GND | GND | AB30 | GND |
| N/A | GND | GND | AB34 | GND |
| N/A | GND | GND | AB5 | GND |
| N/A | GND | GND | AB9 | GND |
| N/A | GND | GND | AD3 | GND |
| N/A | GND | GND | AD32 | GND |
| N/A | GND | GND | AE10 | GND |
| N/A | GND | GND | AE25 | GND |
| N/A | GND | GND | AF1 | GND |
| N/A | GND | GND | AF13 | GND |
| N/A | GND | GND | AF16 | GND |
| N/A | GND | GND | AF19 | GND |
| N/A | GND | GND | AF22 | GND |
| N/A | GND | GND | AF30 | GND |
| N/A | GND | GND | AF34 | GND |
| N/A | GND | GND | AF5 | GND |
| N/A | GND | GND | AH28 | GND |
| N/A | GND | GND | AH7 | GND |
| N/A | GND | GND | AK1 | GND |
| N/A | GND | GND | AK13 | GND |
| N/A | GND | GND | AK16 | GND |
| N/A | GND | GND | AK19 | GND |
| N/A | GND | GND | AK22 | GND |
| N/A | GND | GND | AK26 | GND |
| N/A | GND | GND | AK30 | GND |
| N/A | GND | GND | AK34 | GND |
| N/A | GND | GND | AK5 | GND |
| N/A | GND | GND | AK9 | GND |
| N/A | GND | GND | AM11 | GND |
| N/A | GND | GND | AM24 | GND |
| N/A | GND | GND | AM3 | GND |
| N/A | GND | GND | AM32 | GND |

*Table 110:* **FG1156 Package Pinout *(Cont'd)***

| Bank | XC3S4000 Pin Name | XC3S5000 Pin Name | FG1156 Pin Number | Type |
|---|---|---|---|---|
| N/A | GND | GND | Y14 | GND |
| N/A | GND | GND | Y15 | GND |
| N/A | GND | GND | Y16 | GND |
| N/A | GND | GND | Y17 | GND |
| N/A | GND | GND | Y18 | GND |
| N/A | GND | GND | Y19 | GND |
| N/A | GND | GND | Y20 | GND |
| N/A | GND | GND | Y21 | GND |
| N/A | N.C. (◆) | N.C. (■) | AK31 | N.C. |
| N/A | VCCAUX | VCCAUX | AD30 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AD5 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AG16 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AG19 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AJ30 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AJ5 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AK11 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AK15 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AK20 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AK24 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AK29 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AK6 | VCCAUX |
| N/A | VCCAUX | VCCAUX | E11 | VCCAUX |
| N/A | VCCAUX | VCCAUX | E15 | VCCAUX |
| N/A | VCCAUX | VCCAUX | E20 | VCCAUX |
| N/A | VCCAUX | VCCAUX | E24 | VCCAUX |
| N/A | VCCAUX | VCCAUX | E29 | VCCAUX |
| N/A | VCCAUX | VCCAUX | E6 | VCCAUX |
| N/A | VCCAUX | VCCAUX | F30 | VCCAUX |
| N/A | VCCAUX | VCCAUX | F5 | VCCAUX |
| N/A | VCCAUX | VCCAUX | H16 | VCCAUX |
| N/A | VCCAUX | VCCAUX | H19 | VCCAUX |
| N/A | VCCAUX | VCCAUX | L30 | VCCAUX |
| N/A | VCCAUX | VCCAUX | L5 | VCCAUX |
| N/A | VCCAUX | VCCAUX | R30 | VCCAUX |
| N/A | VCCAUX | VCCAUX | R5 | VCCAUX |
| N/A | VCCAUX | VCCAUX | T27 | VCCAUX |
| N/A | VCCAUX | VCCAUX | T8 | VCCAUX |
| N/A | VCCAUX | VCCAUX | W27 | VCCAUX |
| N/A | VCCAUX | VCCAUX | W8 | VCCAUX |
| N/A | VCCAUX | VCCAUX | Y30 | VCCAUX |

## User I/Os by Bank

**Note:** The FG(G)1156 package is discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

Table 111 indicates how the available user-I/O pins are distributed between the eight I/O banks for the XC3S4000 in the FG1156 package. Similarly, Table 112 shows how the available user-I/O pins are distributed between the eight I/O banks for the XC3S5000 in the FG1156 package.

*Table 111:* **User I/Os Per Bank for XC3S4000 in FG1156 Package**

| Package Edge | I/O Bank | Maximum I/O | All Possible I/O Pins by Type | | | | |
|---|---|---|---|---|---|---|---|
| | | | I/O | DUAL | DCI | VREF | GCLK |
| Top | 0 | 90 | 79 | 0 | 2 | 7 | 2 |
| | 1 | 90 | 79 | 0 | 2 | 7 | 2 |
| Right | 2 | 88 | 80 | 0 | 2 | 6 | 0 |
| | 3 | 88 | 79 | 0 | 2 | 7 | 0 |
| Bottom | 4 | 90 | 73 | 6 | 2 | 7 | 2 |
| | 5 | 90 | 73 | 6 | 2 | 7 | 2 |
| Left | 6 | 88 | 79 | 0 | 2 | 7 | 0 |
| | 7 | 88 | 79 | 0 | 2 | 7 | 0 |

**Notes:**

1. The FG1156 and FGG1156 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.

*Table 112:* **User I/Os Per Bank for XC3S5000 in FG1156 Package**

| Package Edge | I/O Bank | Maximum I/O | All Possible I/O Pins by Type | | | | |
|---|---|---|---|---|---|---|---|
| | | | I/O | DUAL | DCI | VREF | GCLK |
| Top | 0 | 100 | 89 | 0 | 2 | 7 | 2 |
| | 1 | 100 | 89 | 0 | 2 | 7 | 2 |
| Right | 2 | 96 | 87 | 0 | 2 | 7 | 0 |
| | 3 | 96 | 87 | 0 | 2 | 7 | 0 |
| Bottom | 4 | 100 | 83 | 6 | 2 | 7 | 2 |
| | 5 | 100 | 83 | 6 | 2 | 7 | 2 |
| Left | 6 | 96 | 87 | 0 | 2 | 7 | 0 |
| | 7 | 96 | 87 | 0 | 2 | 7 | 0 |

**Notes:**

1. The FG1156 and FGG1156 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.