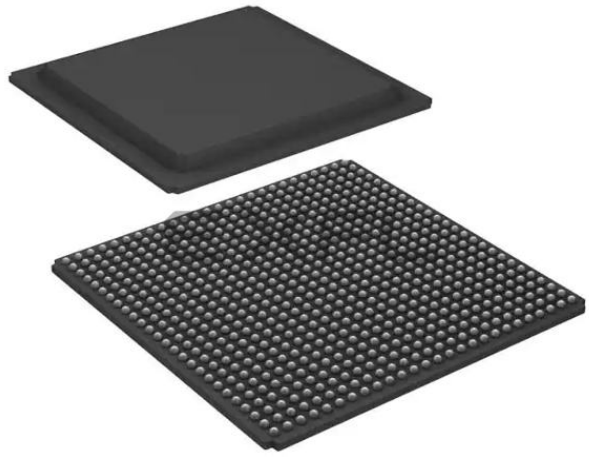

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	6912
Number of Logic Elements/Cells	62208
Total RAM Bits	1769472
Number of I/O	489
Number of Gates	4000000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s4000-4fg676c

According to Figure 7, the clock line OTCLK1 connects the CK inputs of the upper registers on the output and three-state paths. Similarly, OTCLK2 connects the CK inputs for the lower registers on the output and three-state paths. The upper and lower registers on the input path have independent clock lines: ICLK1 and ICLK2. The enable line OCE connects the CE inputs of the upper and lower registers on the output path. Similarly, TCE connects the CE inputs for the register pair on the three-state path and ICE does the same for the register pair on the input path. The Set/Reset (SR) line entering the IOB is common to all six registers, as is the Reverse (REV) line.

Each storage element supports numerous options in addition to the control over signal polarity described in the IOB Overview section. These are described in Table 6.

Table 6: **Storage Element Options**

Option Switch	Function	Specificity
FF/Latch	Chooses between an edge-sensitive flip-flop or a level-sensitive latch	Independent for each storage element.
SYNC/ASYNC	Determines whether SR is synchronous or asynchronous	Independent for each storage element.
SRHIGH/SRLOW	Determines whether SR acts as a Set, which forces the storage element to a logic “1" (SRHIGH) or a Reset, which forces a logic “0” (SRLOW).	Independent for each storage element, except when using FDDR. In the latter case, the selection for the upper element (OFF1 or TFF2) applies to both elements.
INIT1/INIT0	In the event of a Global Set/Reset, after configuration or upon activation of the GSR net, this switch decides whether to set or reset a storage element. By default, choosing SRLOW also selects INIT0; choosing SRHIGH also selects INIT1.	Independent for each storage element, except when using FDDR. In the latter case, selecting INIT0 for one element applies to both elements (even though INIT1 is selected for the other).

Double-Data-Rate Transmission

Double-Data-Rate (DDR) transmission describes the technique of synchronizing signals to both the rising and falling edges of the clock signal. Spartan-3 devices use register-pairs in all three IOB paths to perform DDR operations.

The pair of storage elements on the IOB’s Output path (OFF1 and OFF2), used as registers, combine with a special multiplexer to form a DDR D-type flip-flop (FDDR). This primitive permits DDR transmission where output data bits are synchronized to both the rising and falling edges of a clock. It is possible to access this function by placing either an FDDRRSE or an FDDRCPE component or symbol into the design. DDR operation requires two clock signals (50% duty cycle), one the inverted form of the other. These signals trigger the two registers in alternating fashion, as shown in Figure 8. Commonly, the Digital Clock Manager (DCM) generates the two clock signals by mirroring an incoming signal, then shifting it 180 degrees. This approach ensures minimal skew between the two signals.

The storage-element-pair on the Three-State path (TFF1 and TFF2) can also be combined with a local multiplexer to form an FDDR primitive. This permits synchronizing the output enable to both the rising and falling edges of a clock. This DDR operation is realized in the same way as for the output path.

The storage-element-pair on the input path (IFF1 and IFF2) allows an I/O to receive a DDR signal. An incoming DDR clock signal triggers one register and the inverted clock signal triggers the other register. In this way, the registers take turns capturing bits of the incoming DDR data signal.

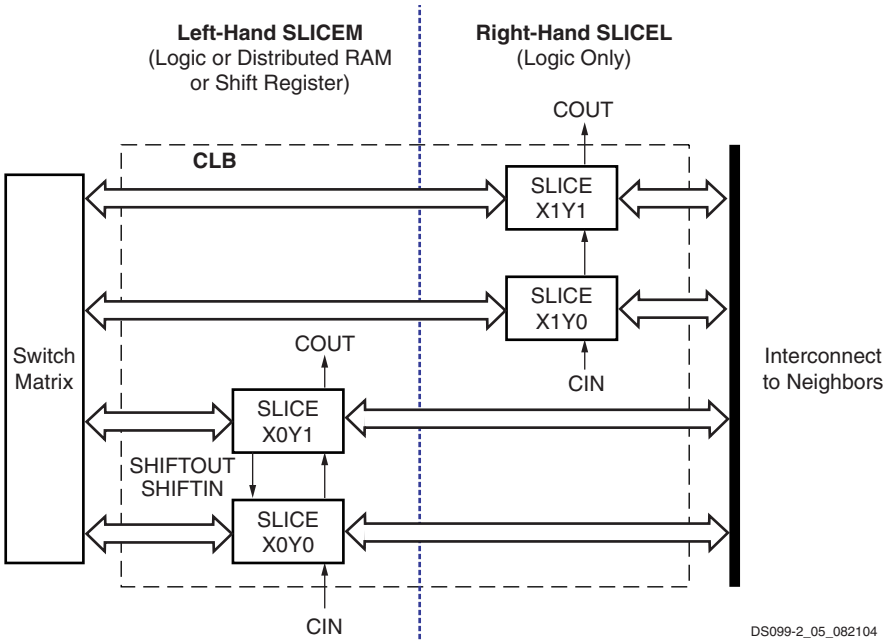


Figure 11: **Arrangement of Slices within the CLB**

Elements Within a Slice

All four slices have the following elements in common: two logic function generators, two storage elements, wide-function multiplexers, carry logic, and arithmetic gates, as shown in Figure 12, page 24. Both the left-hand and right-hand slice pairs use these elements to provide logic, arithmetic, and ROM functions. Besides these, the left-hand pair supports two additional functions: storing data using Distributed RAM and shifting data with 16-bit registers. Figure 12 is a diagram of the left-hand slice; therefore, it represents a superset of the elements and connections to be found in all slices. See Function Generator, page 25 for more information.

The RAM-based function generator—also known as a Look-Up Table or LUT—is the main resource for implementing logic functions. Furthermore, the LUTs in each left-hand slice pair can be configured as Distributed RAM or a 16-bit shift register. For information on the former, refer to the chapter entitled “Using Look-Up Tables as Distributed RAM” in UG331; for information on the latter, refer to the chapter entitled “Using Look-Up Tables as Shift Registers” in UG331. The function generators located in the upper and lower portions of the slice are referred to as the "G" and "F", respectively.

The storage element, which is programmable as either a D-type flip-flop or a level-sensitive latch, provides a means for synchronizing data to a clock signal, among other uses. The storage elements in the upper and lower portions of the slice are called FFY and FFX, respectively.

Wide-function multiplexers effectively combine LUTs in order to permit more complex logic operations. Each slice has two of these multiplexers with F5MUX in the lower portion of the slice and FiMUX in the upper portion. Depending on the slice, FiMUX takes on the name F6MUX, F7MUX, or F8MUX. For more details on the multiplexers, refer to the chapter entitled “Using Dedicated Multiplexers” in UG331.

The carry chain, together with various dedicated arithmetic logic gates, support fast and efficient implementations of math operations. The carry chain enters the slice as CIN and exits as COUT. Five multiplexers control the chain: CYINIT, CY0F, and CYMUXF in the lower portion as well as CY0G and CYMUXG in the upper portion. The dedicated arithmetic logic includes the exclusive-OR gates XORG and XORF (upper and lower portions of the slice, respectively) as well as the AND gates GAND and FAND (upper and lower portions, respectively). For more details on the carry logic, refer to the chapter entitled “Using Carry and Arithmetic Logic” in UG331.

Main Logic Paths

Central to the operation of each slice are two nearly identical data paths, distinguished using the terms *top* and *bottom*. The description that follows uses names associated with the bottom path. (The top path names appear in parentheses.) The basic path originates at an interconnect-switch matrix outside the CLB. Four lines, F1 through F4 (or G1 through G4 on the

upper path), enter the slice and connect directly to the LUT. Once inside the slice, the lower 4-bit path passes through a function generator ‘F’ (or ‘G’) that performs logic operations. The function generator’s Data output, ‘D’, offers five possible paths:

- Exit the slice via line ‘X’ (or ‘Y’) and return to interconnect.
- Inside the slice, ‘X’ (or ‘Y’) serves as an input to the DXMUX (DYMUX) which feeds the data input, ‘D’, of the FFX (FFY) storage element. The ‘Q’ output of the storage element drives the line XQ (or YQ) which exits the slice.
- Control the CYMUXF (or CYMUXG) multiplexer on the carry chain.
- With the carry chain, serve as an input to the XORF (or XORG) exclusive-OR gate that performs arithmetic operations, producing a result on ‘X’ (or ‘Y’).
- Drive the multiplexer F5MUX to implement logic functions wider than four bits. The ‘D’ outputs of both the F-LUT and G-LUT serve as data inputs to this multiplexer.

In addition to the main logic paths described above, there are two bypass paths that enter the slice as BX and BY. Once inside the FPGA, BX in the bottom half of the slice (or BY in the top half) can take any of several possible branches:

- Bypass both the LUT and the storage element, then exit the slice as BXOUT (or BYOUT) and return to interconnect.
- Bypass the LUT, then pass through a storage element via the D input before exiting as XQ (or YQ).
- Control the wide function multiplexer F5MUX (or F6MUX).
- Via multiplexers, serve as an input to the carry chain.
- Drives the DI input of the LUT.
- BY can control the REV inputs of both the FFY and FFX storage elements.
- Finally, the DIG_MUX multiplexer can switch BY onto the DIG line, which exits the slice.

Other slice signals shown in Figure 12 are discussed in the sections that follow.

Function Generator

Each of the two LUTs (F and G) in a slice have four logic inputs (A1-A4) and a single output (D). This permits any four-variable Boolean logic operation to be programmed into them. Furthermore, wide function multiplexers can be used to effectively combine LUTs within the same CLB or across different CLBs, making logic functions with still more input variables possible.

The LUTs in both the right-hand and left-hand slice-pairs not only support the logic functions described above, but also can function as ROM that is initialized with data at the time of configuration.

The LUTs in the left-hand slice-pair (even-numbered columns such as X0 in Figure 11) of each CLB support two additional functions that the right-hand slice-pair (odd-numbered columns such as X1) do not.

First, it is possible to program the “left-hand LUTs” as distributed RAM. This type of memory affords moderate amounts of data buffering anywhere along a data path. One left-hand LUT stores 16 bits. Multiple left-hand LUTs can be combined in various ways to store larger amounts of data. A dual port option combines two LUTs so that memory access is possible from two independent data lines. A Distributed ROM option permits pre-loading the memory with data during FPGA configuration.

Second, it is possible to program each left-hand LUT as a 16-bit shift register. Used in this way, each LUT can delay serial data anywhere from one to 16 clock cycles. The four left-hand LUTs of a single CLB can be combined to produce delays up to 64 clock cycles. The SHIFTIN and SHIFTOUT lines cascade LUTs to form larger shift registers. It is also possible to combine shift registers across more than one CLB. The resulting programmable delays can be used to balance the timing of data pipelines.

Block RAM Overview

All Spartan-3 devices support block RAM, which is organized as configurable, synchronous 18Kbit blocks. Block RAM stores relatively large amounts of data more efficiently than the distributed RAM feature described earlier. (The latter is better suited for buffering small amounts of data anywhere along signal paths.) This section describes basic Block RAM functions. For more information, refer to the chapter entitled “Using Block RAM” in UG331.

The aspect ratio—i.e., width vs. depth—of each block RAM is configurable. Furthermore, multiple blocks can be cascaded to create still wider and/or deeper memories.

A choice among primitives determines whether the block RAM functions as dual- or single-port memory. A name of the form RAMB16_S[w_A]_S[w_B] calls out the dual-port primitive, where the integers w_A and w_B specify the total data path width at ports w_A and w_B, respectively. Thus, a RAMB16_S9_S18 is a dual-port RAM with a 9-bit-wide Port A and an 18-bit-wide Port B. A name of the form RAMB16_S[w] identifies the single-port primitive, where the integer w specifies the total data path width of the lone port. A RAMB16_S18 is a single-port RAM with an 18-bit-wide port. Other memory functions—e.g., FIFOs, data path width conversion, ROM, etc.—are readily available using the CORE Generator™ software, part of the Xilinx development software.

DFS Clock Output Connections

There are two basic cases that determine how to connect the DFS clock outputs: on-chip and off-chip, which are illustrated in sections [a] and [c], respectively, of Figure 21. This is similar to what has already been described for the DLL component. See DLL Clock Output and Feedback Connections, page 34.

In the on-chip case, it is possible to connect either of the DFS's two output clock signals through general routing resources to the FPGA's internal registers. Either a Global Clock Buffer (BUFG) or a BUFGMUX affords access to the global clock network. The optional feedback loop is formed in this way, routing CLK0 to a global clock net, which in turn drives the CLKFB input.

In the off-chip case, the DFS's two output clock signals, plus CLK0 for an optional feedback loop, can exit the FPGA using output buffers (OBUF) to drive a clock network plus registers on the board. The feedback loop is formed by feeding the CLK0 signal back into the FPGA using an IBUFG, which directly accesses the global clock network, or an IBUF. Then, the global clock net is connected directly to the CLKFB input.

Phase Shifter (PS)

The DCM provides two approaches to controlling the phase of a DCM clock output signal relative to the CLKIN signal: First, there are nine clock outputs that employ the DLL to achieve a desired phase relationship: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, CLKDV CLKFX, and CLKFX180. These outputs afford "coarse" phase control.

The second approach uses the PS component described in this section to provide a still finer degree of control. The PS component is only available when the DLL is operating in its low-frequency mode. The PS component phase shifts the DCM output clocks by introducing a "fine phase shift" (T_{PS}) between the CLKFB and CLKIN signals inside the DLL component. The user can control this fine phase shift down to a resolution of 1/256 of a CLKIN cycle or one tap delay (DCM_TAP), whichever is greater. When in use, the PS component shifts the phase of all nine DCM clock output signals together. If the PS component is used together with a DCM clock output such as the CLK90, CLK180, CLK270, CLK2X180 and CLKFX180, then the fine phase shift of the former gets added to the coarse phase shift of the latter.

PS Component Enabling and Mode Selection

The CLKOUT_PHASE_SHIFT attribute enables the PS component for use in addition to selecting between two operating modes. As described in Table 20, this attribute has three possible values: NONE, FIXED and VARIABLE. When CLKOUT_PHASE_SHIFT is set to NONE, the PS component is disabled and its inputs, PSEN, PSCLK, and PSINCDEC, must be tied to GND. The set of waveforms in section [a] of Figure 22 shows the disabled case, where the DLL maintains a zero-phase alignment of signals CLKFB and CLKIN upon which the PS component has no effect. The PS component is enabled by setting the attribute to either the FIXED or VARIABLE values, which select the Fixed Phase mode and the Variable Phase mode, respectively. These two modes are described in the sections that follow

Determining the Fine Phase Shift

The user controls the phase shift of CLKFB relative to CLKIN by setting and/or adjusting the value of the PHASE_SHIFT attribute. This value must be an integer ranging from –255 to +255. The PS component uses this value to calculate the desired fine phase shift (T_{PS}) as a fraction of the CLKIN period (T_{CLKIN}). Given values for PHASE-SHIFT and T_{CLKIN}, it is possible to calculate T_{PS} as follows:

$$T_{PS} = T_{CLKIN}(PHASE\_SHIFT/256) \qquad \textit{Equation 4}$$

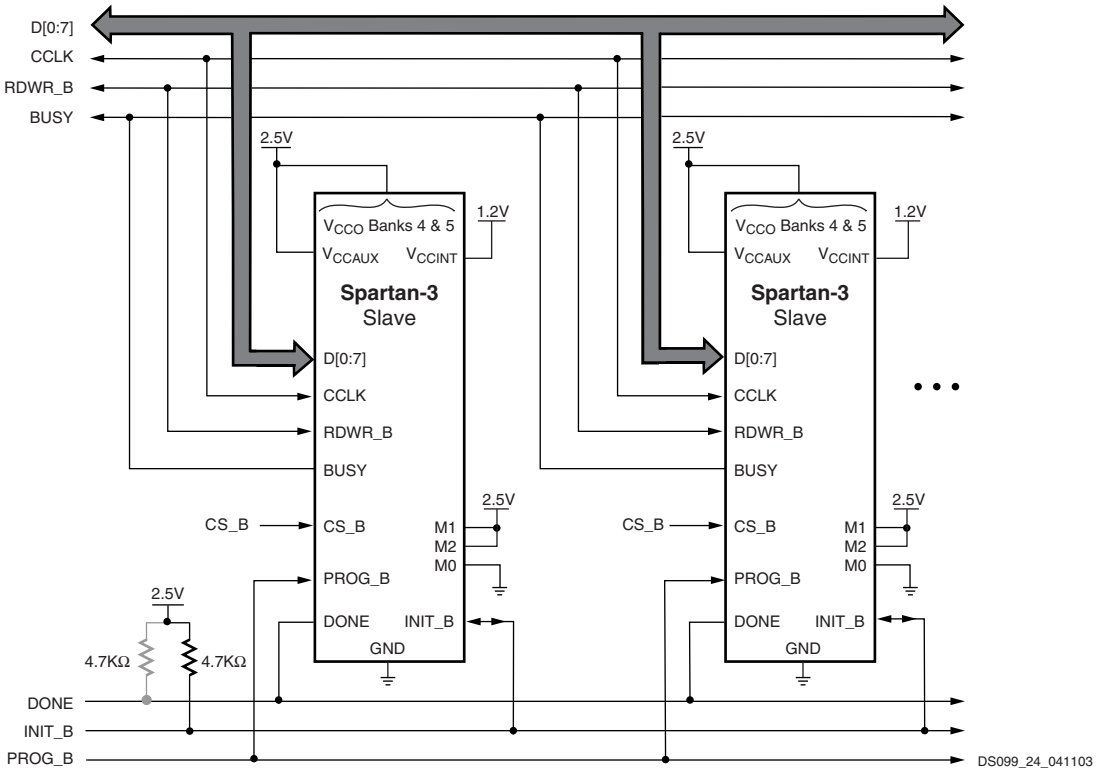
Both the Fixed Phase and Variable Phase operating modes employ this calculation. If the PHASE_SHIFT value is zero, then CLKFB and CLKIN will be in phase, the same as when the PS component is disabled. When the PHASE_SHIFT value is positive, the CLKFB signal will be shifted later in time with respect to CLKIN. If the attribute value is negative, the CLKFB signal will be shifted earlier in time with respect to CLKIN.

The Fixed Phase Mode

This mode fixes the desired fine phase shift to a fraction of the T_{CLKIN}, as determined by Equation 4 and its user-selected PHASE_SHIFT value P. The set of waveforms insection [b] of Figure 22 illustrates the relationship between CLKFB and CLKIN in the Fixed Phase mode. In the Fixed Phase mode, the PSEN, PSCLK and PSINCDEC inputs are not used and must be tied to GND. Fixed phase shift requires ISE software version 10.1.03 or later.

(e.g. all configuration pins taken together) when operating in the User mode. This is accomplished by setting the *Persist* option to *Yes*.

Multiple FPGAs can be configured using the Slave Parallel mode and can be made to start-up simultaneously. Figure 27 shows the device connections. To configure multiple devices in this way, wire the individual CCLK, Data, RDWR_B, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by deasserting the CS_B pin of each device in turn and writing the appropriate data.



Notes:

1. There are two ways to use the DONE line. First, one may set the BitGen option DriveDone to "Yes" only for the last FPGA to be configured in the chain shown above (or for the single FPGA as may be the case). This enables the DONE pin to drive High; thus, no pull-up resistor is necessary. DriveDone is set to "No" for the remaining FPGAs in the chain. Second, DriveDone can be set to "No" for all FPGAs. Then all DONE lines are open-drain and require the pull-up resistor shown in grey. In most cases, a value between 3.3KΩ to 4.7KΩ is sufficient. However, when using DONE synchronously with a long chain of FPGAs, cumulative capacitance may necessitate lower resistor values (e.g. down to 330Ω) in order to ensure a rise time within one clock cycle.
2. If the FPGAs use different configuration data files, configure them in sequence by first asserting the CS_B of one FPGA then asserting the CS_B of the other FPGA.
3. For information on how to program the FPGA using 3.3V signals and power, see 3.3V-Tolerant Configuration Interface.

Figure 27: **Connection Diagram for Slave Parallel Configuration**

DC Electrical Characteristics

In this section, specifications may be designated as Advance, Preliminary, or Production. These terms are defined as follows:

- **Advance:** Initial estimates are based on simulation, early characterization, and/or extrapolation from the characteristics of other families. Values are subject to change. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur. Use as estimates, not for production.
- **Preliminary:** Based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reported delays is greatly reduced compared to Advance data. Use as estimates, not for production.
- **Production:** These specifications are approved only after silicon has been characterized over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Parameter values are considered stable with no future changes expected.

  Production-quality systems must only use FPGA designs compiled with a Production status speed file. FPGA designs using a less mature speed file designation should only be used during system prototyping or preproduction qualification. FPGA designs with speed files designated as Advance or Preliminary should not be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the latest Xilinx ISE® software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **The following applies unless otherwise noted: The parameter values published in this module apply to all Spartan®-3 devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.** All parameters representing voltages are measured with respect to GND.

Mask and Fab Revisions

Some specifications list different values for one or more mask or fab revisions, indicated by the device top marking (see Package Marking, page 5). The revision differences involve the power ramp rates, differential DC specifications, and DCM characteristics. The most recent revision (mask rev E and GQ fab/geometry code) is errata-free with improved specifications than earlier revisions.

Mask rev E with fab rev GQ has been shipping since 2005 (see XCN05009) and has been 100% of Xilinx Spartan-3 device shipments since 2006. SCD 0974 was provided to ensure the receipt of the rev E silicon, but it is no longer needed. Parts ordered under the SCD appended “0974” to the standard part number. For example, “XC3S50-4VQ100C” became “XC3S50-4VQ100C0974”.

Table 28: **Absolute Maximum Ratings**

Symbol	Description	Conditions		Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND			–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage relative to GND			–0.5	3.00	V
V_{CCO}	Output driver supply voltage relative to GND			–0.5	3.75	V
V_{REF}	Input reference voltage relative to GND			–0.5	V_{CCO} + 0.5	V
V_{IN}	Voltage applied to all User I/O pins and Dual-Purpose pins relative to GND(2,4)	Driver in a high-impedance state	Commercial	–0.95	4.4	V
			Industrial	–0.85	4.3	
	Voltage applied to all Dedicated pins relative to GND(3)		All temp. ranges	–0.5	V_{CCAUX} + 0.5	V

Table 36: **DC Characteristics of User I/Os Using Single-Ended Standards *(Cont'd)***

Signal Standard (IOSTANDARD) and Current Drive Attribute (mA)		Test Conditions		Logic Level Characteristics	
		I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
LVCMOS33[4]	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24	24	–24		
LVDCI_33, LVDCI_DV2_33		Note 3	Note 3		
LVTTL[4]	2	2	–2	0.4	2.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24	24	–24		
PCI33_3		Note 6	Note 6	$0.10V_{CCO}$	$0.90V_{CCO}$
SSTL18_I		6.7	–6.7	V_{TT} – 0.475	V_{TT} + 0.475
SSTL18_I_DCI		Note 3	Note 3		
SSTL18_II		13.4	–13.4	V_{TT} – 0.475	V_{TT} + 0.475
SSTL2_I		8.1	–8.1	V_{TT} – 0.61	V_{TT} + 0.61
SSTL2_I_DCI		Note 3	Note 3		
SSTL2_II[7]		16.2	–16.2	V_{TT} – 0.81	V_{TT} + 0.81
SSTL2_II_DCI[7]		Note 3	Note 3		

Notes:

1. The numbers in this table are based on the conditions set forth in Table 32 and Table 35.
2. Descriptions of the symbols used in this table are as follows:
   I_{OL} – the output current condition under which VOL is tested
   I_{OH} – the output current condition under which VOH is tested
   V_{OL} – the output voltage that indicates a Low logic level
   V_{OH} – the output voltage that indicates a High logic level
   V_{IL} – the input voltage that indicates a Low logic level
   V_{IH} – the input voltage that indicates a High logic level
   V_{CCO} – the supply voltage for output drivers as well as LVCMOS, LVTTL, and PCI inputs
   V_{REF} – the reference voltage for setting the input switching threshold
   V_{TT} – the voltage applied to a resistor termination
3. Tested according to the standard's relevant specifications. When using the DCI version of a standard on a given I/O bank, that bank will consume more power than if the non-DCI version had been used instead. The additional power is drawn for the purpose of impedance-matching at the I/O pins. A portion of this power is dissipated in the two RREF resistors.
4. For the LVCMOS and LVTTL standards: the same V_{OL} and V_{OH} limits apply for both the Fast and Slow slew attributes.
5. All dedicated output pins (CCLK, DONE, and TDO) and dual-purpose totem-pole output pins (D0-D7 and BUSY/DOUT) exhibit the characteristics of LVCMOS25 with 12 mA drive and slow slew rate. For information concerning the use of 3.3V signals, see 3.3V-Tolerant Configuration Interface, page 47.
6. Tested according to the relevant PCI specifications. For more information, see XAPP457.
7. The minimum usable V_{TT} voltage is 1.25V.

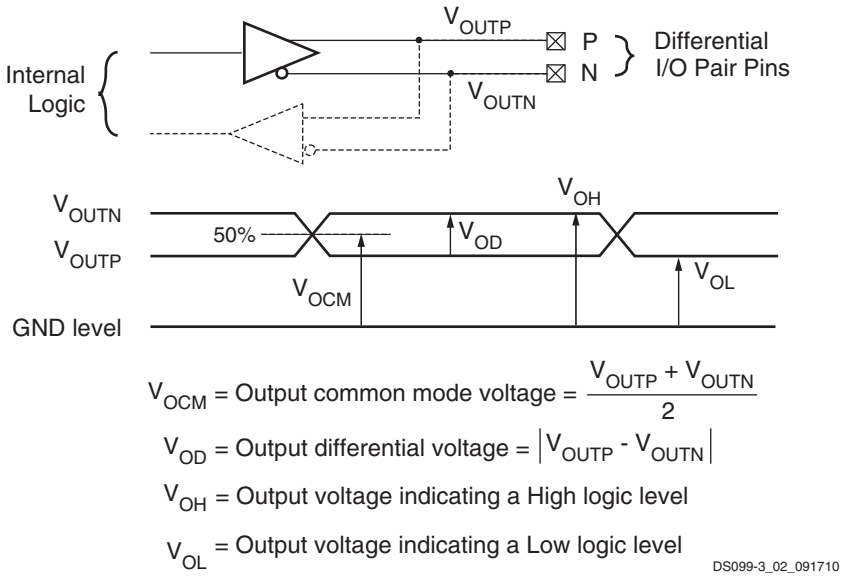


Figure 33: **Differential Output Voltages**

Table 38: **DC Characteristics of User I/Os Using Differential Signal Standards**

Signal Standard	Mask[3] Revision	V_{OD}			V_{OCM}			V_{OH}	V_{OL}
		Min (mV)	Typ (mV)	Max (mV)	Min (V)	Typ (V)	Max (V)	Min (V)	Max (V)
LDT_25 (ULVDS_25)	All	430[4]	600	670	0.495	0.600	0.715	0.71	0.50
LVDS_25	All	100	–	600	0.80	–	1.6	0.85	1.55
	'E'	200	–	500	1.0	–	1.5	1.10	1.40
BLVDS_25[5]	All	250	350	450	–	1.20	–	–	–
LVDSEXT_25	All	100	–	600	0.80	–	1.6	0.85	1.55
	'E'	300	–	700	1.0	–	1.5	1.15	1.35
LVPECL_25[5]	All	–	–	-	–	–	-	1.35	1.005
RSDS_25[6]	All	100	–	600	0.80	–	1.6	0.85	1.55
	'E'	200	–	500	1.0	–	1.5	1.10	1.40
DIFF_HSTL_II_18	All	–	–	–	–	–	–	V_{CCO} – 0.40	0.40
DIFF_SSTL2_II	All	–	–	–	–	–	–	V_{TT} + 0.80	V_{TT} – 0.80

Notes:

1. The numbers in this table are based on the conditions set forth in Table 32 and Table 37.
2. Output voltage measurements for all differential standards are made with a termination resistor (R_T) of 100Ω across the N and P pins of the differential signal pair.
3. Mask revision E devices have tighter output ranges but can be used in any design that was in a previous revision. See Mask and Fab Revisions, page 58.
4. This value must be compatible with the receiver to which the FPGA's output pair is connected.
5. Each LVPECL_25 or BLVDS_25 output-pair requires three external resistors for proper output operation as shown in Figure 34. Each LVPECL_25 or BLVDS_25 input-pair uses a 100W termination resistor at the receiver.
6. Only one of the differential standards RSDS_25, LDT_25, LVDS_25, and LVDSEXT_25 may be used for outputs within a bank. Each differential standard input-pair requires an external 100Ω termination resistor.

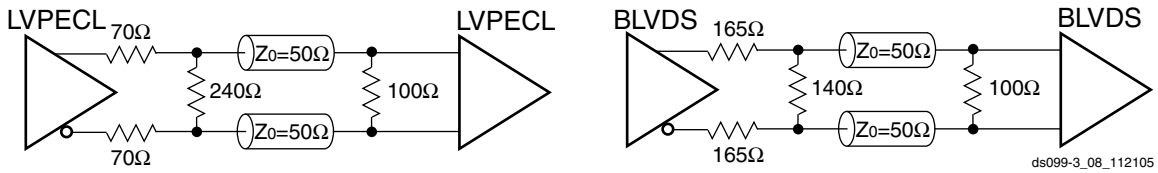


Figure 34: **External Termination Required for LVPECL and BLVDS Output and Input**

Table 67: **Timing for the Master and Slave Parallel Configuration Modes *(Cont'd)***

Symbol	Description			Slave/ Master	All Speed Grades		Units
					Min	Max	
Clock Timing							
T_{CCH}	CCLK input pin High pulse width			Slave	5	∞	ns
T_{CCL}	CCLK input pin Low pulse width				5	∞	ns
F_{CCPAR}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	Not using the BUSY pin(4)		0	50	MHz
			Using the BUSY pin		0	66	MHz
		With bitstream compression			0	20	MHz
		During STARTUP phase			0	50	MHz
ΔF_{CCPAR}	Variation from the CCLK output frequency set using the BitGen option ConfigRate			Master	–50%	+50%	–

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32.
2. Some Xilinx documents may refer to Parallel modes as "SelectMAP" modes.
3. RDWR_B is synchronized to CCLK for the purpose of performing the Abort operation. The same pin asynchronously controls the driver impedance of the D0 - D7 pins. To avoid contention when writing configuration data to the D0 - D7 bus, do not bring RDWR_B High when CS_B is Low.
4. In the Slave Parallel mode, it is necessary to use the BUSY pin when the CCLK frequency exceeds this maximum specification.

Date	Version	Description
05/25/07	2.2	Improved absolute maximum voltage specifications in Table 28, providing additional overshoot allowance. Improved XC3S50 HBM ESD to 2000V in Table 28. Based on extensive 90 nm production data, improved (reduced) the maximum quiescent current limits for the I_{CCINTQ} and I_{CCOQ} specifications in Table 34. Widened the recommended voltage range for the PCI standard and clarified the hysteresis footnote in Table 35. Noted restriction on combining differential outputs in Table 38. Updated footnote 1 in Table 64.
11/30/07	2.3	Updated 3.3V VCCO max from 3.45V to 3.465V in Table 32 and elsewhere. Reduced t_{ICCK} minimum from 0.50µs to 0.25µs in Table 65. Updated links to technical documentation.
06/25/08	2.4	Clarified dual marking. Added Mask and Fab Revisions. Added references to XAPP459 in Table 28 and Table 32. Removed absolute minimum and added footnote referring to timing analyzer for minimum delay values. Added HSLVDCI to Table 48 and Table 50. Updated t_{DICK} in Table 51 to match largest possible value in speed file. Updated formatting and links.
12/04/09	2.5	Updated notes 2 and 3 in Table 28. Removed silicon process specific information and revised notes in Table 30. Updated note 3 in Table 32. Updated note 3 in Table 34. Updated note 5 in Table 35. Updated V_{OL} max and V_{OH} min for SSTL2_II in Table 36. Updated note 5 in Table 36. Updated JTAG Waveforms in Figure 39. Updated V_{ICM} max for LVPECL_25 in Table 37. Updated RT and VT for LVDS_25_DCI in Table 48. Updated Simultaneously Switching Output Guidelines. Noted that the CP132 package is being discontinued in Table 49. Removed minimum values for T_{MULTCK} clock-to-output times in Table 54. Updated footnote 3 in Table 58. Removed minimum values for T_{MULT} propagation times in Table 55. Removed silicon process specific information and revised notes in Table 61. Updated Phase Shifter (PS).
10/29/12	3.0	Added Notice of Disclaimer. Per XCN07022, updated the discontinued FG1156 and FGG1156 package discussion throughout document. Per XCN08011, updated the discontinued CP132 and CPG132 package discussion throughout document. Revised description of V_{IN} in Table 32 and added note 7. Added note 4 to Table 33. This product is not recommended for new designs.

Table 79: **Pin Behavior After Power-Up, During Configuration *(Cont'd)***

Pin Name	Configuration Mode Settings <M2:M1:M0>					Bitstream Configuration Option
	Serial Modes		SelectMap Parallel Modes		JTAG Mode <1:0:1>	
	Master <0:0:0>	Slave <1:1:1>	Master <0:1:1>	Slave <1:1:0>		
IO_Lxxy_#/ D5			D5 (I/O)	D5 (I/O)		Persist UnusedPin
IO_Lxxy_#/ D6			D6 (I/O)	D6 (I/O)		Persist UnusedPin
IO_Lxxy_#/ D7			D7 (I/O)	D7 (I/O)		Persist UnusedPin
IO_Lxxy_#/ CS_B			CS_B (I)	CS_B (I)		Persist UnusedPin
IO_Lxxy_#/ RDWR_B			RDWR_B (I)	RDWR_B (I)		Persist UnusedPin
IO_Lxxy_#/ BUSY/DOUT	DOUT (O)	DOUT (O)	BUSY (O)	BUSY (O)		Persist UnusedPin
DUAL: Dual-purpose configuration pins (INIT_B has a pull-up resistor to VCCO_4 or VCCO_BOTTOM always active during configuration, regardless of HSWAP_EN pin)						
IO_Lxxy_#/ INIT_B	INIT_B (I/OD)	INIT_B (I/OD)	INIT_B (I/OD)	INIT_B (I/OD)		UnusedPin
DCI: Digitally Controlled Impedance reference resistor input pins						
IO_Lxxy_#/ VRN_#						UnusedPin
IO/VRN_#						UnusedPin
IO_Lxxy_#/ VRP_#						UnusedPin
IO/VRP_#						UnusedPin
GCLK: Global clock buffer inputs						
IO_Lxxy_#/ GCLK0 through GCLK7						UnusedPin
VREF: I/O bank input reference voltage pins						
IO_Lxxy_#/ VREF_#						UnusedPin
IO/VREF_#						UnusedPin
CONFIG: Dedicated configuration pins (pull-up resistor to VCCAUX always active during configuration, regardless of HSWAP_EN pin)						
CCLK	CCLK (I/O)	CCLK (I)	CCLK (I/O)	CCLK (I)		CclkPin ConfigRate
PROG_B	PROG_B (I) (pull-up)	PROG_B (I) (pull-up)	PROG_B (I) (pull-up)	PROG_B (I) (pull-up)	PROG_B (I), Via JPROG_B instruction	ProgPin
DONE	DONE (I/OD)	DONE (I/OD)	DONE (I/OD)	DONE (I/OD)	DONE (I/OD)	DriveDone DonePin DonePipe
M2	M2=0 (I)	M2=1 (I)	M2=0 (I)	M2=1 (I)	M2=1 (I)	M2Pin
M1	M1=0 (I)	M1=1 (I)	M1=1 (I)	M1=1 (I)	M1=0 (I)	M1Pin
M0	M0=0 (I)	M0=1 (I)	M0=1 (I)	M0=0 (I)	M0=1 (I)	M0Pin
HSWAP_EN	HSWAP_EN (I)	HSWAP_EN (I)	HSWAP_EN (I)	HSWAP_EN (I)	HSWAP_EN (I)	HswapenPin

Table 87: **VQ100 Package Pinout *(Cont'd)***

Bank	XC3S50 XC3S200 Pin Name	VQ100 Pin Number	Type
VCCAUX	TDO	P76	JTAG
VCCAUX	TMS	P78	JTAG

User I/Os by Bank

Table 88 indicates how the available user-I/O pins are distributed between the eight I/O banks on the VQ100 package.

Table 88: **User I/Os Per Bank in VQ100 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	6	1	0	2	1	2
	1	7	2	0	2	1	2
Right	2	8	5	0	2	1	0
	3	8	5	0	2	1	0
Bottom	4	10	0	6	2	0	2
	5	8	0	6	0	0	2
Left	6	8	4	0	2	2	0
	7	8	5	0	2	1	0

Table 91: **TQ144 Package Pinout *(Cont'd)***

Bank	XC3S50, XC3S200, XC3S400 Pin Name	TQ144 Pin Number	Type
2	IO_L23N_2/VREF_2	P98	VREF
2	IO_L23P_2	P97	I/O
2	IO_L24N_2	P96	I/O
2	IO_L24P_2	P95	I/O
2	IO_L40N_2	P93	I/O
2	IO_L40P_2/VREF_2	P92	VREF
3	IO	P76	I/O
3	IO_L01N_3/VRP_3	P74	DCI
3	IO_L01P_3/VRN_3	P73	DCI
3	IO_L20N_3	P78	I/O
3	IO_L20P_3	P77	I/O
3	IO_L21N_3	P80	I/O
3	IO_L21P_3	P79	I/O
3	IO_L22N_3	P83	I/O
3	IO_L22P_3	P82	I/O
3	IO_L23N_3	P85	I/O
3	IO_L23P_3/VREF_3	P84	VREF
3	IO_L24N_3	P87	I/O
3	IO_L24P_3	P86	I/O
3	IO_L40N_3/VREF_3	P90	VREF
3	IO_L40P_3	P89	I/O
4	IO/VREF_4	P70	VREF
4	IO_L01N_4/VRP_4	P69	DCI
4	IO_L01P_4/VRN_4	P68	DCI
4	IO_L27N_4/DIN/D0	P65	DUAL
4	IO_L27P_4/D1	P63	DUAL
4	IO_L30N_4/D2	P60	DUAL
4	IO_L30P_4/D3	P59	DUAL
4	IO_L31N_4/INIT_B	P58	DUAL
4	IO_L31P_4/DOUT/BUSY	P57	DUAL
4	IO_L32N_4/GCLK1	P56	GCLK
4	IO_L32P_4/GCLK0	P55	GCLK
5	IO/VREF_5	P44	VREF
5	IO_L01N_5/RDWR_B	P41	DUAL
5	IO_L01P_5/CS_B	P40	DUAL
5	IO_L28N_5/D6	P47	DUAL
5	IO_L28P_5/D7	P46	DUAL
5	IO_L31N_5/D4	P51	DUAL
5	IO_L31P_5/D5	P50	DUAL
5	IO_L32N_5/GCLK3	P53	GCLK

User I/Os by Bank

Table 94 indicates how the available user-I/O pins are distributed between the eight I/O banks for the XC3S50 in the PQ208 package. Similarly, Table 95 shows how the available user-I/O pins are distributed between the eight I/O banks for the XC3S200 and XC3S400 in the PQ208 package.

Table 94: **User I/Os Per Bank for XC3S50 in PQ208 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	15	9	0	2	2	2
	1	15	9	0	2	2	2
Right	2	16	13	0	2	2	0
	3	16	12	0	2	2	0
Bottom	4	15	3	6	2	2	2
	5	15	3	6	2	2	2
Left	6	16	12	0	2	2	0
	7	16	12	0	2	2	0

Table 95: **User I/Os Per Bank for XC3S200 and XC3S400 in PQ208 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	16	9	0	2	3	2
	1	15	9	0	2	2	2
Right	2	19	14	0	2	3	0
	3	20	15	0	2	3	0
Bottom	4	17	4	6	2	3	2
	5	15	3	6	2	2	2
Left	6	19	14	0	2	3	0
	7	20	15	0	2	3	0

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
1	IO_L15P_1	IO_L15P_1	E17	I/O
1	IO_L16N_1	IO_L16N_1	B17	I/O
1	IO_L16P_1	IO_L16P_1	C17	I/O
1	N.C. (◆)	IO_L19N_1	C16	I/O
1	N.C. (◆)	IO_L19P_1	D16	I/O
1	N.C. (◆)	IO_L22N_1	A16	I/O
1	N.C. (◆)	IO_L22P_1	B16	I/O
1	IO_L24N_1	IO_L24N_1	D15	I/O
1	IO_L24P_1	IO_L24P_1	E15	I/O
1	IO_L25N_1	IO_L25N_1	B15	I/O
1	IO_L25P_1	IO_L25P_1	A15	I/O
1	IO_L27N_1	IO_L27N_1	D14	I/O
1	IO_L27P_1	IO_L27P_1	E14	I/O
1	IO_L28N_1	IO_L28N_1	A14	I/O
1	IO_L28P_1	IO_L28P_1	B14	I/O
1	IO_L29N_1	IO_L29N_1	C13	I/O
1	IO_L29P_1	IO_L29P_1	D13	I/O
1	IO_L30N_1	IO_L30N_1	A13	I/O
1	IO_L30P_1	IO_L30P_1	B13	I/O
1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	D12	VREF
1	IO_L31P_1	IO_L31P_1	E12	I/O
1	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	B12	GCLK
1	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	C12	GCLK
1	VCCO_1	VCCO_1	C15	VCCO
1	VCCO_1	VCCO_1	F15	VCCO
1	VCCO_1	VCCO_1	G12	VCCO
1	VCCO_1	VCCO_1	G13	VCCO
1	VCCO_1	VCCO_1	G14	VCCO
2	IO	IO	C22	I/O
2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	C20	DCI
2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	C21	DCI
2	IO_L16N_2	IO_L16N_2	D20	I/O
2	IO_L16P_2	IO_L16P_2	D19	I/O
2	IO_L17N_2	IO_L17N_2	D21	I/O
2	IO_L17P_2/VREF_2	IO_L17P_2/VREF_2	D22	VREF
2	IO_L19N_2	IO_L19N_2	E18	I/O
2	IO_L19P_2	IO_L19P_2	F18	I/O
2	IO_L20N_2	IO_L20N_2	E19	I/O
2	IO_L20P_2	IO_L20P_2	E20	I/O
2	IO_L21N_2	IO_L21N_2	E21	I/O

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
6	IO_L20N_6	IO_L20N_6	IO_L20N_6	IO_L20N_6	IO_L20N_6	V7	I/O
6	IO_L20P_6	IO_L20P_6	IO_L20P_6	IO_L20P_6	IO_L20P_6	U7	I/O
6	IO_L21N_6	IO_L21N_6	IO_L21N_6	IO_L21N_6	IO_L21N_6	V5	I/O
6	IO_L21P_6	IO_L21P_6	IO_L21P_6	IO_L21P_6	IO_L21P_6	V4	I/O
6	IO_L22N_6	IO_L22N_6	IO_L22N_6	IO_L22N_6	IO_L22N_6	V3	I/O
6	IO_L22P_6	IO_L22P_6	IO_L22P_6	IO_L22P_6	IO_L22P_6	V2	I/O
6	IO_L23N_6	IO_L23N_6	IO_L23N_6	IO_L23N_6	IO_L23N_6	U6	I/O
6	IO_L23P_6	IO_L23P_6	IO_L23P_6	IO_L23P_6	IO_L23P_6	U5	I/O
6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	U4	VREF
6	IO_L24P_6	IO_L24P_6	IO_L24P_6	IO_L24P_6	IO_L24P_6	U3	I/O
6	IO_L26N_6	IO_L26N_6	IO_L26N_6	IO_L26N_6	IO_L26N_6	U2	I/O
6	IO_L26P_6	IO_L26P_6	IO_L26P_6	IO_L26P_6	IO_L26P_6	U1	I/O
6	IO_L27N_6	IO_L27N_6	IO_L27N_6	IO_L27N_6	IO_L27N_6	T8	I/O
6	IO_L27P_6	IO_L27P_6	IO_L27P_6	IO_L27P_6	IO_L27P_6	T7	I/O
6	IO_L28N_6	IO_L28N_6	IO_L28N_6	IO_L28N_6	IO_L28N_6	T6	I/O
6	IO_L28P_6	IO_L28P_6	IO_L28P_6	IO_L28P_6	IO_L28P_6	T5	I/O
6	IO_L29N_6	IO_L29N_6	IO_L29N_6	IO_L29N_6	IO_L29N_6	T2	I/O
6	IO_L29P_6	IO_L29P_6	IO_L29P_6	IO_L29P_6	IO_L29P_6	T1	I/O
6	IO_L31N_6	IO_L31N_6	IO_L31N_6	IO_L31N_6	IO_L31N_6	R8	I/O
6	IO_L31P_6	IO_L31P_6	IO_L31P_6	IO_L31P_6	IO_L31P_6	R7	I/O
6	IO_L32N_6	IO_L32N_6	IO_L32N_6	IO_L32N_6	IO_L32N_6	R6	I/O
6	IO_L32P_6	IO_L32P_6	IO_L32P_6	IO_L32P_6	IO_L32P_6	R5	I/O
6	IO_L33N_6	IO_L33N_6	IO_L33N_6	IO_L33N_6	IO_L33N_6	T4	I/O
6	IO_L33P_6	IO_L33P_6	IO_L33P_6	IO_L33P_6	IO_L33P_6	R3	I/O
6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	R2	VREF
6	IO_L34P_6	IO_L34P_6	IO_L34P_6	IO_L34P_6	IO_L34P_6	R1	I/O
6	IO_L35N_6	IO_L35N_6	IO_L35N_6	IO_L35N_6	IO_L35N_6	P8	I/O
6	IO_L35P_6	IO_L35P_6	IO_L35P_6	IO_L35P_6	IO_L35P_6	P7	I/O
6	IO_L38N_6	IO_L38N_6	IO_L38N_6	IO_L38N_6	IO_L38N_6	P6	I/O
6	IO_L38P_6	IO_L38P_6	IO_L38P_6	IO_L38P_6	IO_L38P_6	P5	I/O
6	IO_L39N_6	IO_L39N_6	IO_L39N_6	IO_L39N_6	IO_L39N_6	P4	I/O
6	IO_L39P_6	IO_L39P_6	IO_L39P_6	IO_L39P_6	IO_L39P_6	P3	I/O
6	IO_L40N_6	IO_L40N_6	IO_L40N_6	IO_L40N_6	IO_L40N_6	P2	I/O
6	IO_L40P_6/VREF_6	IO_L40P_6/VREF_6	IO_L40P_6/VREF_6	IO_L40P_6/VREF_6	IO_L40P_6/VREF_6	P1	VREF
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	P9	VCCO
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	P10	VCCO
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	R9	VCCO
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	T3	VCCO
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	T9	VCCO
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	U8	VCCO
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	V8	VCCO
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	Y3	VCCO
7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	F5	DCI

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
3	N.C. (◆)	IO_L50P_3	V26	I/O
3	VCCO_3	VCCO_3	U20	VCCO
3	VCCO_3	VCCO_3	V20	VCCO
3	VCCO_3	VCCO_3	W20	VCCO
3	VCCO_3	VCCO_3	Y22	VCCO
3	VCCO_3	VCCO_3	V24	VCCO
3	VCCO_3	VCCO_3	AB24	VCCO
3	VCCO_3	VCCO_3	AD26	VCCO
3	VCCO_3	VCCO_3	V28	VCCO
3	VCCO_3	VCCO_3	AB28	VCCO
3	VCCO_3	VCCO_3	AF28	VCCO
4	IO	IO	AA16	I/O
4	IO	IO	AG18	I/O
4	IO	IO	AA18	I/O
4	IO	IO	AE22	I/O
4	IO	IO	AD23	I/O
4	IO	IO	AH27	I/O
4	IO/VREF_4	IO/VREF_4	AF16	VREF
4	IO/VREF_4	IO/VREF_4	AK28	VREF
4	IO_L01N_4/VRP_4	IO_L01N_4/VRP_4	AJ27	DCI
4	IO_L01P_4/VRN_4	IO_L01P_4/VRN_4	AK27	DCI
4	IO_L02N_4	IO_L02N_4	AJ26	I/O
4	IO_L02P_4	IO_L02P_4	AK26	I/O
4	IO_L03N_4	IO_L03N_4	AG26	I/O
4	IO_L03P_4	IO_L03P_4	AF25	I/O
4	IO_L04N_4	IO_L04N_4	AD24	I/O
4	IO_L04P_4	IO_L04P_4	AC23	I/O
4	IO_L05N_4	IO_L05N_4	AE23	I/O
4	IO_L05P_4	IO_L05P_4	AF23	I/O
4	IO_L06N_4/VREF_4	IO_L06N_4/VREF_4	AG23	VREF
4	IO_L06P_4	IO_L06P_4	AH23	I/O
4	IO_L07N_4	IO_L07N_4	AJ23	I/O
4	IO_L07P_4	IO_L07P_4	AK23	I/O
4	IO_L08N_4	IO_L08N_4	AB22	I/O
4	IO_L08P_4	IO_L08P_4	AC22	I/O
4	IO_L09N_4	IO_L09N_4	AF22	I/O
4	IO_L09P_4	IO_L09P_4	AG22	I/O
4	IO_L10N_4	IO_L10N_4	AJ22	I/O
4	IO_L10P_4	IO_L10P_4	AK22	I/O
4	IO_L11N_4	IO_L11N_4	AD21	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
5	IO_L07N_5	IO_L07N_5	AK8	I/O
5	IO_L07P_5	IO_L07P_5	AJ8	I/O
5	IO_L08N_5	IO_L08N_5	AC9	I/O
5	IO_L08P_5	IO_L08P_5	AB9	I/O
5	IO_L09N_5	IO_L09N_5	AG9	I/O
5	IO_L09P_5	IO_L09P_5	AF9	I/O
5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	AK9	DCI
5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	AJ9	DCI
5	IO_L11N_5/VREF_5	IO_L11N_5/VREF_5	AE10	VREF
5	IO_L11P_5	IO_L11P_5	AE9	I/O
5	IO_L12N_5	IO_L12N_5	AJ10	I/O
5	IO_L12P_5	IO_L12P_5	AH10	I/O
5	IO_L13N_5	IO_L13N_5	AD11	I/O
5	IO_L13P_5	IO_L13P_5	AD10	I/O
5	IO_L14N_5	IO_L14N_5	AF11	I/O
5	IO_L14P_5	IO_L14P_5	AE11	I/O
5	IO_L15N_5	IO_L15N_5	AH11	I/O
5	IO_L15P_5	IO_L15P_5	AG11	I/O
5	IO_L16N_5	IO_L16N_5	AK11	I/O
5	IO_L16P_5	IO_L16P_5	AJ11	I/O
5	IO_L17N_5	IO_L17N_5	AB12	I/O
5	IO_L17P_5	IO_L17P_5	AC11	I/O
5	IO_L18N_5	IO_L18N_5	AD12	I/O
5	IO_L18P_5	IO_L18P_5	AC12	I/O
5	IO_L19N_5	IO_L19N_5	AF12	I/O
5	IO_L19P_5/VREF_5	IO_L19P_5/VREF_5	AE12	VREF
5	IO_L20N_5	IO_L20N_5	AH12	I/O
5	IO_L20P_5	IO_L20P_5	AG12	I/O
5	IO_L21N_5	IO_L21N_5	AK12	I/O
5	IO_L21P_5	IO_L21P_5	AJ12	I/O
5	IO_L22N_5	IO_L22N_5	AA13	I/O
5	IO_L22P_5	IO_L22P_5	AA12	I/O
5	IO_L23N_5	IO_L23N_5	AC13	I/O
5	IO_L23P_5	IO_L23P_5	AB13	I/O
5	IO_L24N_5	IO_L24N_5	AG13	I/O
5	IO_L24P_5	IO_L24P_5	AF13	I/O
5	IO_L25N_5	IO_L25N_5	AK13	I/O
5	IO_L25P_5	IO_L25P_5	AJ13	I/O
5	IO_L26N_5	IO_L26N_5	AB14	I/O
5	IO_L26P_5	IO_L26P_5	AA14	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
N/A	VCCINT	VCCINT	Y22	VCCINT
VCCAUX	CCLK	CCLK	AL31	CONFIG
VCCAUX	DONE	DONE	AD24	CONFIG
VCCAUX	HSWAP_EN	HSWAP_EN	L11	CONFIG
VCCAUX	M0	M0	AL4	CONFIG
VCCAUX	M1	M1	AK4	CONFIG
VCCAUX	M2	M2	AG8	CONFIG
VCCAUX	PROG_B	PROG_B	D4	CONFIG
VCCAUX	TCK	TCK	D31	JTAG
VCCAUX	TDI	TDI	E4	JTAG
VCCAUX	TDO	TDO	E31	JTAG
VCCAUX	TMS	TMS	H27	JTAG