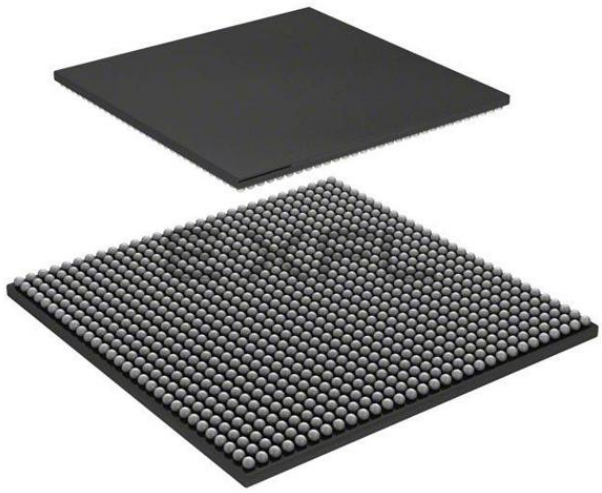

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Details	
Product Status	Active
Number of LABs/CLBs	6912
Number of Logic Elements/Cells	62208
Total RAM Bits	1769472
Number of I/O	633
Number of Gates	4000000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	900-BBGA
Supplier Device Package	900-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s4000-4fg900i

Table 3 shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination.

Table 3: **Spartan-3 Device I/O Chart**

Available User I/Os and Differential (Diff) I/O Pairs by Package Type																				
Package	**VQ100 VQG100**		**CP132(1) CPG132**		**TQ144 TQG144**		**PQ208 PQG208**		**FT256 FTG256**		**FG320 FGG320**		**FG456 FGG456**		**FG676 FGG676**		**FG900 FGG900**		**FG1156(1) FGG1156**	
Footprint (mm)	**16 x 16**		**8 x 8**		**22 x 22**		**30.6 x 30.6**		**17 x 17**		**19 x 19**		**23 x 23**		**27 x 27**		**31 x 31**		**35 x 35**	
Device	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**
XC3S50	63	29	89(1)	44(1)	97	46	124	56	–	–	–	–	–	–	–	–	–	–	–	–
XC3S200	63	29	–	–	97	46	141	62	173	76	–	–	–	–	–	–	–	–	–	–
XC3S400	–	–	–	–	97	46	141	62	173	76	221	100	264	116	–	–	–	–	–	–
XC3S1000	–	–	–	–	–	–	–	–	173	76	221	100	333	149	391	175	–	–	–	–
XC3S1500	–	–	–	–	–	–	–	–	–	–	221	100	333	149	487	221	–	–	–	–
XC3S2000	–	–	–	–	–	–	–	–	–	–	–	–	333	149	489	221	565	270	–	–
XC3S4000	–	–	–	–	–	–	–	–	–	–	–	–	–	–	489	221	633	300	712(1)	312(1)
XC3S5000	–	–	–	–	–	–	–	–	–	–	–	–	–	–	489	221	633	300	784(1)	344(1)

Notes:

1. The CP132, CPG132, FG1156, and FGG1156 packages are discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.
2. All device options listed in a given package column are pin-compatible.
3. User = Single-ended user I/O pins. Diff = Differential I/O pairs.

Package Marking

Figure 2 shows the top marking for Spartan-3 FPGAs in the quad-flat packages. Figure 3 shows the top marking for Spartan-3 FPGAs in BGA packages except the 132-ball chip-scale package (CP132 and CPG132). The markings for the BGA packages are nearly identical to those for the quad-flat packages, except that the marking is rotated with respect to the ball A1 indicator. Figure 4 shows the top marking for Spartan-3 FPGAs in the CP132 and CPG132 packages.

The "5C" and "4I" part combinations may be dual marked as "5C/4I". Devices with the dual mark can be used as either -5C or -4I devices. Devices with a single mark are only guaranteed for the marked speed grade and temperature range. Some specifications vary according to mask revision. Mask revision E devices are errata-free. All shipments since 2006 have been mask revision E.

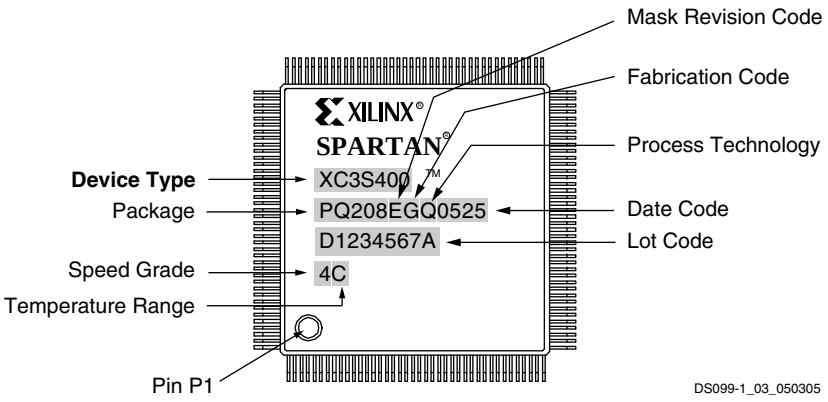

Figure 2: **Spartan-3 FPGA QFP Package Marking Example for Part Number XC3S400-4PQ208C**

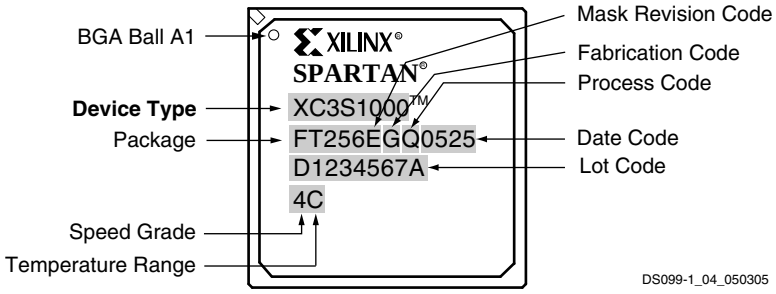

Figure 3: **Spartan-3 FPGA BGA Package Marking Example for Part Number XC3S1000-4FT256C**

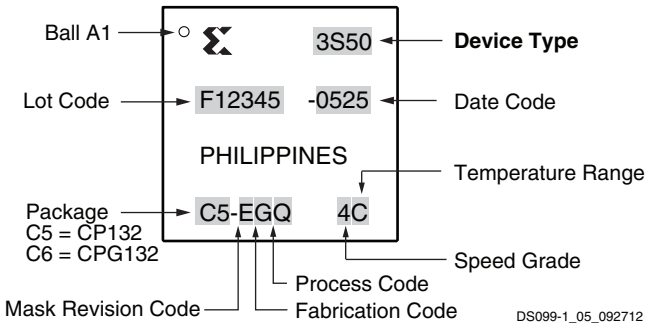

Figure 4: **Spartan-3 FPGA CP132 and CPG132 Package Marking Example for XC3S50-4CP132C**

Ordering Information

Spartan-3 FPGAs are available in both standard (Figure 5) and Pb-free (Figure 6) packaging options for all device/package combinations. The Pb-free packages include a special 'G' character in the ordering code.

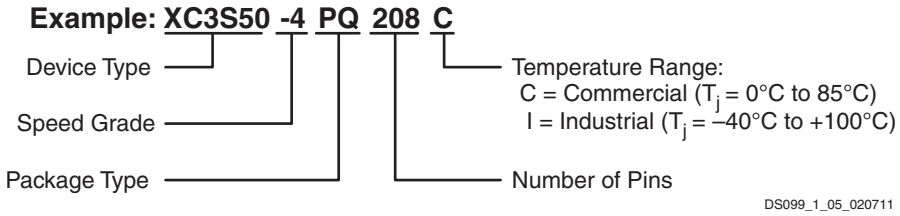

Figure 5: **Standard Packaging**

For additional information on Pb-free packaging, see XAPP427: *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

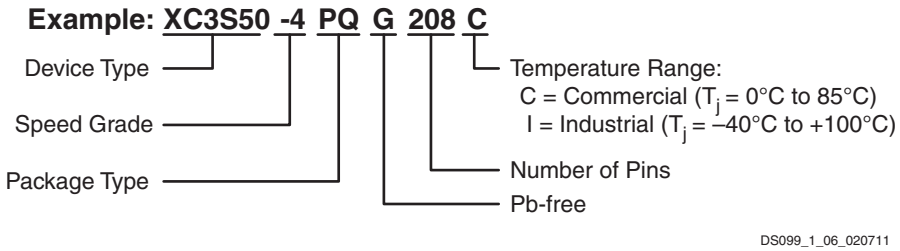

Figure 6: **Pb-Free Packaging**

The DLL component has two clock inputs, CLKIN and CLKFB, as well as seven clock outputs, CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV as described in Table 16. The clock outputs drive simultaneously; however, the High Frequency mode only supports a subset of the outputs available in the Low Frequency mode. See DLL Frequency Modes, page 35. Signals that initialize and report the state of the DLL are discussed in The Status Logic Component, page 41.

Table 16: **DLL Signals**

Signal	Direction	Description	Mode Support	
			Low Frequency	High Frequency
CLKIN	Input	Accepts original clock signal.	Yes	Yes
CLKFB	Input	Accepts either CLK0 or CLK2X as feed back signal. (Set CLK_FEEDBACK attribute accordingly).	Yes	Yes
CLK0	Output	Generates clock signal with same frequency and phase as CLKIN.	Yes	Yes
CLK90	Output	Generates clock signal with same frequency as CLKIN, only phase-shifted 90°.	Yes	No
CLK180	Output	Generates clock signal with same frequency as CLKIN, only phase-shifted 180°.	Yes	Yes
CLK270	Output	Generates clock signal with same frequency as CLKIN, only phase-shifted 270°.	Yes	No
CLK2X	Output	Generates clock signal with same phase as CLKIN, only twice the frequency.	Yes	No
CLK2X180	Output	Generates clock signal with twice the frequency of CLKIN, phase-shifted 180° with respect to CLKIN.	Yes	No
CLKDV	Output	Divides the CLKIN frequency by CLKDV_DIVIDE value to generate lower frequency clock signal that is phase-aligned to CLKIN.	Yes	Yes

The clock signal supplied to the CLKIN input serves as a reference waveform, with which the DLL seeks to align the feedback signal at the CLKFB input. When eliminating clock skew, the common approach to using the DLL is as follows: The CLK0 signal is passed through the clock distribution network to all the registers it synchronizes. These registers are either internal or external to the FPGA. After passing through the clock distribution network, the clock signal returns to the DLL via a feedback line called CLKFB. The control block inside the DLL measures the phase error between CLKFB and CLKIN. This phase error is a measure of the clock skew that the clock distribution network introduces. The control block activates the appropriate number of delay elements to cancel out the clock skew. Once the DLL has brought the CLK0 signal in phase with the CLKIN signal, it asserts the LOCKED output, indicating a “lock” on to the CLKIN signal.

DLL Attributes and Related Functions

A number of different functional options can be set for the DLL component through the use of the attributes described in Table 17. Each attribute is described in detail in the sections that follow:

Table 17: **DLL Attributes**

Attribute	Description	Values
CLK_FEEDBACK	Chooses either the CLK0 or CLK2X output to drive the CLKFB input	NONE, 1X, 2X
DLL_FREQUENCY_MODE	Chooses between High Frequency and Low Frequency modes	LOW, HIGH
CLKIN_DIVIDE_BY_2	Halves the frequency of the CLKIN signal just as it enters the DCM	TRUE, FALSE
CLKDV_DIVIDE	Selects constant used to divide the CLKIN input frequency to generate the CLKDV output frequency	1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, 6.0, 6.5, 7.0, 7.5, 8, 9, 10, 11, 12, 13, 14, 15, and 16.
DUTY_CYCLE_CORRECTION	Enables 50% duty cycle correction for the CLK0, CLK90, CLK180, and CLK270 outputs	TRUE, FALSE

Table 36: **DC Characteristics of User I/Os Using Single-Ended Standards**

Signal Standard (IOSTANDARD) and Current Drive Attribute (mA)		Test Conditions		Logic Level Characteristics	
		I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
GTL		32	–	0.4	–
GTL_DCI		Note 3	Note 3		
GTLP		36	–	0.6	–
GTLP_DCI		Note 3	Note 3		
HSLVDCI_15		Note 3	Note 3	0.4	V_{CCO} – 0.4
HSLVDCI_18					
HSLVDCI_25					
HSLVDCI_33					
HSTL_I		8	–8	0.4	V_{CCO} – 0.4
HSTL_I_DCI		Note 3	Note 3		
HSTL_III		24	–8	0.4	V_{CCO} – 0.4
HSTL_III_DCI		Note 3	Note 3		
HSTL_I_18		8	–8	0.4	V_{CCO} – 0.4
HSTL_I_DCI_18		Note 3	Note 3		
HSTL_II_18		16	–16	0.4	V_{CCO} – 0.4
HSTL_II_DCI_18		Note 3	Note 3		
HSTL_III_18		24	–8	0.4	V_{CCO} – 0.4
HSTL_III_DCI_18		Note 3	Note 3		
LVCMOS12(4)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
LVCMOS15(4)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
LVDCI_15, LVDCI_DV2_15		Note 3	Note 3		
LVCMOS18(4)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
LVDCI_18, LVDCI_DV2_18		Note 3	Note 3		
LVCMOS25(4,5)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24	24	–24		
LVDCI_25, LVDCI_DV2_25		Note 3	Note 3		

Phase Shifter (PS)

Phase shifter operation is only supported if the DLL is in low-frequency mode, see Table 58. Fixed phase shift requires ISE software version 10.1.03 (or later).

Table 62: **Recommended Operating Conditions for the PS in Variable Phase Mode**

Symbol	Description	Frequency Mode/ F_{CLKIN} Range		Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Operating Frequency Ranges								
PSCLK_FREQ (F_{PSCLK})	Frequency for the PSCLK input	Low		1	167	1	167	MHz
Input Pulse Requirements								
PSCLK_PULSE	PSCLK pulse width as a percentage of the PSCLK period	Low	$F_{CLKIN} \leq 100$ MHz	40%	60%	40%	60%	-
			$F_{CLKIN} > 100$ MHz	45%	55%	45%	55%	-

Table 63: **Switching Characteristics for the PS in Variable or Fixed Phase Shift Mode**

Symbol	Description	Frequency Mode/ F_{CLKIN} Range	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Phase Shifting Range							
FINE_SHIFT_RANGE	Phase shift range	Low	–	10.0	–	10.0	ns
Lock Time							
LOCK_DLL_PS	When using the PS in conjunction with the DLL: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase.	18 MHz $\leq F_{CLKIN} \leq$ 30 MHz	–	3.28	–	3.28	ms
		30 MHz $< F_{CLKIN} \leq$ 40 MHz	–	2.56	–	2.56	ms
		40 MHz $< F_{CLKIN} \leq$ 50 MHz	–	1.60	–	1.60	ms
		50 MHz $< F_{CLKIN} \leq$ 60 MHz	–	1.00	–	1.00	ms
		60 MHz $< F_{CLKIN} \leq$ 165 MHz	–	0.88	–	0.88	ms
LOCK_DLL_PS_FX	When using the PS in conjunction with the DLL and DFS: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase.	Low	–	10.40	–	10.40	ms

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32 and Table 62.
2. The PS specifications in this table apply when the PS attribute CLKOUT_PHASE_SHIFT= VARIABLE or FIXED.

Miscellaneous DCM Timing

Table 64: **Miscellaneous DCM Timing**

Symbol	Description	DLL Frequency Mode	Temperature Range		Units
			Commercial	Industrial	
DCM_INPUT_CLOCK_STOP	Maximum duration that the CLKIN and CLKFB signals can be stopped(1,2)	Any	100	100	ms
DCM_RST_PW_MIN	Minimum duration of a RST pulse width	Any	3	3	CLKIN cycles
DCM_RST_PW_MAX(3)	Maximum duration of a RST pulse width(1,2)	Low	N/A	N/A	seconds
		High	N/A	10	seconds
DCM_CONFIG_LAG_TIME(4)	Maximum duration from V_{CCINT} applied to FPGA configuration successfully completed (DONE pin goes High) and clocks applied to DCM DLL(1,2)	Low	N/A	N/A	minutes
		High	N/A	10	minutes

Notes:

1. These limits only apply to applications that use the DCM DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV). The DCM DFS outputs (CLKFX, CLKFX180) are unaffected. Required due to effects of device cooling: see “Momentarily Stopping CLKIN” in Chapter 3 of UG331.
2. Industrial-temperature applications that use the DLL in High-Frequency mode must use a continuous or increasing operating frequency. The DLL under these conditions does not support reducing the operating frequency once establishing an initial operating frequency.
3. This specification is equivalent to the Virtex-4 FPGA DCM_RESET specification.
4. This specification is equivalent to the Virtex-4 FPGA TCONFIG specification.

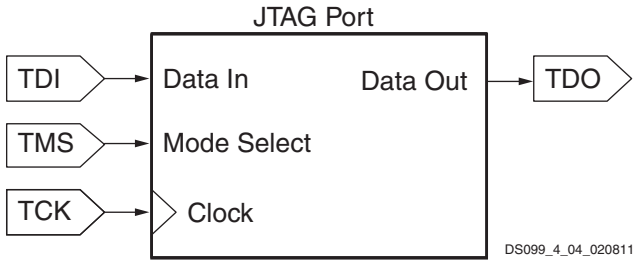

Figure 43: **JTAG Port**

IDCODE Register

Spartan-3 FPGAs contain a 32-bit identification register called the IDCODE register, as defined in the IEEE 1149.1 JTAG standard. The fixed value electrically identifies the manufacture (Xilinx) and the type of device being addressed over a JTAG chain. This register allows the JTAG host to identify the device being tested or programmed via JTAG. See Table 78.

Using JTAG Port After Configuration

The JTAG port is always active and available before, during, and after FPGA configuration. Add the BSCAN_SPARTAN3 primitive to the design to create user-defined JTAG instructions and JTAG chains to communicate with internal logic.

Furthermore, the contents of the User ID register within the JTAG port can be specified as a Bitstream Generation option. By default, the 32-bit User ID register contains `0xFFFFFFFF`.

Table 78: **Spartan-3 JTAG IDCODE Register Values (hexadecimal)**

Part Number	IDCODE Register
XC3S50	0x0140C093
XC3S200	0x01414093
XC3S400	0x0141C093
XC3S1000	0x01428093
XC3S1500	0x01434093
XC3S2000	0x01440093
XC3S4000	0x01448093
XC3S5000	0x01450093

Precautions When Using the JTAG Port in 3.3V Environments

The JTAG port is powered by the +2.5V VCCAUX power supply. When connecting to a 3.3V interface, the JTAG input pins must be current-limited using a series resistor. Similarly, the TDO pin is a CMOS output powered from +2.5V. The TDO output can directly drive a 3.3V input but with reduced noise immunity. See 3.3V-Tolerant Configuration Interface, page 47. See also XAPP453: *The 3.3V Configuration of Spartan-3 FPGAs* for additional details.

The following interface precautions are recommended when connecting the JTAG port to a 3.3V interface.

- Avoid actively driving the JTAG input signals High with 3.3V signal levels. If required in the application, use series current-limiting resistors to keep the current below 10 mA per pin.
- If possible, drive the FPGA JTAG inputs with drivers that can be placed in high-impedance (Hi-Z) after using the JTAG port. Alternatively, drive the FPGA JTAG inputs with open-drain outputs, which only drive Low. In both cases, pull-up resistors are required. The FPGA JTAG pins have pull-up resistors to VCCAUX before configuration and optional pull-up resistors after configuration, controlled by Bitstream Options, page 125.

Table 87: **VQ100 Package Pinout *(Cont'd)***

Bank	XC3S50 XC3S200 Pin Name	VQ100 Pin Number	Type
6	IO_L40P_6/VREF_6	P13	VREF
6	VCCO_6	P19	VCCO
7	IO_L01N_7/VRP_7	P2	DCI
7	IO_L01P_7/VRN_7	P1	DCI
7	IO_L21N_7	P5	I/O
7	IO_L21P_7	P4	I/O
7	IO_L23N_7	P9	I/O
7	IO_L23P_7	P8	I/O
7	IO_L40N_7/VREF_7	P12	VREF
7	IO_L40P_7	P11	I/O
7	VCCO_7	P6	VCCO
N/A	GND	P3	GND
N/A	GND	P10	GND
N/A	GND	P20	GND
N/A	GND	P29	GND
N/A	GND	P41	GND
N/A	GND	P56	GND
N/A	GND	P66	GND
N/A	GND	P73	GND
N/A	GND	P82	GND
N/A	GND	P95	GND
N/A	VCCAUX	P7	VCCAUX
N/A	VCCAUX	P33	VCCAUX
N/A	VCCAUX	P58	VCCAUX
N/A	VCCAUX	P84	VCCAUX
N/A	VCCINT	P18	VCCINT
N/A	VCCINT	P45	VCCINT
N/A	VCCINT	P69	VCCINT
N/A	VCCINT	P93	VCCINT
VCCAUX	CCLK	P52	CONFIG
VCCAUX	DONE	P51	CONFIG
VCCAUX	HSWAP_EN	P98	CONFIG
VCCAUX	M0	P25	CONFIG
VCCAUX	M1	P24	CONFIG
VCCAUX	M2	P26	CONFIG
VCCAUX	PROG_B	P99	CONFIG
VCCAUX	TCK	P77	JTAG
VCCAUX	TDI	P100	JTAG

CP132: 132-Ball Chip-Scale Package

Note: The CP132 and CPG132 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.

The pinout and footprint for the XC3S50 in the 132-ball chip-scale package, CP132, appear in Table 89 and Figure 45.

All the package pins appear in Table 89 and are sorted by bank number, then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The CP132 footprint has eight I/O banks. However, the voltage supplies for the two I/O banks along an edge are connected together internally. Consequently, there are four output voltage supplies, labeled VCCO_TOP, VCCO_RIGHT, VCCO_BOTTOM, and VCCO_LEFT.

Pinout Table

Table 89: **CP132 Package Pinout**

Bank	XC3S50 Pin Name	CP132 Ball	Type
0	IO_L01N_0/VRP_0	A3	DCI
0	IO_L01P_0/VRN_0	C4	DCI
0	IO_L27N_0	C5	I/O
0	IO_L27P_0	B5	I/O
0	IO_L30N_0	B6	I/O
0	IO_L30P_0	A6	I/O
0	IO_L31N_0	C7	I/O
0	IO_L31P_0/VREF_0	B7	VREF
0	IO_L32N_0/GCLK7	A7	GCLK
0	IO_L32P_0/GCLK6	C8	GCLK
1	IO_L01N_1/VRP_1	A13	DCI
1	IO_L01P_1/VRN_1	B13	DCI
1	IO_L27N_1	C11	I/O
1	IO_L27P_1	A12	I/O
1	IO_L28N_1	A11	I/O
1	IO_L28P_1	B11	I/O
1	IO_L31N_1/VREF_1	C9	VREF
1	IO_L31P_1	A10	I/O
1	IO_L32N_1/GCLK5	A8	GCLK
1	IO_L32P_1/GCLK4	A9	GCLK
2	IO_L01N_2/VRP_2	D12	DCI
2	IO_L01P_2/VRN_2	C14	DCI
2	IO_L20N_2	E12	I/O
2	IO_L20P_2	E13	I/O
2	IO_L21N_2	E14	I/O
2	IO_L21P_2	F12	I/O
2	IO_L23N_2/VREF_2	F13	VREF
2	IO_L23P_2	F14	I/O
2	IO_L24N_2	G12	I/O

CP132 Footprint

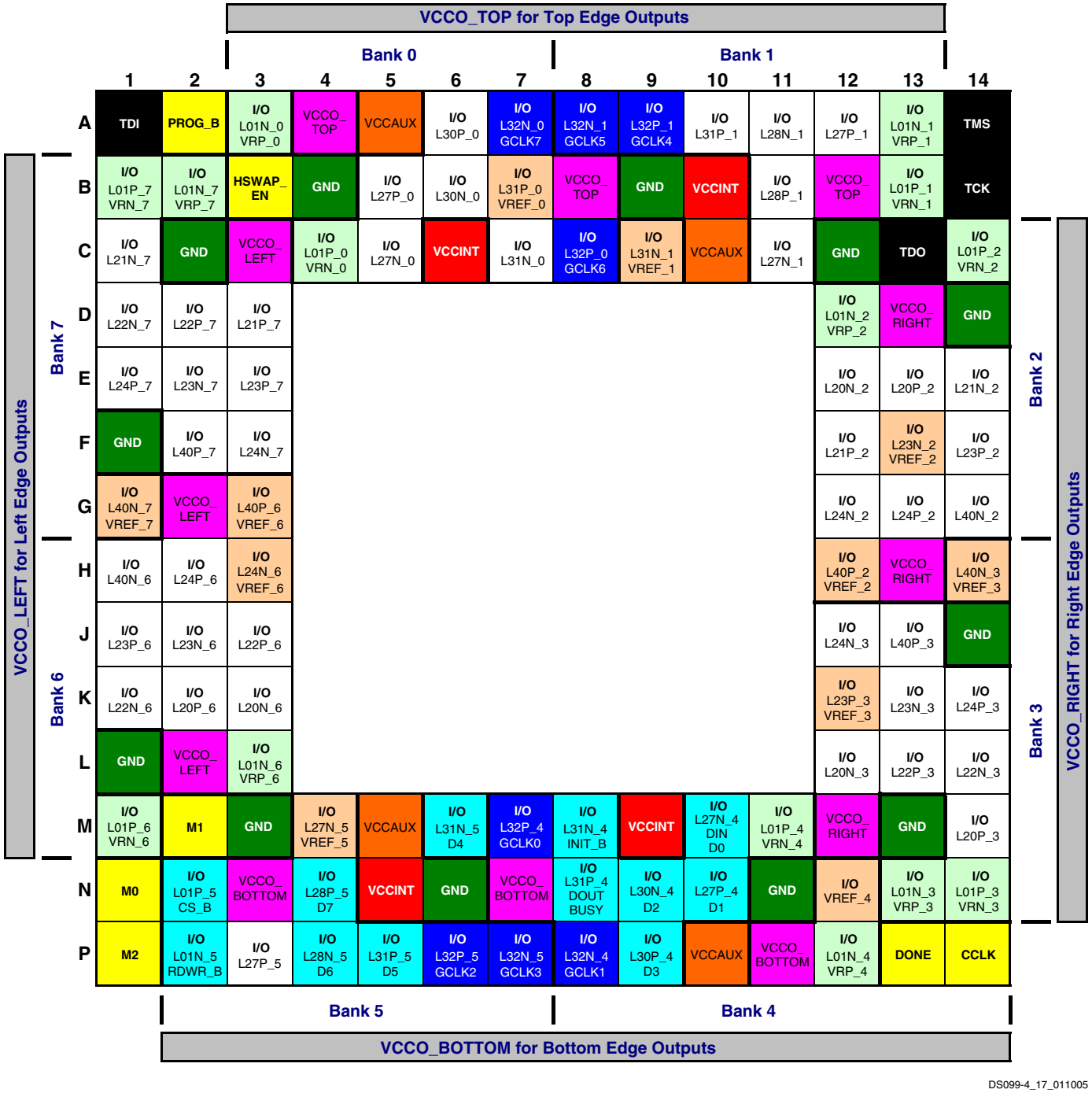

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Figure 45: **CP132 Package Footprint (Top View). Note pin 1 indicator in top-left corner and logo orientation.**

44	**I/O:** Unrestricted, general-purpose user I/O	12	**DUAL:** Configuration pin, then possible user I/O	11	**VREF:** User I/O or input voltage reference for bank
14	**DCI:** User I/O or reference resistor input for bank	8	**GCLK:** User I/O, input, or global buffer input	12	**VCCO:** Output voltage supply for bank
7	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	4	**VCCINT:** Internal core voltage supply (+1.2V)
0	**N.C.:** No unconnected pins in this package	12	**GND:** Ground	4	**VCCAUX:** Auxiliary voltage supply (+2.5V)

Table 91: **TQ144 Package Pinout *(Cont'd)***

Bank	XC3S50, XC3S200, XC3S400 Pin Name	TQ144 Pin Number	Type
6,7	VCCO_LEFT	P34	VCCO
6,7	VCCO_LEFT	P3	VCCO
N/A	GND	P136	GND
N/A	GND	P139	GND
N/A	GND	P114	GND
N/A	GND	P117	GND
N/A	GND	P94	GND
N/A	GND	P101	GND
N/A	GND	P81	GND
N/A	GND	P88	GND
N/A	GND	P64	GND
N/A	GND	P67	GND
N/A	GND	P42	GND
N/A	GND	P45	GND
N/A	GND	P22	GND
N/A	GND	P29	GND
N/A	GND	P9	GND
N/A	GND	P16	GND
N/A	VCCAUX	P134	VCCAUX
N/A	VCCAUX	P120	VCCAUX
N/A	VCCAUX	P62	VCCAUX
N/A	VCCAUX	P48	VCCAUX
N/A	VCCINT	P133	VCCINT
N/A	VCCINT	P121	VCCINT
N/A	VCCINT	P61	VCCINT
N/A	VCCINT	P49	VCCINT
VCCAUX	CCLK	P72	CONFIG
VCCAUX	DONE	P71	CONFIG
VCCAUX	HSWAP_EN	P142	CONFIG
VCCAUX	M0	P38	CONFIG
VCCAUX	M1	P37	CONFIG
VCCAUX	M2	P39	CONFIG
VCCAUX	PROG_B	P143	CONFIG
VCCAUX	TCK	P110	JTAG
VCCAUX	TDI	P144	JTAG
VCCAUX	TDO	P109	JTAG
VCCAUX	TMS	P111	JTAG

Table 96: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S200, XC3S400, XC3S1000 Pin Name	FT256 Pin Number	Type
2	VCCO_2	G11	VCCO
2	VCCO_2	H11	VCCO
2	VCCO_2	H12	VCCO
3	IO	K15	I/O
3	IO_L01N_3/VRP_3	P16	DCI
3	IO_L01P_3/VRN_3	R16	DCI
3	IO_L16N_3	P15	I/O
3	IO_L16P_3	P14	I/O
3	IO_L17N_3	N16	I/O
3	IO_L17P_3/VREF_3	N15	VREF
3	IO_L19N_3	M14	I/O
3	IO_L19P_3	N14	I/O
3	IO_L20N_3	M16	I/O
3	IO_L20P_3	M15	I/O
3	IO_L21N_3	L13	I/O
3	IO_L21P_3	M13	I/O
3	IO_L22N_3	L15	I/O
3	IO_L22P_3	L14	I/O
3	IO_L23N_3	K12	I/O
3	IO_L23P_3/VREF_3	L12	VREF
3	IO_L24N_3	K14	I/O
3	IO_L24P_3	K13	I/O
3	IO_L39N_3	J14	I/O
3	IO_L39P_3	J13	I/O
3	IO_L40N_3/VREF_3	J16	VREF
3	IO_L40P_3	K16	I/O
3	VCCO_3	J11	VCCO
3	VCCO_3	J12	VCCO
3	VCCO_3	K11	VCCO
4	IO	T12	I/O
4	IO	T14	I/O
4	IO/VREF_4	N12	VREF
4	IO/VREF_4	P13	VREF
4	IO/VREF_4	T10	VREF
4	IO_L01N_4/VRP_4	R13	DCI
4	IO_L01P_4/VRN_4	T13	DCI
4	IO_L25N_4	P12	I/O
4	IO_L25P_4	R12	I/O
4	IO_L27N_4/DIN/D0	M11	DUAL
4	IO_L27P_4/D1	N11	DUAL

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
2	IO_L20N_2	E17	I/O
2	IO_L20P_2	E18	I/O
2	IO_L21N_2	F15	I/O
2	IO_L21P_2	E15	I/O
2	IO_L22N_2	F14	I/O
2	IO_L22P_2	G14	I/O
2	IO_L23N_2/VREF_2	G18	VREF
2	IO_L23P_2	F17	I/O
2	IO_L24N_2	G15	I/O
2	IO_L24P_2	G16	I/O
2	IO_L27N_2	H13	I/O
2	IO_L27P_2	H14	I/O
2	IO_L34N_2/VREF_2	H16	VREF
2	IO_L34P_2	H15	I/O
2	IO_L35N_2	H17	I/O
2	IO_L35P_2	H18	I/O
2	IO_L39N_2	J18	I/O
2	IO_L39P_2	J17	I/O
2	IO_L40N_2	J15	I/O
2	IO_L40P_2/VREF_2	J14	VREF
2	VCCO_2	F16	VCCO
2	VCCO_2	H12	VCCO
2	VCCO_2	J12	VCCO
3	IO	K15	I/O
3	IO_L01N_3/VRP_3	T17	DCI
3	IO_L01P_3/VRN_3	T16	DCI
3	IO_L16N_3	T18	I/O
3	IO_L16P_3	U18	I/O
3	IO_L17N_3	P16	I/O
3	IO_L17P_3/VREF_3	R16	VREF
3	IO_L19N_3	R17	I/O
3	IO_L19P_3	R18	I/O
3	IO_L20N_3	P18	I/O
3	IO_L20P_3	P17	I/O
3	IO_L21N_3	P15	I/O
3	IO_L21P_3	N15	I/O
3	IO_L22N_3	M14	I/O
3	IO_L22P_3	N14	I/O
3	IO_L23N_3	M15	I/O
3	IO_L23P_3/VREF_3	M16	VREF

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
7	IO_L20P_7	E1	I/O
7	IO_L21N_7	E4	I/O
7	IO_L21P_7	F4	I/O
7	IO_L22N_7	G5	I/O
7	IO_L22P_7	F5	I/O
7	IO_L23N_7	G1	I/O
7	IO_L23P_7	F2	I/O
7	IO_L24N_7	G4	I/O
7	IO_L24P_7	G3	I/O
7	IO_L27N_7	H5	I/O
7	IO_L27P_7/VREF_7	H6	VREF
7	IO_L34N_7	H4	I/O
7	IO_L34P_7	H3	I/O
7	IO_L35N_7	H1	I/O
7	IO_L35P_7	H2	I/O
7	IO_L39N_7	J1	I/O
7	IO_L39P_7	J2	I/O
7	IO_L40N_7/VREF_7	J5	VREF
7	IO_L40P_7	J4	I/O
7	VCCO_7	F3	VCCO
7	VCCO_7	H7	VCCO
7	VCCO_7	J7	VCCO
N/A	GND	A1	GND
N/A	GND	A13	GND
N/A	GND	A18	GND
N/A	GND	A6	GND
N/A	GND	B17	GND
N/A	GND	B2	GND
N/A	GND	C10	GND
N/A	GND	C9	GND
N/A	GND	F1	GND
N/A	GND	F18	GND
N/A	GND	G12	GND
N/A	GND	G7	GND
N/A	GND	H10	GND
N/A	GND	H11	GND
N/A	GND	H8	GND
N/A	GND	H9	GND
N/A	GND	J11	GND
N/A	GND	J16	GND

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
1	N.C. (◆)	IO_L18P_1	IO_L18P_1	IO_L18P_1	IO[3]	C18	I/O
1	IO_L19N_1	IO_L19N_1	IO_L19N_1	IO_L19N_1	IO_L19N_1	F17	I/O
1	IO_L19P_1	IO_L19P_1	IO_L19P_1	IO_L19P_1	IO_L19P_1	G17	I/O
1	IO_L22N_1	IO_L22N_1	IO_L22N_1	IO_L22N_1	IO_L22N_1	D17	I/O
1	IO_L22P_1	IO_L22P_1	IO_L22P_1	IO_L22P_1	IO_L22P_1	E17	I/O
1	N.C. (◆)	IO_L23N_1	IO_L23N_1	IO_L23N_1	IO_L23N_1	A17	I/O
1	N.C. (◆)	IO_L23P_1	IO_L23P_1	IO_L23P_1	IO_L23P_1	B17	I/O
1	IO_L24N_1	IO_L24N_1	IO_L24N_1	IO_L24N_1	IO_L24N_1	G16	I/O
1	IO_L24P_1	IO_L24P_1	IO_L24P_1	IO_L24P_1	IO_L24P_1	H16	I/O
1	IO_L25N_1	IO_L25N_1	IO_L25N_1	IO_L25N_1	IO_L25N_1	E16	I/O
1	IO_L25P_1	IO_L25P_1	IO_L25P_1	IO_L25P_1	IO_L25P_1	F16	I/O
1	N.C. (◆)	IO_L26N_1	IO_L26N_1	IO_L26N_1	IO_L26N_1	A16	I/O
1	N.C. (◆)	IO_L26P_1	IO_L26P_1	IO_L26P_1	IO_L26P_1	B16	I/O
1	IO_L27N_1	IO_L27N_1	IO_L27N_1	IO_L27N_1	IO_L27N_1	G15	I/O
1	IO_L27P_1	IO_L27P_1	IO_L27P_1	IO_L27P_1	IO_L27P_1	H15	I/O
1	IO_L28N_1	IO_L28N_1	IO_L28N_1	IO_L28N_1	IO_L28N_1	E15	I/O
1	IO_L28P_1	IO_L28P_1	IO_L28P_1	IO_L28P_1	IO_L28P_1	F15	I/O
1	IO_L29N_1	IO_L29N_1	IO_L29N_1	IO_L29N_1	IO_L29N_1	A15	I/O
1	IO_L29P_1	IO_L29P_1	IO_L29P_1	IO_L29P_1	IO_L29P_1	B15	I/O
1	IO_L30N_1	IO_L30N_1	IO_L30N_1	IO_L30N_1	IO_L30N_1	G14	I/O
1	IO_L30P_1	IO_L30P_1	IO_L30P_1	IO_L30P_1	IO_L30P_1	H14	I/O
1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	D14	VREF
1	IO_L31P_1	IO_L31P_1	IO_L31P_1	IO_L31P_1	IO_L31P_1	E14	I/O
1	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	B14	GCLK
1	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	C14	GCLK
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	C16	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	C20	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	H17	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	H18	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	J14	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	J15	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	J16	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	K14	VCCO
2	N.C. (◆)	N.C. (■)	IO	IO	IO	F22	I/O
2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	C25	DCI
2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	C26	DCI
2	IO_L02N_2	IO_L02N_2	IO_L02N_2	IO_L02N_2	IO_L02N_2	E23	I/O
2	IO_L02P_2	IO_L02P_2	IO_L02P_2	IO_L02P_2	IO_L02P_2	E24	I/O
2	IO_L03N_2/VREF_2	IO_L03N_2/VREF_2[1]	IO_L03N_2/VREF_2	IO_L03N_2/VREF_2	IO_L03N_2/VREF_2	D25	VREF[1]
2	IO_L03P_2	IO_L03P_2	IO_L03P_2	IO_L03P_2	IO_L03P_2	D26	I/O
2	N.C. (◆)	IO_L05N_2	IO_L05N_2	IO_L05N_2	IO_L05N_2	E25	I/O
2	N.C. (◆)	IO_L05P_2	IO_L05P_2	IO_L05P_2	IO_L05P_2	E26	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
3	IO_L48P_3	IO_L48P_3	AB24	I/O
3	N.C. (◆)	IO_L49N_3	AA26	I/O
3	N.C. (◆)	IO_L49P_3	AA25	I/O
3	IO_L50N_3	IO_L50N_3	Y25	I/O
3	IO_L50P_3	IO_L50P_3	Y24	I/O
3	N.C. (◆)	IO_L51N_3	V24	I/O
3	N.C. (◆)	IO_L51P_3	W24	I/O
3	VCCO_3	VCCO_3	AA23	VCCO
3	VCCO_3	VCCO_3	AB23	VCCO
3	VCCO_3	VCCO_3	AB29	VCCO
3	VCCO_3	VCCO_3	AB33	VCCO
3	VCCO_3	VCCO_3	AD27	VCCO
3	VCCO_3	VCCO_3	AD31	VCCO
3	VCCO_3	VCCO_3	AG28	VCCO
3	VCCO_3	VCCO_3	AG32	VCCO
3	VCCO_3	VCCO_3	AL32	VCCO
3	VCCO_3	VCCO_3	W23	VCCO
3	VCCO_3	VCCO_3	W31	VCCO
3	VCCO_3	VCCO_3	Y23	VCCO
3	VCCO_3	VCCO_3	Y27	VCCO
4	IO	IO	AD18	I/O
4	IO	IO	AD19	I/O
4	IO	IO	AD20	I/O
4	IO	IO	AD22	I/O
4	IO	IO	AE18	I/O
4	IO	IO	AE19	I/O
4	IO	IO	AE22	I/O
4	N.C. (◆)	IO	AE24	I/O
4	IO	IO	AF24	I/O
4	N.C. (◆)	IO	AF26	I/O
4	IO	IO	AG26	I/O
4	IO	IO	AG27	I/O
4	IO	IO	AJ27	I/O
4	IO	IO	AJ29	I/O
4	IO	IO	AK25	I/O
4	IO	IO	AN26	I/O
4	IO/VREF_4	IO/VREF_4	AF21	VREF
4	IO/VREF_4	IO/VREF_4	AH23	VREF
4	IO/VREF_4	IO/VREF_4	AK18	VREF
4	IO/VREF_4	IO/VREF_4	AL30	VREF

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
4	IO_L01N_4/VRP_4	IO_L01N_4/VRP_4	AN32	DCI
4	IO_L01P_4/VRN_4	IO_L01P_4/VRN_4	AP32	DCI
4	IO_L02N_4	IO_L02N_4	AN31	I/O
4	IO_L02P_4	IO_L02P_4	AP31	I/O
4	IO_L03N_4	IO_L03N_4	AM30	I/O
4	IO_L03P_4	IO_L03P_4	AN30	I/O
4	IO_L04N_4	IO_L04N_4	AN27	I/O
4	IO_L04P_4	IO_L04P_4	AP27	I/O
4	IO_L05N_4	IO_L05N_4	AH26	I/O
4	IO_L05P_4	IO_L05P_4	AJ26	I/O
4	IO_L06N_4/VREF_4	IO_L06N_4/VREF_4	AL26	VREF
4	IO_L06P_4	IO_L06P_4	AM26	I/O
4	IO_L07N_4	IO_L07N_4	AF25	I/O
4	IO_L07P_4	IO_L07P_4	AG25	I/O
4	IO_L08N_4	IO_L08N_4	AH25	I/O
4	IO_L08P_4	IO_L08P_4	AJ25	I/O
4	IO_L09N_4	IO_L09N_4	AL25	I/O
4	IO_L09P_4	IO_L09P_4	AM25	I/O
4	IO_L10N_4	IO_L10N_4	AN25	I/O
4	IO_L10P_4	IO_L10P_4	AP25	I/O
4	IO_L11N_4	IO_L11N_4	AD23	I/O
4	IO_L11P_4	IO_L11P_4	AE23	I/O
4	IO_L12N_4	IO_L12N_4	AF23	I/O
4	IO_L12P_4	IO_L12P_4	AG23	I/O
4	IO_L13N_4	IO_L13N_4	AJ23	I/O
4	IO_L13P_4	IO_L13P_4	AK23	I/O
4	IO_L14N_4	IO_L14N_4	AL23	I/O
4	IO_L14P_4	IO_L14P_4	AM23	I/O
4	IO_L15N_4	IO_L15N_4	AN23	I/O
4	IO_L15P_4	IO_L15P_4	AP23	I/O
4	IO_L16N_4	IO_L16N_4	AG22	I/O
4	IO_L16P_4	IO_L16P_4	AH22	I/O
4	IO_L17N_4	IO_L17N_4	AL22	I/O
4	IO_L17P_4	IO_L17P_4	AM22	I/O
4	IO_L18N_4	IO_L18N_4	AD21	I/O
4	IO_L18P_4	IO_L18P_4	AE21	I/O
4	IO_L19N_4	IO_L19N_4	AG21	I/O
4	IO_L19P_4	IO_L19P_4	AH21	I/O
4	IO_L20N_4	IO_L20N_4	AJ21	I/O
4	IO_L20P_4	IO_L20P_4	AK21	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
N/A	GND	GND	AA18	GND
N/A	GND	GND	AA19	GND
N/A	GND	GND	AA20	GND
N/A	GND	GND	AA21	GND
N/A	GND	GND	AB1	GND
N/A	GND	GND	AB17	GND
N/A	GND	GND	AB18	GND
N/A	GND	GND	AB26	GND
N/A	GND	GND	AB30	GND
N/A	GND	GND	AB34	GND
N/A	GND	GND	AB5	GND
N/A	GND	GND	AB9	GND
N/A	GND	GND	AD3	GND
N/A	GND	GND	AD32	GND
N/A	GND	GND	AE10	GND
N/A	GND	GND	AE25	GND
N/A	GND	GND	AF1	GND
N/A	GND	GND	AF13	GND
N/A	GND	GND	AF16	GND
N/A	GND	GND	AF19	GND
N/A	GND	GND	AF22	GND
N/A	GND	GND	AF30	GND
N/A	GND	GND	AF34	GND
N/A	GND	GND	AF5	GND
N/A	GND	GND	AH28	GND
N/A	GND	GND	AH7	GND
N/A	GND	GND	AK1	GND
N/A	GND	GND	AK13	GND
N/A	GND	GND	AK16	GND
N/A	GND	GND	AK19	GND
N/A	GND	GND	AK22	GND
N/A	GND	GND	AK26	GND
N/A	GND	GND	AK30	GND
N/A	GND	GND	AK34	GND
N/A	GND	GND	AK5	GND
N/A	GND	GND	AK9	GND
N/A	GND	GND	AM11	GND
N/A	GND	GND	AM24	GND
N/A	GND	GND	AM3	GND
N/A	GND	GND	AM32	GND

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
N/A	GND	GND	T21	GND
N/A	GND	GND	T26	GND
N/A	GND	GND	T30	GND
N/A	GND	GND	T34	GND
N/A	GND	GND	T5	GND
N/A	GND	GND	T9	GND
N/A	GND	GND	U13	GND
N/A	GND	GND	U14	GND
N/A	GND	GND	U15	GND
N/A	GND	GND	U16	GND
N/A	GND	GND	U17	GND
N/A	GND	GND	U18	GND
N/A	GND	GND	U19	GND
N/A	GND	GND	U20	GND
N/A	GND	GND	U21	GND
N/A	GND	GND	U22	GND
N/A	GND	GND	V13	GND
N/A	GND	GND	V14	GND
N/A	GND	GND	V15	GND
N/A	GND	GND	V16	GND
N/A	GND	GND	V17	GND
N/A	GND	GND	V18	GND
N/A	GND	GND	V19	GND
N/A	GND	GND	V20	GND
N/A	GND	GND	V21	GND
N/A	GND	GND	V22	GND
N/A	GND	GND	W1	GND
N/A	GND	GND	W14	GND
N/A	GND	GND	W15	GND
N/A	GND	GND	W16	GND
N/A	GND	GND	W17	GND
N/A	GND	GND	W18	GND
N/A	GND	GND	W19	GND
N/A	GND	GND	W20	GND
N/A	GND	GND	W21	GND
N/A	GND	GND	W26	GND
N/A	GND	GND	W30	GND
N/A	GND	GND	W34	GND
N/A	GND	GND	W5	GND
N/A	GND	GND	W9	GND

All Devices

Top Right Corner of FG1156 Package (Top View)

12	**DUAL:** Configuration pin, then possible user I/O	16	**DCI:** User I/O or reference resistor input for bank	8	**GCLK:** User I/O or global clock buffer input
7	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	104	**VCCO:** Output voltage supply for bank
40	**VCCINT:** Internal core voltage supply (+1.2V)	32	**VCCAUX:** Auxiliary voltage supply (+2.5V)	184	**GND:** Ground

Bank 1

18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	
I/O	GND	I/O L40N_1	I/O L26N_1	GND	I/O L19N_1	I/O L15N_1	I/O L14N_1	GND	I/O L08N_1	I/O L34N_1 ◆	I/O L05N_1	GND	I/O L02N_1	I/O L01N_1 VRP_1	GND	GND	A
I/O L32N_1 GCLK5	I/O L28N_1	I/O L40P_1	I/O L26P_1	VCCO_1	I/O L19P_1	I/O L15P_1	I/O L14P_1	I/O	I/O L08P_1	I/O L34P_1 ◆	I/O L05P_1	I/O L03N_1	I/O L02P_1	I/O L01P_1 VRN_1	GND	GND	B
I/O L32P_1 GCLK4	I/O L28P_1	I/O L39N_1	I/O L25N_1	I/O L22N_1	I/O	GND	I/O L13N_1	I/O L10N_1 VREF_1	VCCO_1	I/O L33N_1 ◆	I/O L04N_1	I/O L03P_1	VCCO_1	GND	I/O L01N_2 VRP_2	I/O L01P_2 VRN_2	C
I/O L31N_1 VREF_1	VCCO_1	I/O L39P_1	I/O L25P_1	I/O L22P_1	I/O L18N_1	VCCO_1	I/O L13P_1	I/O L10P_1	I/O L07N_1	I/O L33P_1 ◆	I/O L04P_1	IO VREF_1	TCK	VCCO_2	I/O L02N_2	I/O L02P_2	D
I/O L31P_1	GND	VCCAUX	I/O	GND	I/O L18P_1	VCCAUX	I/O	GND	I/O L07P_1	I/O L06N_1 VREF_1	VCCAUX	GND	TDO	I/O L03N_2 VREF_2	I/O L03P_2	GND	E
I/O	I/O L27N_1	I/O L38N_1	I/O L24N_1	VCCO_1	I/O L17N_1 VREF_1	I/O L36N_1 ◆	I/O L12N_1	I/O L09N_1	I/O	I/O L06P_1	I/O	VCCAUX	I/O L04N_2	I/O L04P_2	I/O L41N_2	I/O L41P_2	F
I/O L30N_1	I/O L27P_1	I/O L38P_1	I/O L24P_1	I/O L21N_1	I/O L17P_1	I/O L36P_1 ◆	I/O L12P_1	I/O L09P_1	VCCO_1	GND	I/O L05N_2	I/O L05P_2	I/O L42N_2 ◆	I/O L42P_2 ◆	I/O	I/O	G
I/O L30P_1	VCCAUX	VCCO_1	I/O L23N_1	I/O L21P_1	I/O	VCCO_1	I/O L11N_1	I/O	TMS	VCCO_2	I/O L06N_2	I/O L06P_2	I/O L09N_2 VREF_2	VCCO_2	I/O L07N_2	I/O L07P_2	H
I/O L29N_1	GND	I/O L37N_1	I/O L23P_1	GND	I/O L16N_1	I/O L35N_1 ◆	I/O L11P_1	I/O ◆	I/O L11N_2	I/O L08N_2	I/O L08P_2	GND	I/O L09P_2	I/O L10N_2	I/O L10P_2	GND	J
I/O L29P_1	I/O	I/O L37P_1	IO VREF_1	I/O L20N_1	I/O L16P_1	I/O L35P_1 ◆	GND	I/O L11P_2	I/O L12N_2	I/O L12P_2	I/O L13N_2	I/O L13P_2 VREF_2	I/O L14N_2	I/O L14P_2	I/O L15N_2	I/O L15P_2	K
IO VREF_1	I/O	I/O	I/O	I/O L20P_1	I/O ◆	I/O	I/O L16N_2	I/O L16P_2	VCCO_2	I/O L17N_2 ◆	I/O L17P_2 VREF_2 ◆	VCCAUX	VCCO_2	GND	I/O L45N_2	I/O L45P_2	L
VCCINT	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCINT	I/O L46N_2	I/O L46P_2	I/O L21N_2	I/O L47N_2	I/O L47P_2	I/O L19N_2	I/O L19P_2	I/O L20N_2	I/O L20P_2	I/O L48N_2	I/O L48P_2	M
GND	VCCINT	VCCINT	VCCINT	VCCINT	VCCO_2	I/O L24N_2	I/O L21P_2	GND	I/O L22N_2	I/O L22P_2	VCCO_2	GND	I/O L23N_2 VREF_2	I/O L23P_2	VCCO_2	GND	N
GND	GND	GND	GND	VCCINT	VCCO_2	I/O L24P_2	I/O L49N_2 ◆	I/O L49P_2 ◆	I/O L50N_2	I/O L50P_2	I/O L26N_2	I/O L26P_2	I/O L27N_2	I/O L27P_2	I/O L28N_2	I/O L28P_2	P
GND	GND	GND	GND	VCCINT	VCCO_2	I/O L29N_2	I/O L29P_2	I/O L33N_2	VCCO_2	I/O L30N_2	I/O L30P_2	VCCAUX	I/O L31N_2	I/O L31P_2	I/O L32N_2	I/O L32P_2	R
GND	GND	GND	GND	VCCINT	VCCO_2	I/O L51N_2 ◆	I/O L33P_2	GND	VCCAUX	I/O L34N_2 VREF_2	I/O L34P_2	GND	VCCO_2	I/O L35N_2	I/O L35P_2	GND	T
GND	GND	GND	GND	GND	VCCINT	I/O L51P_2 ◆	I/O	I/O	I/O L37N_2	I/O L37P_2	I/O L38N_2	I/O L38P_2	I/O L39N_2	I/O L39P_2	I/O L40N_2	I/O L40P_2 VREF_2	U

Bank 2

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Figure 58: FG1156 Package Footprint (Top View) Continued