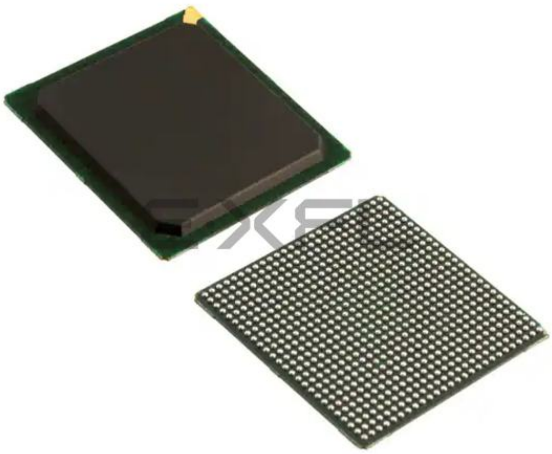

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	6912
Number of Logic Elements/Cells	62208
Total RAM Bits	1769472
Number of I/O	489
Number of Gates	4000000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s4000-4fgg676i

ESD Protection

Clamp diodes protect all device pads against damage from Electro-Static Discharge (ESD) as well as excessive voltage transients. Each I/O has two clamp diodes: One diode extends P-to-N from the pad to V_{CCO} and a second diode extends N-to-P from the pad to GND. During operation, these diodes are normally biased in the off state. These clamp diodes are always connected to the pad, regardless of the signal standard selected. The presence of diodes limits the ability of Spartan-3 FPGA I/Os to tolerate high signal voltages. The V_{IN} absolute maximum rating in Table 28, page 58 specifies the voltage range that I/Os can tolerate.

Slew Rate Control and Drive Strength

Two options, FAST and SLOW, control the output slew rate. The FAST option supports output switching at a high rate. The SLOW option reduces bus transients. These options are only available when using one of the LVCMOS or LVTTL standards, which also provide up to seven different levels of current drive strength: 2, 4, 6, 8, 12, 16, and 24 mA. Choosing the appropriate drive strength level is yet another means to minimize bus transients.

Table 7 shows the drive strengths that the LVCMOS and LVTTL standards support.

Table 7: **Programmable Output Drive Current**

Signal Standard (IOSTANDARD)	Current Drive (mA)						
	2	4	6	8	12	16	24
LVTTL	✓	✓	✓	✓	✓	✓	✓
LVCMOS33	✓	✓	✓	✓	✓	✓	✓
LVCMOS25	✓	✓	✓	✓	✓	✓	✓
LVCMOS18	✓	✓	✓	✓	✓	✓	–
LVCMOS15	✓	✓	✓	✓	✓	–	–
LVCMOS12	✓	✓	✓	–	–	–	–

Boundary-Scan Capability

All Spartan-3 FPGA IOBs support boundary-scan testing compatible with IEEE 1149.1 standards. During boundary- scan operations such as EXTEST and HIGHZ the I/O pull-down resistor is active. For more information, see Boundary-Scan (JTAG) Mode, page 50, and refer to the “Using Boundary-Scan and BSDL Files” chapter in UG331.

SelectIO Interface Signal Standards

The IOBs support 18 different single-ended signal standards, as listed in Table 8. Furthermore, the majority of IOBs can be used in specific pairs supporting any of eight differential signal standards, as shown in Table 9.

To define the SelectIO™ interface signaling standard in a design, set the IOSTANDARD attribute to the appropriate setting. Xilinx provides a variety of different methods for applying the IOSTANDARD for maximum flexibility. For a full description of different methods of applying attributes to control IOSTANDARD, refer to the “Using I/O Resources” chapter in UG331.

Together with placing the appropriate I/O symbol, two externally applied voltage levels, V_{CCO} and V_{REF}, select the desired signal standard. The V_{CCO} lines provide current to the output driver. The voltage on these lines determines the output voltage swing for all standards except GTL and GTLP.

All single-ended standards except the LVCMOS, LVTTL, and PCI varieties require a Reference Voltage (V_{REF}) to bias the input-switching threshold. Once a configuration data file is loaded into the FPGA that calls for the I/Os of a given bank to use such a signal standard, a few specifically reserved I/O pins on the same bank automatically convert to V_{REF} inputs. When using one of the LVCMOS standards, these pins remain I/Os because the V_{CCO} voltage biases the input-switching threshold, so there is no need for V_{REF}. Select the V_{CCO} and V_{REF} levels to suit the desired single-ended standard according to Table 8.

Table 9: **Differential I/O Standards**

Signal Standard (IOSTANDARD)	V_{CCO} (Volts)		V_{REF} for Inputs (Volts)
	For Outputs	For Inputs	
LDT_25 (ULVDS_25)	2.5	–	–
LVDS_25	2.5	–	–
BLVDS_25	2.5	–	–
LVDSEXT_25	2.5	–	–
LVPECL_25	2.5	–	–
RSDS_25	2.5	–	–
DIFF_HSTL_II_18	1.8	–	–
DIFF_SSTL2_II	2.5	–	–

Notes:
1. See Table 10 for a listing of the differential DCI standards.

The need to supply V_{REF} and V_{CCO} imposes constraints on which standards can be used in the same bank. See The Organization of IOBs into Banks section for additional guidelines concerning the use of the V_{CCO} and V_{REF} lines.

Digitally Controlled Impedance (DCI)

When the round-trip delay of an output signal—i.e., from output to input and back again—exceeds rise and fall times, it is common practice to add termination resistors to the line carrying the signal. These resistors effectively match the impedance of a device's I/O to the characteristic impedance of the transmission line, thereby preventing reflections that adversely affect signal integrity. However, with the high I/O counts supported by modern devices, adding resistors requires significantly more components and board area. Furthermore, for some packages—e.g., ball grid arrays—it may not always be possible to place resistors close to pins.

DCI answers these concerns by providing two kinds of on-chip terminations: Parallel terminations make use of an integrated resistor network. Series terminations result from controlling the impedance of output drivers. DCI actively adjusts both parallel and series terminations to accurately match the characteristic impedance of the transmission line. This adjustment process compensates for differences in I/O impedance that can result from normal variation in the ambient temperature, the supply voltage and the manufacturing process. When the output driver turns off, the series termination, by definition, approaches a very high impedance; in contrast, parallel termination resistors remain at the targeted values.

DCI is available only for certain I/O standards, as listed in Table 10. DCI is selected by applying the appropriate I/O standard extensions to symbols or components. There are five basic ways to configure terminations, as shown in Table 11. The DCI I/O standard determines which of these terminations is put into effect.

HSTL_I_DCI-, HSTL_III_DCI-, and SSTL2_I_DCI-type outputs do not require the VRN and VRP reference resistors. Likewise, LVDCI-type inputs do not require the VRN and VRP reference resistors. In a bank without any DCI I/O or a bank containing non-DCI I/O and purely HSTL_I_DCI- or HSTL_III_DCI-type outputs, or SSTL2_I_DCI-type outputs or LVDCI-type inputs, the associated VRN and VRP pins can be used as general-purpose I/O pins.

The HSLVDCI (High-Speed LVDCI) standard is intended for bidirectional use. The driver is identical to LVDCI, while the input is identical to HSTL. By using a V_{REF}-referenced input, HSLVDCI allows greater input sensitivity at the receiver than when using a single-ended LVCMOS-type receiver.

The DLL component has two clock inputs, CLKIN and CLKFB, as well as seven clock outputs, CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV as described in Table 16. The clock outputs drive simultaneously; however, the High Frequency mode only supports a subset of the outputs available in the Low Frequency mode. See DLL Frequency Modes, page 35. Signals that initialize and report the state of the DLL are discussed in The Status Logic Component, page 41.

Table 16: **DLL Signals**

Signal	Direction	Description	Mode Support	
			Low Frequency	High Frequency
CLKIN	Input	Accepts original clock signal.	Yes	Yes
CLKFB	Input	Accepts either CLK0 or CLK2X as feed back signal. (Set CLK_FEEDBACK attribute accordingly).	Yes	Yes
CLK0	Output	Generates clock signal with same frequency and phase as CLKIN.	Yes	Yes
CLK90	Output	Generates clock signal with same frequency as CLKIN, only phase-shifted 90°.	Yes	No
CLK180	Output	Generates clock signal with same frequency as CLKIN, only phase-shifted 180°.	Yes	Yes
CLK270	Output	Generates clock signal with same frequency as CLKIN, only phase-shifted 270°.	Yes	No
CLK2X	Output	Generates clock signal with same phase as CLKIN, only twice the frequency.	Yes	No
CLK2X180	Output	Generates clock signal with twice the frequency of CLKIN, phase-shifted 180° with respect to CLKIN.	Yes	No
CLKDV	Output	Divides the CLKIN frequency by CLKDV_DIVIDE value to generate lower frequency clock signal that is phase-aligned to CLKIN.	Yes	Yes

The clock signal supplied to the CLKIN input serves as a reference waveform, with which the DLL seeks to align the feedback signal at the CLKFB input. When eliminating clock skew, the common approach to using the DLL is as follows: The CLK0 signal is passed through the clock distribution network to all the registers it synchronizes. These registers are either internal or external to the FPGA. After passing through the clock distribution network, the clock signal returns to the DLL via a feedback line called CLKFB. The control block inside the DLL measures the phase error between CLKFB and CLKIN. This phase error is a measure of the clock skew that the clock distribution network introduces. The control block activates the appropriate number of delay elements to cancel out the clock skew. Once the DLL has brought the CLK0 signal in phase with the CLKIN signal, it asserts the LOCKED output, indicating a "lock" on to the CLKIN signal.

DLL Attributes and Related Functions

A number of different functional options can be set for the DLL component through the use of the attributes described in Table 17. Each attribute is described in detail in the sections that follow:

Table 17: **DLL Attributes**

Attribute	Description	Values
CLK_FEEDBACK	Chooses either the CLK0 or CLK2X output to drive the CLKFB input	NONE, 1X, 2X
DLL_FREQUENCY_MODE	Chooses between High Frequency and Low Frequency modes	LOW, HIGH
CLKIN_DIVIDE_BY_2	Halves the frequency of the CLKIN signal just as it enters the DCM	TRUE, FALSE
CLKDV_DIVIDE	Selects constant used to divide the CLKIN input frequency to generate the CLKDV output frequency	1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, 6.0, 6.5, 7.0, 7.5, 8, 9, 10, 11, 12, 13, 14, 15, and 16.
DUTY_CYCLE_CORRECTION	Enables 50% duty cycle correction for the CLK0, CLK90, CLK180, and CLK270 outputs	TRUE, FALSE

Coarse Phase Shift Outputs of the DLL Component

In addition to CLK0 for zero-phase alignment to the CLKIN signal, the DLL also provides the CLK90, CLK180 and CLK270 outputs for 90°, 180° and 270° phase-shifted signals, respectively. These signals are described in Table 16, page 33. Their relative timing in the Low Frequency Mode is shown in Figure 22, page 37. The CLK90, CLK180 and CLK270 outputs are not available when operating in the High Frequency mode. (See the description of the DLL_FREQUENCY_MODE attribute in Table 17, page 33.) For control in finer increments than 90°, see Phase Shifter (PS), page 39.

Basic Frequency Synthesis Outputs of the DLL Component

The DLL component provides basic options for frequency multiplication and division in addition to the more flexible synthesis capability of the DFS component, described in a later section. These operations result in output clock signals with frequencies that are either a fraction (for division) or a multiple (for multiplication) of the incoming clock frequency. The CLK2X output produces an in-phase signal that is twice the frequency of CLKIN. The CLK2X180 output also doubles the frequency, but is 180° out-of-phase with respect to CLKIN. The CLKDIV output generates a clock frequency that is a predetermined fraction of the CLKIN frequency. The CLKDV_DIVIDE attribute determines the factor used to divide the CLKIN frequency. The attribute can be set to various values as described in Table 17. The basic frequency synthesis outputs are described in Table 16. Their relative timing in the Low Frequency Mode is shown in Figure 22.

The CLK2X and CLK2X180 outputs are not available when operating in the High Frequency mode. See the description of the DLL_FREQUENCY_MODE attribute in Table 18.

Duty Cycle Correction of DLL Clock Outputs

The CLK2X[(1)], CLK2X180, and CLKDV[(2)] output signals ordinarily exhibit a 50% duty cycle—even if the incoming CLKIN signal has a different duty cycle. A 50% duty cycle means that the High and Low times of each clock cycle are equal. The DUTY_CYCLE_CORRECTION attribute determines whether or not duty cycle correction is applied to the CLK0, CLK90, CLK180 and CLK270 outputs. If DUTY_CYCLE_CORRECTION is set to TRUE, then the duty cycle of these four outputs is corrected to 50%. If DUTY_CYCLE_CORRECTION is set to FALSE, then these outputs exhibit the same duty cycle as the CLKIN signal. Figure 22 compares the characteristics of the DLL's output signals to those of the CLKIN signal.

1. The CLK2X output generates a 25% duty cycle clock at the same frequency as the CLKIN signal until the DLL has achieved lock.
2. The duty cycle of the CLKDV outputs may differ somewhat from 50% (i.e., the signal will be High for less than 50% of the period) when the CLKDV_DIVIDE attribute is set to a non-integer value *and* the DLL is operating in the High Frequency mode.

Table 22: **Status Logic Signals**

Signal	Direction	Description
RST	Input	A High resets the entire DCM to its initial power-on state. Initializes the DLL taps for a delay of zero. Sets the LOCKED output Low. This input is asynchronous.
STATUS[7:0]	Output	The bit values on the STATUS bus provide information regarding the state of DLL and PS operation
LOCKED	Output	Indicates that the CLKIN and CLKFB signals are in phase by going High. The two signals are out-of-phase when Low.

Table 23: **DCM STATUS Bus**

Bit	Name	Description
0	Phase Shift Overflow	A value of 1 indicates a phase shift overflow when one of two conditions occurs: Incrementing (or decrementing) TPS beyond 255/256 of a CLKIN cycle. The DLL is producing its maximum possible phase shift (i.e., all delay taps are active).(1)
1	CLKIN Input Stopped Toggling	A value of 1 indicates that the CLKIN input signal is not toggling. A value of 0 indicates toggling. This bit functions only when the CLKFB input is connected.(2)
2	CLKFX/CLKFX180 Output Stopped Toggling	A value of 1 indicates that the CLKFX or CLKFX180 output signals are not toggling. A value of 0 indicates toggling. This bit functions only when using the Digital Frequency Synthesizer (DFS).
3:7	Reserved	–

Notes:
1. The DLL phase shift with all delay taps active is specified as the parameter FINE_SHIFT_RANGE.
2. If only the DFS clock outputs are used, but none of the DLL clock outputs, this bit will not go High when the CLKIN signal stops.

Table 24: **Status Attributes**

Attribute	Description	Values
STARTUP_WAIT	Delays transition from configuration to user mode until lock condition is achieved.	TRUE, FALSE

Stabilizing DCM Clocks Before User Mode

It is possible to delay the completion of device configuration until after the DLL has achieved a lock condition using the STARTUP_WAIT attribute described in Table 24. This option ensures that the FPGA does not enter user mode—i.e., begin functional operation—until all system clocks generated by the DCM are stable. In order to achieve the delay, it is necessary to set the attribute to TRUE as well as set the BitGen option LCK_cycle to one of the six cycles making up the Startup phase of configuration. The selected cycle defines the point at which configuration will halt until the LOCKED output goes High.

Global Clock Network

Spartan-3 devices have eight Global Clock inputs called GCLK0 - GCLK7. These inputs provide access to a low-capacitance, low-skew network that is well-suited to carrying high-frequency signals. The Spartan-3 FPGAs clock network is shown in Figure 23. GCLK0 through GCLK3 are located in the center of the bottom edge. GCLK4 through GCLK7 are located in the center of the top edge.

Eight Global Clock Multiplexers (also called BUFGMUX elements) are provided that accept signals from Global Clock inputs and route them to the internal clock network as well as DCMs. Four BUFGMUX elements are located in the center of the bottom edge, just above the GCLK0 - GCLK3 inputs. The remaining four BUFGMUX elements are located in the center of the top edge, just below the GCLK4 - GCLK7 inputs.

Pairs of BUFGMUX elements share global inputs, as shown in Figure 24. For example, the GCLK4 and GCLK5 inputs both potentially connect to BUFGMUX4 and BUFGMUX5 located in the upper right center. A differential clock input uses a pair of GCLK inputs to connect to a single BUFGMUX element.

Table 34: **Quiescent Supply Current Characteristics**

Symbol	Description	Device	Typical(1)	Commercial Maximum(1)	Industrial Maximum(1)	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC3S50	5	24	31	mA
		XC3S200	10	54	80	mA
		XC3S400	15	110	157	mA
		XC3S1000	35	160	262	mA
		XC3S1500	45	260	332	mA
		XC3S2000	60	360	470	mA
		XC3S4000	100	450	810	mA
		XC3S5000	120	600	870	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC3S50	1.5	2.0	2.5	mA
		XC3S200	1.5	3.0	3.5	mA
		XC3S400	1.5	3.0	3.5	mA
		XC3S1000	2.0	4.0	5.0	mA
		XC3S1500	2.5	4.0	5.0	mA
		XC3S2000	3.0	5.0	6.0	mA
		XC3S4000	3.5	5.0	6.0	mA
		XC3S5000	3.5	5.0	6.0	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC3S50	7	20	22	mA
		XC3S200	10	30	33	mA
		XC3S400	15	40	44	mA
		XC3S1000	20	50	55	mA
		XC3S1500	35	75	85	mA
		XC3S2000	45	90	100	mA
		XC3S4000	55	110	125	mA
		XC3S5000	70	130	145	mA

Notes:

1. The numbers in this table are based on the conditions set forth in Table 32. Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. Typical values are characterized using devices with typical processing at room temperature (T_J of 25°C at V_{CCINT} = 1.2V, V_{CCO} = 3.3V, and V_{CCAUX} = 2.5V). Maximum values are the production test limits measured for each device at the maximum specified junction temperature and at maximum voltage limits with V_{CCINT} = 1.26V, V_{CCO} = 3.465V, and V_{CCAUX} = 2.625V. The FPGA is programmed with a "blank" configuration data file (i.e., a design with no functional elements instantiated). For conditions other than those described above, (e.g., a design including functional elements, the use of DCI standards, etc.), measured quiescent current levels may be different than the values in the table. Use the XPower Estimator or XPower Analyzer for more accurate estimates. See Note 2.
2. There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The Spartan-3 XPower Estimator provides quick, approximate, typical estimates, and does not require a netlist of the design. b) XPower Analyzer, part of the Xilinx ISE development software, uses the FPGA netlist as input to provide more accurate maximum and typical estimates.
3. The maximum numbers in this table also indicate the minimum current each power rail requires in order for the FPGA to power-on successfully, once all three rails are supplied. If V_{CCINT} is applied before V_{CCAUX}, there may be temporary additional I_{CCINT} current until V_{CCAUX} is applied. See Surplus I_{CCINT} if V_{CCINT} Applied before V_{CCAUX}, page 54

Table 48: **Test Methods for Timing Measurement at I/Os *(Cont'd)***

Signal Standard (IOSTANDARD)	Inputs			Outputs		Inputs and Outputs
	V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
DIFF_SSTL2_II	-	V_{ICM} – 0.75	V_{ICM} + 0.75	50	1.25	V_{ICM}
DIFF_SSTL2_II_DCI						

Notes:

1. Descriptions of the relevant symbols are as follows:
   VREF – The reference voltage for setting the input switching threshold
   VICM – The common mode input voltage
   VM – Voltage of measurement point on signal transition
   VL – Low-level test voltage at Input pin
   VH – High-level test voltage at Input pin
   RT – Effective termination resistance, which takes on a value of 1MW when no parallel termination is required
   VT – Termination voltage
2. The load capacitance (CL) at the Output pin is 0 pF for all signal standards.
3. According to the PCI specification.

The capacitive load (C_L) is connected between the output and GND. *The Output timing for all standards, as published in the speed files and the data sheet, is always based on a C_L value of zero.* High-impedance probes (less than 1 pF) are used for all measurements. Any delay that the test fixture might contribute to test measurements is subtracted from those measurements to produce the final timing numbers as published in the speed files and data sheet.

Using IBIS Models to Simulate Load Conditions in Application

IBIS Models permit the most accurate prediction of timing delays for a given application. The parameters found in the IBIS model (V_{REF}, R_{REF}, and V_{MEAS}) correspond directly with the parameters used in Table 48, V_T, R_T, and V_M. Do not confuse V_{REF} (the termination voltage) from the IBIS model with V_{REF} (the input-switching threshold) from the table. A fourth parameter, C_{REF}, is always zero. The four parameters describe all relevant output test conditions. IBIS models are found in the Xilinx development software as well as at the following link.

http://www.xilinx.com/support/download/index.htm

Simulate delays for a given application according to its specific load conditions as follows:

1. Simulate the desired signal standard with the output driver connected to the test setup shown in Figure 35. Use parameter values V_T, R_T, and V_M from Table 48. C_{REF} is zero.
2. Record the time to V_M.
3. Simulate the same signal standard with the output driver connected to the PCB trace with load. Use the appropriate IBIS model (including V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} values) or capacitive value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase (or decrease) in delay should be added to (or subtracted from) the appropriate Output standard adjustment (Table 47) to yield the worst-case delay of the PCB trace.

Table 54: **Synchronous 18 x 18 Multiplier Timing**

Symbol	Description	P Outputs	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Clock-to-Output Times							
T_{MULTCK}	When reading from the Multiplier, the time from the active transition at the C clock input to data appearing at the P outputs	P[0]	–	1.00	–	1.15	ns
		P[15]	–	1.15	–	1.32	ns
		P[17]	–	1.30	–	1.50	ns
		P[19]	–	1.45	–	1.67	ns
		P[23]	–	1.76	–	2.02	ns
		P[31]	–	2.37	–	2.72	ns
		P[35]	–	2.67	–	3.07	ns
Setup Times							
$T_{MULIDCK}$	Time from the setup of data at the A and B inputs to the active transition at the C input of the Multiplier	-	1.84	–	2.11	–	ns
Hold Times							
$T_{MULCKID}$	Time from the active transition at the Multiplier's C input to the point where data is last held at the A and B inputs	-	0	–	0	–	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32.

Table 55: **Asynchronous 18 x 18 Multiplier Timing**

Symbol	Description	P Outputs	Speed Grade		Units
			-5	-4	
			Max	Max	
Propagation Times					
T_{MULT}	The time it takes for data to travel from the A and B inputs to the P outputs	P[0]	1.55	1.78	ns
		P[15]	3.15	3.62	ns
		P[17]	3.36	3.86	ns
		P[19]	3.49	4.01	ns
		P[23]	3.73	4.29	ns
		P[31]	4.23	4.86	ns
		P[35]	4.47	5.14	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32.

Table 70: **Spartan-3 FPGA Pin Definitions *(Cont'd)***

Pin Name	Direction	Description
GCLK: Global clock buffer inputs		
IO_Lxxy_#/GCLK0, IO_Lxxy_#/GCLK1, IO_Lxxy_#/GCLK2, IO_Lxxy_#/GCLK3, IO_Lxxy_#/GCLK4, IO_Lxxy_#/GCLK5, IO_Lxxy_#/GCLK6, IO_Lxxy_#/GCLK7	Input if connected to global clock buffers Otherwise, same as I/O	**Global Buffer Input:** Direct input to a low-skew global clock buffer. If not connected to a global clock buffer, this pin is a user I/O.
VREF: I/O bank input reference voltage pins		
IO_Lxxy_#/VREF_# or IO/VREF_#	Voltage supply input when VREF pins are used within a bank. Otherwise, same as I/O	**Input Buffer Reference Voltage for Special I/O Standards (per bank):** If required to support special I/O standards, all the VREF pins within a bank connect to a input threshold voltage source. If not used as input reference voltage pins, these pins are available as individual user-I/O pins.
CONFIG: Dedicated configuration pins (pull-up resistor to VCCAUX always active during configuration, regardless of HSWAP_EN pin)		
CCLK	Input in Slave configuration modes Output in Master configuration modes	**Configuration Clock:** The configuration clock signal synchronizes configuration data. This pin has an internal pull-up resistor to VCCAUX during configuration.
PROG_B	Input	**Program/Configure Device:** Active Low asynchronous reset to configuration logic. Asserting PROG_B Low for an extended period delays the configuration process. This pin has an internal pull-up resistor to VCCAUX during configuration.
DONE	Bidirectional with open-drain or totem-pole Output	**Configuration Done, Delay Start-up Sequence:** A Low-to-High output transition on this bidirectional pin signals the end of the configuration process. The FPGA produces a Low-to-High transition on this pin to indicate that the configuration process is complete. The DriveDone bitstream generation option defines whether this pin functions as a totem-pole output that actively drives High or as an open-drain output. An open-drain output requires a pull-up resistor to produce a High logic level. The open-drain option permits the DONE lines of multiple FPGAs to be tied together, so that the common node transitions High only after all of the FPGAs have completed configuration. Externally holding the open-drain output Low delays the start-up sequence, which marks the transition to user mode.
M0, M1, M2	Input	**Configuration Mode Selection:** These inputs select the configuration mode. The logic levels applied to the mode pins are sampled on the rising edge of INIT_B. See Table 75. These pins have an internal pull-up resistor to VCCAUX during configuration, making Slave Serial the default configuration mode.
HSWAP_EN	Input	**Disable Pull-up Resistors During Configuration:** A Low on this pin enables pull-up resistors on all pins that are not actively involved in the configuration process. A High value disables all pull-ups, allowing the non-configuration pins to float.
JTAG: JTAG interface pins (pull-up resistor to VCCAUX always active during configuration, regardless of HSWAP_EN pin)		
TCK	Input	**JTAG Test Clock:** The TCK clock signal synchronizes all JTAG port operations. This pin has an internal pull-up resistor to VCCAUX during configuration.

Package Overview

Table 81 shows the 10 low-cost, space-saving production package styles for the Spartan-3 family. Each package style is available as a standard and an environmentally-friendly lead-free (Pb-free) option. The Pb-free packages include an extra 'G' in the package style name. For example, the standard "VQ100" package becomes "VQG100" when ordered as the Pb-free option. The mechanical dimensions of the standard and Pb-free packages are similar, as shown in the mechanical drawings provided in Table 83.

Not all Spartan-3 device densities are available in all packages. However, for a specific package there is a common footprint that supports the various devices available in that package. See the footprint diagrams that follow.

Table 81: **Spartan-3 Family Package Options**

Package	Leads	Type	Maximum I/O	Pitch (mm)	Footprint (mm)	Height (mm)
VQ100 / VQG100	100	Very-thin Quad Flat Pack	63	0.5	16 x 16	1.20
CP132 / CPG132(1)	132	Chip-Scale Package	89	0.5	8 x 8	1.10
TQ144 / TQG144	144	Thin Quad Flat Pack	97	0.5	22 x 22	1.60
PQ208 / PQG208	208	Quad Flat Pack	141	0.5	30.6 x 30.6	4.10
FT256 / FTG256	256	Fine-pitch, Thin Ball Grid Array	173	1.0	17 x 17	1.55
FG320 / FGG320	320	Fine-pitch Ball Grid Array	221	1.0	19 x 19	2.00
FG456 / FGG456	456	Fine-pitch Ball Grid Array	333	1.0	23 x 23	2.60
FG676 / FGG676	676	Fine-pitch Ball Grid Array	489	1.0	27 x 27	2.60
FG900 / FGG900	900	Fine-pitch Ball Grid Array	633	1.0	31 x 31	2.60
FG1156 / FGG1156(1)	1156	Fine-pitch Ball Grid Array	784	1.0	35 x 35	2.60

Notes:

1. The CP132, CPG132, FG1156, and FGG1156 packages are discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

Selecting the Right Package Option

Spartan-3 FPGAs are available in both quad-flat pack (QFP) and ball grid array (BGA) packaging options. While QFP packaging offers the lowest absolute cost, the BGA packages are superior in almost every other aspect, as summarized in Table 82. Consequently, Xilinx recommends using BGA packaging whenever possible.

Table 82: **Comparing Spartan-3 Device Packaging Options**

Characteristic	Quad Flat-Pack (QFP)	Ball Grid Array (BGA)
Maximum User I/O	141	633
Packing Density (Logic/Area)	Good	Better
Signal Integrity	Fair	Better
Simultaneous Switching Output (SSO) Support	Limited	Better
Thermal Dissipation	Fair	Better
Minimum Printed Circuit Board (PCB) Layers	4	6
Hand Assembly/Rework	Possible	Very Difficult

Table 93: **PQ208 Package Pinout *(Cont'd)***

Bank	XC3S50 Pin Name	XC3S200, XC3S400 Pin Names	PQ208 Pin Number	Type
7	IO_L21N_7	IO_L21N_7	P13	I/O
7	IO_L21P_7	IO_L21P_7	P12	I/O
7	IO_L22N_7	IO_L22N_7	P16	I/O
7	IO_L22P_7	IO_L22P_7	P15	I/O
7	IO_L23N_7	IO_L23N_7	P19	I/O
7	IO_L23P_7	IO_L23P_7	P18	I/O
7	IO_L24N_7	IO_L24N_7	P21	I/O
7	IO_L24P_7	IO_L24P_7	P20	I/O
7	N.C. (◆)	IO_L39N_7	P24	I/O
7	N.C. (◆)	IO_L39P_7	P22	I/O
7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	P27	VREF
7	IO_L40P_7	IO_L40P_7	P26	I/O
7	VCCO_7	VCCO_7	P6	VCCO
7	VCCO_7	VCCO_7	P23	VCCO
N/A	GND	GND	P1	GND
N/A	GND	GND	P186	GND
N/A	GND	GND	P195	GND
N/A	GND	GND	P202	GND
N/A	GND	GND	P163	GND
N/A	GND	GND	P170	GND
N/A	GND	GND	P179	GND
N/A	GND	GND	P134	GND
N/A	GND	GND	P145	GND
N/A	GND	GND	P151	GND
N/A	GND	GND	P157	GND
N/A	GND	GND	P112	GND
N/A	GND	GND	P118	GND
N/A	GND	GND	P129	GND
N/A	GND	GND	P82	GND
N/A	GND	GND	P91	GND
N/A	GND	GND	P99	GND
N/A	GND	GND	P105	GND
N/A	GND	GND	P53	GND
N/A	GND	GND	P59	GND
N/A	GND	GND	P66	GND
N/A	GND	GND	P75	GND
N/A	GND	GND	P30	GND
N/A	GND	GND	P41	GND
N/A	GND	GND	P47	GND
N/A	GND	GND	P8	GND

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
6	N.C. (◆)	IO_L28N_6	R5	I/O
6	N.C. (◆)	IO_L28P_6	P6	I/O
6	N.C. (◆)	IO_L29N_6	R2	I/O
6	N.C. (◆)	IO_L29P_6	R1	I/O
6	N.C. (◆)	IO_L31N_6	P5	I/O
6	N.C. (◆)	IO_L31P_6	P4	I/O
6	N.C. (◆)	IO_L32N_6	P2	I/O
6	N.C. (◆)	IO_L32P_6	P1	I/O
6	N.C. (◆)	IO_L33N_6	N6	I/O
6	N.C. (◆)	IO_L33P_6	N5	I/O
6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	N4	VREF
6	IO_L34P_6	IO_L34P_6	N3	I/O
6	IO_L35N_6	IO_L35N_6	N2	I/O
6	IO_L35P_6	IO_L35P_6	N1	I/O
6	IO_L38N_6	IO_L38N_6	M6	I/O
6	IO_L38P_6	IO_L38P_6	M5	I/O
6	IO_L39N_6	IO_L39N_6	M4	I/O
6	IO_L39P_6	IO_L39P_6	M3	I/O
6	IO_L40N_6	IO_L40N_6	M2	I/O
6	IO_L40P_6/VREF_6	IO_L40P_6/VREF_6	M1	VREF
6	VCCO_6	VCCO_6	M7	VCCO
6	VCCO_6	VCCO_6	N7	VCCO
6	VCCO_6	VCCO_6	P7	VCCO
6	VCCO_6	VCCO_6	R3	VCCO
6	VCCO_6	VCCO_6	R6	VCCO
7	IO	IO	C2	I/O
7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	C3	DCI
7	IO_L01P_7/VRN_7	IO_L01P_7/VRN_7	C4	DCI
7	IO_L16N_7	IO_L16N_7	D1	I/O
7	IO_L16P_7/VREF_7	IO_L16P_7/VREF_7	C1	VREF
7	IO_L17N_7	IO_L17N_7	E4	I/O
7	IO_L17P_7	IO_L17P_7	D4	I/O
7	IO_L19N_7/VREF_7	IO_L19N_7/VREF_7	D3	VREF
7	IO_L19P_7	IO_L19P_7	D2	I/O
7	IO_L20N_7	IO_L20N_7	F4	I/O
7	IO_L20P_7	IO_L20P_7	E3	I/O
7	IO_L21N_7	IO_L21N_7	E1	I/O
7	IO_L21P_7	IO_L21P_7	E2	I/O
7	IO_L22N_7	IO_L22N_7	G6	I/O
7	IO_L22P_7	IO_L22P_7	F5	I/O

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
4	IO_L22N_4/VREF_4	IO_L22N_4/VREF_4	IO_L22N_4/VREF_4	IO_L22N_4/VREF_4	IO_L22N_4/VREF_4	AD17	VREF
4	IO_L22P_4	IO_L22P_4	IO_L22P_4	IO_L22P_4	IO_L22P_4	AB17	I/O
4	N.C. (◆)	IO_L23N_4	IO_L23N_4	IO_L23N_4	IO_L23N_4	AE17	I/O
4	N.C. (◆)	IO_L23P_4	IO_L23P_4	IO_L23P_4	IO_L23P_4	AF17	I/O
4	IO_L24N_4	IO_L24N_4	IO_L24N_4	IO_L24N_4	IO_L24N_4	Y16	I/O
4	IO_L24P_4	IO_L24P_4	IO_L24P_4	IO_L24P_4	IO_L24P_4	AA16	I/O
4	IO_L25N_4	IO_L25N_4	IO_L25N_4	IO_L25N_4	IO_L25N_4	AB16	I/O
4	IO_L25P_4	IO_L25P_4	IO_L25P_4	IO_L25P_4	IO_L25P_4	AC16	I/O
4	N.C. (◆)	IO_L26N_4	IO_L26N_4	IO_L26N_4	IO_L26N_4	AE16	I/O
4	N.C. (◆)	IO_L26P_4/VREF_4	IO_L26P_4/VREF_4	IO_L26P_4/VREF_4	IO_L26P_4/VREF_4	AF16	VREF
4	IO_L27N_4/DIN/D0	IO_L27N_4/DIN/D0	IO_L27N_4/DIN/D0	IO_L27N_4/DIN/D0	IO_L27N_4/DIN/D0	Y15	DUAL
4	IO_L27P_4/D1	IO_L27P_4/D1	IO_L27P_4/D1	IO_L27P_4/D1	IO_L27P_4/D1	W14	DUAL
4	IO_L28N_4	IO_L28N_4	IO_L28N_4	IO_L28N_4	IO_L28N_4	AA15	I/O
4	IO_L28P_4	IO_L28P_4	IO_L28P_4	IO_L28P_4	IO_L28P_4	AB15	I/O
4	IO_L29N_4	IO_L29N_4	IO_L29N_4	IO_L29N_4	IO_L29N_4	AE15	I/O
4	IO_L29P_4	IO_L29P_4	IO_L29P_4	IO_L29P_4	IO_L29P_4	AF15	I/O
4	IO_L30N_4/D2	IO_L30N_4/D2	IO_L30N_4/D2	IO_L30N_4/D2	IO_L30N_4/D2	Y14	DUAL
4	IO_L30P_4/D3	IO_L30P_4/D3	IO_L30P_4/D3	IO_L30P_4/D3	IO_L30P_4/D3	AA14	DUAL
4	IO_L31N_4/INIT_B	IO_L31N_4/INIT_B	IO_L31N_4/INIT_B	IO_L31N_4/INIT_B	IO_L31N_4/INIT_B	AC14	DUAL
4	IO_L31P_4/ DOUT/BUSY	IO_L31P_4/ DOUT/BUSY	IO_L31P_4/ DOUT/BUSY	IO_L31P_4/ DOUT/BUSY	IO_L31P_4/ DOUT/BUSY	AD14	DUAL
4	IO_L32N_4/GCLK1	IO_L32N_4/GCLK1	IO_L32N_4/GCLK1	IO_L32N_4/GCLK1	IO_L32N_4/GCLK1	AE14	GCLK
4	IO_L32P_4/GCLK0	IO_L32P_4/GCLK0	IO_L32P_4/GCLK0	IO_L32P_4/GCLK0	IO_L32P_4/GCLK0	AF14	GCLK
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	AD16	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	AD20	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	U14	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	V14	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	V15	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	V16	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	W17	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	W18	VCCO
5	IO	IO	IO	IO	IO	AA7	I/O
5	IO	IO	IO	IO	IO	AA13	I/O
5	IO	IO	IO	IO	IO_L17P_5[(3)]	AB9	I/O
5	N.C. (◆)	IO	IO	IO	IO_L17N_5[(3)]	AC9	I/O
5	IO	IO	IO	IO	IO	AC11	I/O
5	IO	IO	IO	IO	IO	AD10	I/O
5	IO	IO	IO	IO	IO	AD12	I/O
5	IO	IO	IO	IO	IO	AF4	I/O
5	IO	IO	IO	IO	IO	Y8	I/O
5	IO/VREF_5	IO/VREF_5	IO/VREF_5	IO/VREF_5	IO/VREF_5	AF5	VREF
5	IO/VREF_5	IO/VREF_5	IO/VREF_5	IO/VREF_5	IO/VREF_5	AF13	VREF
5	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	AC5	DUAL

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
7	IO_L29P_7	IO_L29P_7	IO_L29P_7	IO_L29P_7	IO_L29P_7	L2	I/O
7	IO_L31N_7	IO_L31N_7	IO_L31N_7	IO_L31N_7	IO_L31N_7	M7	I/O
7	IO_L31P_7	IO_L31P_7	IO_L31P_7	IO_L31P_7	IO_L31P_7	M8	I/O
7	IO_L32N_7	IO_L32N_7	IO_L32N_7	IO_L32N_7	IO_L32N_7	M6	I/O
7	IO_L32P_7	IO_L32P_7	IO_L32P_7	IO_L32P_7	IO_L32P_7	M5	I/O
7	IO_L33N_7	IO_L33N_7	IO_L33N_7	IO_L33N_7	IO_L33N_7	M3	I/O
7	IO_L33P_7	IO_L33P_7	IO_L33P_7	IO_L33P_7	IO_L33P_7	L4	I/O
7	IO_L34N_7	IO_L34N_7	IO_L34N_7	IO_L34N_7	IO_L34N_7	M1	I/O
7	IO_L34P_7	IO_L34P_7	IO_L34P_7	IO_L34P_7	IO_L34P_7	M2	I/O
7	IO_L35N_7	IO_L35N_7	IO_L35N_7	IO_L35N_7	IO_L35N_7	N7	I/O
7	IO_L35P_7	IO_L35P_7	IO_L35P_7	IO_L35P_7	IO_L35P_7	N8	I/O
7	IO_L38N_7	IO_L38N_7	IO_L38N_7	IO_L38N_7	IO_L38N_7	N5	I/O
7	IO_L38P_7	IO_L38P_7	IO_L38P_7	IO_L38P_7	IO_L38P_7	N6	I/O
7	IO_L39N_7	IO_L39N_7	IO_L39N_7	IO_L39N_7	IO_L39N_7	N3	I/O
7	IO_L39P_7	IO_L39P_7	IO_L39P_7	IO_L39P_7	IO_L39P_7	N4	I/O
7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	N1	VREF
7	IO_L40P_7	IO_L40P_7	IO_L40P_7	IO_L40P_7	IO_L40P_7	N2	I/O
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	G3	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	J8	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	K8	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	L3	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	L9	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	M9	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	N9	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	N10	VCCO
N/A	GND	GND	GND	GND	GND	A1	GND
N/A	GND	GND	GND	GND	GND	A26	GND
N/A	GND	GND	GND	GND	GND	AC4	GND
N/A	GND	GND	GND	GND	GND	AC12	GND
N/A	GND	GND	GND	GND	GND	AC15	GND
N/A	GND	GND	GND	GND	GND	AC23	GND
N/A	GND	GND	GND	GND	GND	AD3	GND
N/A	GND	GND	GND	GND	GND	AD24	GND
N/A	GND	GND	GND	GND	GND	AE2	GND
N/A	GND	GND	GND	GND	GND	AE25	GND
N/A	GND	GND	GND	GND	GND	AF1	GND
N/A	GND	GND	GND	GND	GND	AF26	GND
N/A	GND	GND	GND	GND	GND	B2	GND
N/A	GND	GND	GND	GND	GND	B25	GND
N/A	GND	GND	GND	GND	GND	C3	GND
N/A	GND	GND	GND	GND	GND	C24	GND
N/A	GND	GND	GND	GND	GND	D4	GND
N/A	GND	GND	GND	GND	GND	D12	GND

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
1	IO_L25P_1	IO_L25P_1	D19	I/O
1	IO_L26N_1	IO_L26N_1	A19	I/O
1	IO_L26P_1	IO_L26P_1	B19	I/O
1	IO_L27N_1	IO_L27N_1	F17	I/O
1	IO_L27P_1	IO_L27P_1	G17	I/O
1	IO_L28N_1	IO_L28N_1	B17	I/O
1	IO_L28P_1	IO_L28P_1	C17	I/O
1	IO_L29N_1	IO_L29N_1	J16	I/O
1	IO_L29P_1	IO_L29P_1	K16	I/O
1	IO_L30N_1	IO_L30N_1	G16	I/O
1	IO_L30P_1	IO_L30P_1	H16	I/O
1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	D16	VREF
1	IO_L31P_1	IO_L31P_1	E16	I/O
1	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	B16	GCLK
1	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	C16	GCLK
1	N.C. (◆)	IO_L37N_1	H18	I/O
1	N.C. (◆)	IO_L37P_1	J18	I/O
1	N.C. (◆)	IO_L38N_1	D18	I/O
1	N.C. (◆)	IO_L38P_1	E18	I/O
1	N.C. (◆)	IO_L39N_1	A18	I/O
1	N.C. (◆)	IO_L39P_1	B18	I/O
1	N.C. (◆)	IO_L40N_1	K17	I/O
1	N.C. (◆)	IO_L40P_1	K18	I/O
1	VCCO_1	VCCO_1	L17	VCCO
1	VCCO_1	VCCO_1	C18	VCCO
1	VCCO_1	VCCO_1	G18	VCCO
1	VCCO_1	VCCO_1	L18	VCCO
1	VCCO_1	VCCO_1	L19	VCCO
1	VCCO_1	VCCO_1	J20	VCCO
1	VCCO_1	VCCO_1	C22	VCCO
1	VCCO_1	VCCO_1	G22	VCCO
1	VCCO_1	VCCO_1	E24	VCCO
1	VCCO_1	VCCO_1	C26	VCCO
2	IO	IO	J25	I/O
2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	C29	DCI
2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	C30	DCI
2	IO_L02N_2	IO_L02N_2	D27	I/O
2	IO_L02P_2	IO_L02P_2	D28	I/O
2	IO_L03N_2/VREF_2	IO_L03N_2/VREF_2	D29	VREF
2	IO_L03P_2	IO_L03P_2	D30	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
3	N.C. (◆)	IO_L50P_3	V26	I/O
3	VCCO_3	VCCO_3	U20	VCCO
3	VCCO_3	VCCO_3	V20	VCCO
3	VCCO_3	VCCO_3	W20	VCCO
3	VCCO_3	VCCO_3	Y22	VCCO
3	VCCO_3	VCCO_3	V24	VCCO
3	VCCO_3	VCCO_3	AB24	VCCO
3	VCCO_3	VCCO_3	AD26	VCCO
3	VCCO_3	VCCO_3	V28	VCCO
3	VCCO_3	VCCO_3	AB28	VCCO
3	VCCO_3	VCCO_3	AF28	VCCO
4	IO	IO	AA16	I/O
4	IO	IO	AG18	I/O
4	IO	IO	AA18	I/O
4	IO	IO	AE22	I/O
4	IO	IO	AD23	I/O
4	IO	IO	AH27	I/O
4	IO/VREF_4	IO/VREF_4	AF16	VREF
4	IO/VREF_4	IO/VREF_4	AK28	VREF
4	IO_L01N_4/VRP_4	IO_L01N_4/VRP_4	AJ27	DCI
4	IO_L01P_4/VRN_4	IO_L01P_4/VRN_4	AK27	DCI
4	IO_L02N_4	IO_L02N_4	AJ26	I/O
4	IO_L02P_4	IO_L02P_4	AK26	I/O
4	IO_L03N_4	IO_L03N_4	AG26	I/O
4	IO_L03P_4	IO_L03P_4	AF25	I/O
4	IO_L04N_4	IO_L04N_4	AD24	I/O
4	IO_L04P_4	IO_L04P_4	AC23	I/O
4	IO_L05N_4	IO_L05N_4	AE23	I/O
4	IO_L05P_4	IO_L05P_4	AF23	I/O
4	IO_L06N_4/VREF_4	IO_L06N_4/VREF_4	AG23	VREF
4	IO_L06P_4	IO_L06P_4	AH23	I/O
4	IO_L07N_4	IO_L07N_4	AJ23	I/O
4	IO_L07P_4	IO_L07P_4	AK23	I/O
4	IO_L08N_4	IO_L08N_4	AB22	I/O
4	IO_L08P_4	IO_L08P_4	AC22	I/O
4	IO_L09N_4	IO_L09N_4	AF22	I/O
4	IO_L09P_4	IO_L09P_4	AG22	I/O
4	IO_L10N_4	IO_L10N_4	AJ22	I/O
4	IO_L10P_4	IO_L10P_4	AK22	I/O
4	IO_L11N_4	IO_L11N_4	AD21	I/O