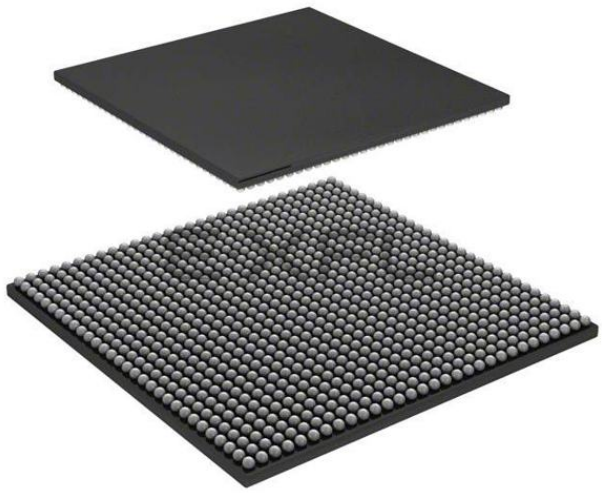
AMD Xilinx - XC3S4000-4FGG900I Datasheet



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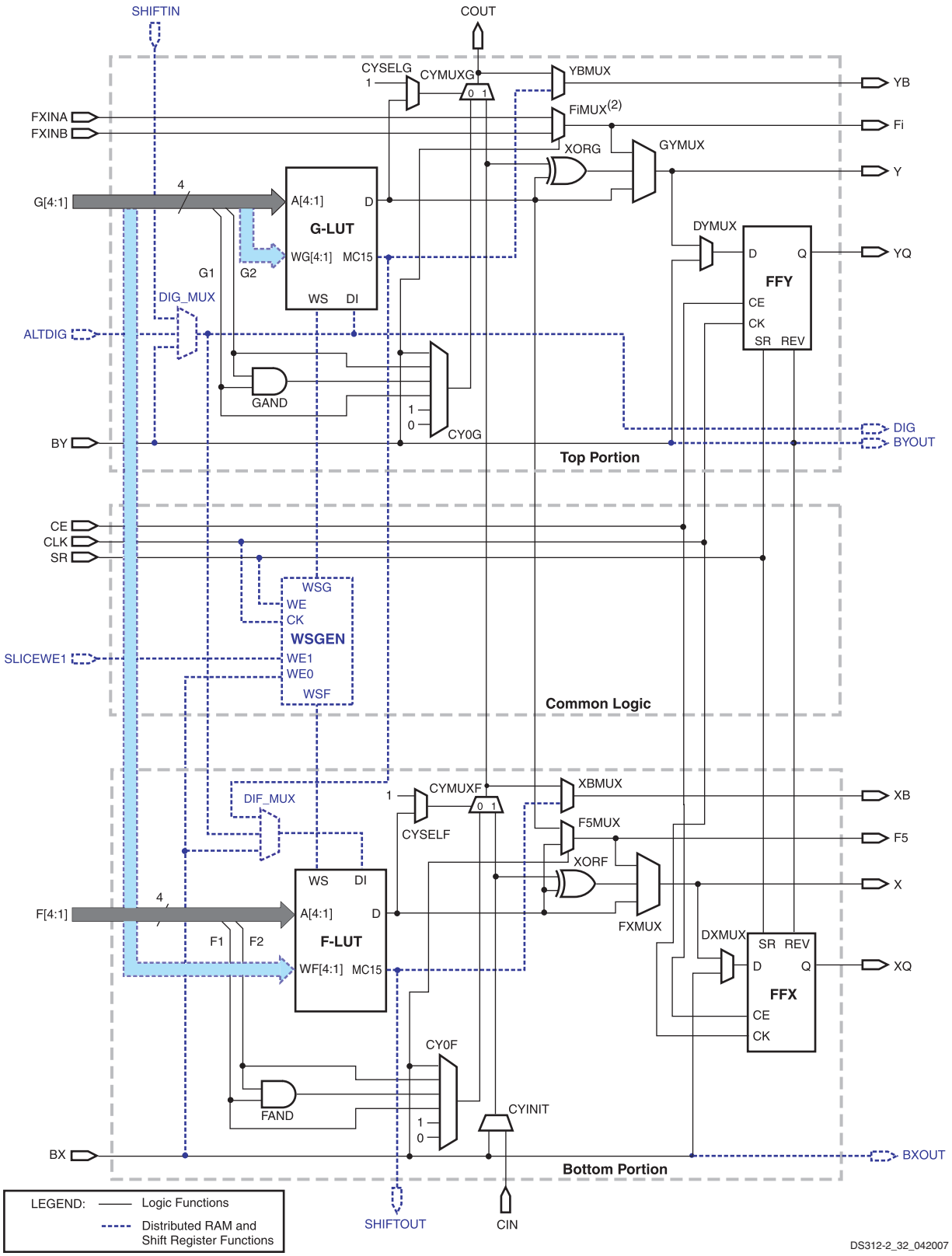
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	6912
Number of Logic Elements/Cells	62208
Total RAM Bits	1769472
Number of I/O	633
Number of Gates	4000000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	900-BBGA
Supplier Device Package	900-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s4000-4fgg900i



Notes:

1. Options to invert signal polarity as well as other options that enable lines for various functions are not shown.
2. The index i can be 6, 7, or 8, depending on the slice. In this position, the upper right-hand slice has an F8MUX, and the upper left-hand slice has an F7MUX. The lower right-hand and left-hand slices both have an F6MUX.

Figure 12: **Simplified Diagram of the Left-Hand SLICEM**

Function Generator

Each of the two LUTs (F and G) in a slice have four logic inputs (A1-A4) and a single output (D). This permits any four-variable Boolean logic operation to be programmed into them. Furthermore, wide function multiplexers can be used to effectively combine LUTs within the same CLB or across different CLBs, making logic functions with still more input variables possible.

The LUTs in both the right-hand and left-hand slice-pairs not only support the logic functions described above, but also can function as ROM that is initialized with data at the time of configuration.

The LUTs in the left-hand slice-pair (even-numbered columns such as X0 in Figure 11) of each CLB support two additional functions that the right-hand slice-pair (odd-numbered columns such as X1) do not.

First, it is possible to program the “left-hand LUTs” as distributed RAM. This type of memory affords moderate amounts of data buffering anywhere along a data path. One left-hand LUT stores 16 bits. Multiple left-hand LUTs can be combined in various ways to store larger amounts of data. A dual port option combines two LUTs so that memory access is possible from two independent data lines. A Distributed ROM option permits pre-loading the memory with data during FPGA configuration.

Second, it is possible to program each left-hand LUT as a 16-bit shift register. Used in this way, each LUT can delay serial data anywhere from one to 16 clock cycles. The four left-hand LUTs of a single CLB can be combined to produce delays up to 64 clock cycles. The SHIFTIN and SHIFTOUT lines cascade LUTs to form larger shift registers. It is also possible to combine shift registers across more than one CLB. The resulting programmable delays can be used to balance the timing of data pipelines.

Block RAM Overview

All Spartan-3 devices support block RAM, which is organized as configurable, synchronous 18Kbit blocks. Block RAM stores relatively large amounts of data more efficiently than the distributed RAM feature described earlier. (The latter is better suited for buffering small amounts of data anywhere along signal paths.) This section describes basic Block RAM functions. For more information, refer to the chapter entitled “Using Block RAM” in UG331.

The aspect ratio—i.e., width vs. depth—of each block RAM is configurable. Furthermore, multiple blocks can be cascaded to create still wider and/or deeper memories.

A choice among primitives determines whether the block RAM functions as dual- or single-port memory. A name of the form RAMB16_S[w_A]_S[w_B] calls out the dual-port primitive, where the integers w_A and w_B specify the total data path width at ports w_A and w_B, respectively. Thus, a RAMB16_S9_S18 is a dual-port RAM with a 9-bit-wide Port A and an 18-bit-wide Port B. A name of the form RAMB16_S[w] identifies the single-port primitive, where the integer w specifies the total data path width of the lone port. A RAMB16_S18 is a single-port RAM with an 18-bit-wide port. Other memory functions—e.g., FIFOs, data path width conversion, ROM, etc.—are readily available using the CORE Generator™ software, part of the Xilinx development software.

Table 30: **Power Voltage Ramp Time Requirements**

Symbol	Description	Device	Package	Min	Max	Units
T_{CCO}	V_{CCO} ramp time for all eight banks	All	All	No limit(4)	–	N/A
T_{CCINT}	V_{CCINT} ramp time, only if V_{CCINT} is last in three-rail power-on sequence	All	All	No limit	No limit(5)	N/A

Notes:

1. If a limit exists, this specification is based on characterization.
2. The ramp time is measured from 10% to 90% of the full nominal voltage swing for all I/O standards.
3. For information on power-on current needs, see Power-On Behavior, page 54
4. For mask revisions earlier than revision E (see Mask and Fab Revisions, page 58), T_{CCO} min is limited to 2.0 ms for the XC3S200 and XC3S400 devices in QFP packages, and limited to 0.6 ms for the XC3S200, XC3S400, XC3S1500, and XC3S4000 devices in the FT and FG packages.
5. For earlier device versions with the FQ fabrication/process code (see Mask and Fab Revisions, page 58), T_{CCINT} max is limited to 500 µs.

Table 31: **Power Voltage Levels Necessary for Preserving RAM Contents**

Symbol	Description	Min	Units
V_{DRINT}	V_{CCINT} level required to retain RAM data	1.0	V
V_{DRAUX}	V_{CCAUX} level required to retain RAM data	2.0	V

Notes:

1. RAM contents include data stored in CMOS configuration latches.
2. The level of the V_{CCO} supply has no effect on data retention.
3. If a brown-out condition occurs where V_{CCAUX} or V_{CCINT} drops below the retention voltage, then V_{CCAUX} or V_{CCINT} must drop below the minimum power-on reset voltage indicated in Table 29 in order to clear out the device configuration content.

Table 32: **General Recommended Operating Conditions**

Symbol	Description		Min	Nom	Max	Units
T_J	Junction temperature	Commercial	0	25	85	°C
		Industrial	–40	25	100	°C
V_{CCINT}	Internal supply voltage		1.140	1.200	1.260	V
V_{CCO}(1)	Output driver supply voltage		1.140	–	3.465	V
V_{CCAUX}	Auxiliary supply voltage		2.375	2.500	2.625	V
ΔV_{CCAUX}(2)	Voltage variance on VCCAUX when using a DCM		–	–	10	mV/ms
V_{IN}(3)	Voltage applied to all User I/O pins and Dual-Purpose pins relative to GND(4)(6)	V_{CCO} = 3.3V, IO	–0.3	–	3.75	V
		V_{CCO} = 3.3V, IO_Lxxy(7)	–0.3	–	3.75	V
		$V_{CCO} \le$ 2.5V, IO	–0.3	–	V_{CCO} + 0.3(4)	V
		$V_{CCO} \le$ 2.5V, IO_Lxxy(7)	–0.3	–	V_{CCO} + 0.3(4)	V
	Voltage applied to all Dedicated pins relative to GND(5)		–0.3	–	V_{CCAUX} + 0.3(5)	V

Notes:

1. The V_{CCO} range given here spans the lowest and highest operating voltages of all supported I/O standards. The recommended V_{CCO} range specific to each of the single-ended I/O standards is given in Table 35, and that specific to the differential standards is given in Table 37.
2. Only during DCM operation is it recommended that the rate of change of V_{CCAUX} not exceed 10 mV/ms.
3. Input voltages outside the recommended range are permissible provided that the I_{IK} input diode clamp diode rating is met. Refer to Table 28.
4. Each of the User I/O and Dual-Purpose pins is associated with one of the V_{CCO} rails. Meeting the V_{IN} limit ensures that the internal diode junctions that exist between these pins and their associated V_{CCO} and GND rails do not turn on. The absolute maximum rating is provided in Table 28.
5. All Dedicated pins (PROG_B, DONE, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail (2.5V). Meeting the V_{IN} max limit ensures that the internal diode junctions that exist between each of these pins and the V_{CCAUX} and GND rails do not turn on.
6. See XAPP459, *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Generation FPGAs*.
7. For single-ended signals that are placed on a differential-capable I/O, V_{IN} of –0.2V to –0.3V is supported but can cause increased leakage between the two pins. See the *Parasitic Leakage* section in UG331, *Spartan-3 Generation FPGA User Guide*.

Date	Version	Description
05/25/07	2.2	Improved absolute maximum voltage specifications in Table 28, providing additional overshoot allowance. Improved XC3S50 HBM ESD to 2000V in Table 28. Based on extensive 90 nm production data, improved (reduced) the maximum quiescent current limits for the I_{CCINTQ} and I_{CCOQ} specifications in Table 34. Widened the recommended voltage range for the PCI standard and clarified the hysteresis footnote in Table 35. Noted restriction on combining differential outputs in Table 38. Updated footnote 1 in Table 64.
11/30/07	2.3	Updated 3.3V VCCO max from 3.45V to 3.465V in Table 32 and elsewhere. Reduced t_{ICCK} minimum from 0.50µs to 0.25µs in Table 65. Updated links to technical documentation.
06/25/08	2.4	Clarified dual marking. Added Mask and Fab Revisions. Added references to XAPP459 in Table 28 and Table 32. Removed absolute minimum and added footnote referring to timing analyzer for minimum delay values. Added HSLVDCI to Table 48 and Table 50. Updated t_{DICK} in Table 51 to match largest possible value in speed file. Updated formatting and links.
12/04/09	2.5	Updated notes 2 and 3 in Table 28. Removed silicon process specific information and revised notes in Table 30. Updated note 3 in Table 32. Updated note 3 in Table 34. Updated note 5 in Table 35. Updated V_{OL} max and V_{OH} min for SSTL2_II in Table 36. Updated note 5 in Table 36. Updated JTAG Waveforms in Figure 39. Updated V_{ICM} max for LVPECL_25 in Table 37. Updated RT and VT for LVDS_25_DCI in Table 48. Updated Simultaneously Switching Output Guidelines. Noted that the CP132 package is being discontinued in Table 49. Removed minimum values for T_{MULTCK} clock-to-output times in Table 54. Updated footnote 3 in Table 58. Removed minimum values for T_{MULT} propagation times in Table 55. Removed silicon process specific information and revised notes in Table 61. Updated Phase Shifter (PS).
10/29/12	3.0	Added Notice of Disclaimer. Per XCN07022, updated the discontinued FG1156 and FGG1156 package discussion throughout document. Per XCN08011, updated the discontinued CP132 and CPG132 package discussion throughout document. Revised description of V_{IN} in Table 32 and added note 7. Added note 4 to Table 33. This product is not recommended for new designs.

HSWAP_EN: Disable Pull-up Resistors During Configuration

As shown in Table 76, a Low on this asynchronous pin enables pull-up resistors on all user I/Os not actively involved in the configuration process, although only until device configuration completes. A High disables the pull-up resistors during configuration, which is the desired state for some applications.

The dedicated configuration CONFIG pins (CCLK, DONE, PROG_B, HSWAP_EN, M2, M1, M0), the JTAG pins (TDI, TMS, TCK, TDO) and the INIT_B always have active pull-up resistors during configuration, regardless of the value on HSWAP_EN.

After configuration, HSWAP_EN becomes a "don't care" input and any pull-up resistors previously enabled by HSWAP_EN are disabled. If a user I/O in the application requires a pull-up resistor after configuration, place a PULLUP primitive on the associated I/O pin or, for some pins, set the associated bitstream generator option.

Table 76: **HSWAP_EN Encoding**

HSWAP_EN	Function
During Configuration	
0	Enable pull-up resistors on all pins not actively involved in the configuration process. Pull-ups are only active until configuration completes. See Table 79.
1	No pull-up resistors during configuration.
After Configuration, User Mode	
X	This pin has no function except during device configuration.

Notes:

1. X = don't care, either 0 or 1.

The Bitstream generator option HswapenPin determines whether a pull-up resistor to VCCAUX, a pull-down resistor, or no resistor is present on HSWAP_EN after configuration.

JTAG: Dedicated JTAG Port Pins

Table 77: **JTAG Pin Descriptions**

Pin Name	Direction	Description	Bitstream Generation Option
TCK	Input	**Test Clock:** The TCK clock signal synchronizes all boundary scan operations on its rising edge.	The BitGen option **TckPin** determines whether a pull-up resistor, pull-down resistor or no resistor is present.
TDI	Input	**Test Data Input:** TDI is the serial data input for all JTAG instruction and data registers. This input is sampled on the rising edge of TCK.	The BitGen option **TdiPin** determines whether a pull-up resistor, pull-down resistor or no resistor is present.
TMS	Input	**Test Mode Select:** The TMS input controls the sequence of states through which the JTAG TAP state machine passes. This input is sampled on the rising edge of TCK.	The BitGen option **TmsPin** determines whether a pull-up resistor, pull-down resistor or no resistor is present.
TDO	Output	**Test Data Output:** The TDO pin is the data output for all JTAG instruction and data registers. This output is sampled on the rising edge of TCK. The TDO output is an active totem-pole driver and is not like the open-collector TDO output on Virtex®-II Pro FPGAs.	The BitGen option **TdoPin** determines whether a pull-up resistor, pull-down resistor or no resistor is present.

These pins are dedicated connections to the four-wire IEEE 1532/IEEE 1149.1 JTAG port, shown in Figure 43 and described in Table 77. The JTAG port is used for boundary-scan testing, device configuration, application debugging, and possibly an additional serial port for the application. These pins are dedicated and are not available as user-I/O pins. Every package has four dedicated JTAG pins and these pins are powered by the +2.5V VCCAUX supply.

For additional information on JTAG configuration, see Boundary-Scan (JTAG) Mode, page 50.

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
0	VCCO_0	G9	VCCO
1	IO	A11	I/O
1	IO	B13	I/O
1	IO	D10	I/O
1	IO/VREF_1	A12	VREF
1	IO_L01N_1/VRP_1	A16	DCI
1	IO_L01P_1/VRN_1	A17	DCI
1	IO_L10N_1/VREF_1	A15	VREF
1	IO_L10P_1	B15	I/O
1	IO_L15N_1	C14	I/O
1	IO_L15P_1	C15	I/O
1	IO_L16N_1	A14	I/O
1	IO_L16P_1	B14	I/O
1	IO_L24N_1	D14	I/O
1	IO_L24P_1	D13	I/O
1	IO_L27N_1	E13	I/O
1	IO_L27P_1	E12	I/O
1	IO_L28N_1	C12	I/O
1	IO_L28P_1	D12	I/O
1	IO_L29N_1	F11	I/O
1	IO_L29P_1	E11	I/O
1	IO_L30N_1	C11	I/O
1	IO_L30P_1	D11	I/O
1	IO_L31N_1/VREF_1	A10	VREF
1	IO_L31P_1	B10	I/O
1	IO_L32N_1/GCLK5	E10	GCLK
1	IO_L32P_1/GCLK4	F10	GCLK
1	VCCO_1	B11	VCCO
1	VCCO_1	C13	VCCO
1	VCCO_1	G10	VCCO
1	VCCO_1	G11	VCCO
2	IO	J13	I/O
2	IO_L01N_2/VRP_2	C16	DCI
2	IO_L01P_2/VRN_2	C17	DCI
2	IO_L16N_2	B18	I/O
2	IO_L16P_2	C18	I/O
2	IO_L17N_2	D17	I/O
2	IO_L17P_2/VREF_2	D18	VREF
2	IO_L19N_2	D16	I/O
2	IO_L19P_2	E16	I/O

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
N/A	GND	J3	GND
N/A	GND	J8	GND
N/A	GND	K11	GND
N/A	GND	K16	GND
N/A	GND	K3	GND
N/A	GND	K8	GND
N/A	GND	L10	GND
N/A	GND	L11	GND
N/A	GND	L8	GND
N/A	GND	L9	GND
N/A	GND	M12	GND
N/A	GND	M7	GND
N/A	GND	N1	GND
N/A	GND	N18	GND
N/A	GND	T10	GND
N/A	GND	T9	GND
N/A	GND	U17	GND
N/A	GND	U2	GND
N/A	GND	V1	GND
N/A	GND	V13	GND
N/A	GND	V18	GND
N/A	GND	V6	GND
N/A	VCCAUX	B12	VCCAUX
N/A	VCCAUX	B7	VCCAUX
N/A	VCCAUX	G17	VCCAUX
N/A	VCCAUX	G2	VCCAUX
N/A	VCCAUX	M17	VCCAUX
N/A	VCCAUX	M2	VCCAUX
N/A	VCCAUX	U12	VCCAUX
N/A	VCCAUX	U7	VCCAUX
N/A	VCCINT	F12	VCCINT
N/A	VCCINT	F13	VCCINT
N/A	VCCINT	F6	VCCINT
N/A	VCCINT	F7	VCCINT
N/A	VCCINT	G13	VCCINT
N/A	VCCINT	G6	VCCINT
N/A	VCCINT	M13	VCCINT
N/A	VCCINT	M6	VCCINT
N/A	VCCINT	N12	VCCINT
N/A	VCCINT	N13	VCCINT

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
2	IO_L21P_2	IO_L21P_2	E22	I/O
2	IO_L22N_2	IO_L22N_2	G17	I/O
2	IO_L22P_2	IO_L22P_2	G18	I/O
2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	F19	VREF
2	IO_L23P_2	IO_L23P_2	G19	I/O
2	IO_L24N_2	IO_L24N_2	F20	I/O
2	IO_L24P_2	IO_L24P_2	F21	I/O
2	N.C. (◆)	IO_L26N_2	G20	I/O
2	N.C. (◆)	IO_L26P_2	H19	I/O
2	IO_L27N_2	IO_L27N_2	G21	I/O
2	IO_L27P_2	IO_L27P_2	G22	I/O
2	N.C. (◆)	IO_L28N_2	H18	I/O
2	N.C. (◆)	IO_L28P_2	J17	I/O
2	N.C. (◆)	IO_L29N_2	H21	I/O
2	N.C. (◆)	IO_L29P_2	H22	I/O
2	N.C. (◆)	IO_L31N_2	J18	I/O
2	N.C. (◆)	IO_L31P_2	J19	I/O
2	N.C. (◆)	IO_L32N_2	J21	I/O
2	N.C. (◆)	IO_L32P_2	J22	I/O
2	N.C. (◆)	IO_L33N_2	K17	I/O
2	N.C. (◆)	IO_L33P_2	K18	I/O
2	IO_L34N_2/VREF_2	IO_L34N_2/VREF_2	K19	VREF
2	IO_L34P_2	IO_L34P_2	K20	I/O
2	IO_L35N_2	IO_L35N_2	K21	I/O
2	IO_L35P_2	IO_L35P_2	K22	I/O
2	IO_L38N_2	IO_L38N_2	L17	I/O
2	IO_L38P_2	IO_L38P_2	L18	I/O
2	IO_L39N_2	IO_L39N_2	L19	I/O
2	IO_L39P_2	IO_L39P_2	L20	I/O
2	IO_L40N_2	IO_L40N_2	L21	I/O
2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	L22	VREF
2	VCCO_2	VCCO_2	H17	VCCO
2	VCCO_2	VCCO_2	H20	VCCO
2	VCCO_2	VCCO_2	J16	VCCO
2	VCCO_2	VCCO_2	K16	VCCO
2	VCCO_2	VCCO_2	L16	VCCO
3	IO	IO	Y21	I/O
3	IO_L01N_3/VRP_3	IO_L01N_3/VRP_3	Y20	DCI
3	IO_L01P_3/VRN_3	IO_L01P_3/VRN_3	Y19	DCI
3	IO_L16N_3	IO_L16N_3	W22	I/O

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
3	IO_L16P_3	IO_L16P_3	Y22	I/O
3	IO_L17N_3	IO_L17N_3	V19	I/O
3	IO_L17P_3/VREF_3	IO_L17P_3/VREF_3	W19	VREF
3	IO_L19N_3	IO_L19N_3	W21	I/O
3	IO_L19P_3	IO_L19P_3	W20	I/O
3	IO_L20N_3	IO_L20N_3	U19	I/O
3	IO_L20P_3	IO_L20P_3	V20	I/O
3	IO_L21N_3	IO_L21N_3	V22	I/O
3	IO_L21P_3	IO_L21P_3	V21	I/O
3	IO_L22N_3	IO_L22N_3	T17	I/O
3	IO_L22P_3	IO_L22P_3	U18	I/O
3	IO_L23N_3	IO_L23N_3	U21	I/O
3	IO_L23P_3/VREF_3	IO_L23P_3/VREF_3	U20	VREF
3	IO_L24N_3	IO_L24N_3	R18	I/O
3	IO_L24P_3	IO_L24P_3	T18	I/O
3	N.C. (◆)	IO_L26N_3	T20	I/O
3	N.C. (◆)	IO_L26P_3	T19	I/O
3	IO_L27N_3	IO_L27N_3	T22	I/O
3	IO_L27P_3	IO_L27P_3	T21	I/O
3	N.C. (◆)	IO_L28N_3	R22	I/O
3	N.C. (◆)	IO_L28P_3	R21	I/O
3	N.C. (◆)	IO_L29N_3	P19	I/O
3	N.C. (◆)	IO_L29P_3	R19	I/O
3	N.C. (◆)	IO_L31N_3	P18	I/O
3	N.C. (◆)	IO_L31P_3	P17	I/O
3	N.C. (◆)	IO_L32N_3	P22	I/O
3	N.C. (◆)	IO_L32P_3	P21	I/O
3	N.C. (◆)	IO_L33N_3	N18	I/O
3	N.C. (◆)	IO_L33P_3	N17	I/O
3	IO_L34N_3	IO_L34N_3	N20	I/O
3	IO_L34P_3/VREF_3	IO_L34P_3/VREF_3	N19	VREF
3	IO_L35N_3	IO_L35N_3	N22	I/O
3	IO_L35P_3	IO_L35P_3	N21	I/O
3	IO_L38N_3	IO_L38N_3	M18	I/O
3	IO_L38P_3	IO_L38P_3	M17	I/O
3	IO_L39N_3	IO_L39N_3	M20	I/O
3	IO_L39P_3	IO_L39P_3	M19	I/O
3	IO_L40N_3/VREF_3	IO_L40N_3/VREF_3	M22	VREF
3	IO_L40P_3	IO_L40P_3	M21	I/O
3	VCCO_3	VCCO_3	M16	VCCO

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
4	IO_L30N_4/D2	IO_L30N_4/D2	U12	DUAL
4	IO_L30P_4/D3	IO_L30P_4/D3	V12	DUAL
4	IO_L31N_4/INIT_B	IO_L31N_4/INIT_B	W12	DUAL
4	IO_L31P_4/DOUT/BUSY	IO_L31P_4/DOUT/BUSY	Y12	DUAL
4	IO_L32N_4/GCLK1	IO_L32N_4/GCLK1	AA12	GCLK
4	IO_L32P_4/GCLK0	IO_L32P_4/GCLK0	AB12	GCLK
4	VCCO_4	VCCO_4	T12	VCCO
4	VCCO_4	VCCO_4	T13	VCCO
4	VCCO_4	VCCO_4	T14	VCCO
4	VCCO_4	VCCO_4	U15	VCCO
4	VCCO_4	VCCO_4	Y15	VCCO
5	IO	IO	U7	I/O
5	N.C. (◆)	IO	U9	I/O
5	IO	IO	U10	I/O
5	IO	IO	U11	I/O
5	IO	IO	V7	I/O
5	IO	IO	V10	I/O
5	IO/VREF_5	IO/VREF_5	AB11	VREF
5	IO/VREF_5	IO/VREF_5	U6	VREF
5	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	Y4	DUAL
5	IO_L01P_5/CS_B	IO_L01P_5/CS_B	AA3	DUAL
5	IO_L06N_5	IO_L06N_5	AB4	I/O
5	IO_L06P_5	IO_L06P_5	AA4	I/O
5	IO_L09N_5	IO_L09N_5	Y5	I/O
5	IO_L09P_5	IO_L09P_5	W5	I/O
5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	AB5	DCI
5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	AA5	DCI
5	IO_L15N_5	IO_L15N_5	W6	I/O
5	IO_L15P_5	IO_L15P_5	V6	I/O
5	IO_L16N_5	IO_L16N_5	AA6	I/O
5	IO_L16P_5	IO_L16P_5	Y6	I/O
5	N.C. (◆)	IO_L19N_5	Y7	I/O
5	N.C. (◆)	IO_L19P_5/ VREF_5	W7	VREF
5	N.C. (◆)	IO_L22N_5	AB7	I/O
5	N.C. (◆)	IO_L22P_5	AA7	I/O
5	IO_L24N_5	IO_L24N_5	W8	I/O
5	IO_L24P_5	IO_L24P_5	V8	I/O
5	IO_L25N_5	IO_L25N_5	AB8	I/O
5	IO_L25P_5	IO_L25P_5	AA8	I/O

FG456 Footprint

Left Half of FG456 Package (Top View)

XC3S400 (264 max. user I/O)

196 **I/O:** Unrestricted, general-purpose user I/O

32 **VREF:** User I/O or input voltage reference for bank

69 **N.C.:** Unconnected pins for XC3S400 (◆)

XC3S1000, XC3S1500, XC3S2000 (333 max user I/O)

261 **I/O:** Unrestricted, general-purpose user I/O

36 **VREF:** User I/O or input voltage reference for bank

0 **N.C.:** No unconnected pins in this package

All devices

12 **DUAL:** Configuration pin, then possible user I/O

8 **GCLK:** User I/O or global clock buffer input

16 **DCI:** User I/O or reference resistor input for bank

7 **CONFIG:** Dedicated configuration pins

4 **JTAG:** Dedicated JTAG port pins

12 **VCCINT:** Internal core voltage supply (+1.2V)

40 **VCCO:** Output voltage supply for bank

8 **VCCAUX:** Auxiliary voltage supply (+2.5V)

52 **GND:** Ground

	Bank 0										
	1	2	3	4	5	6	7	8	9	10	11
A	GND	PROG_B	IO VREF_0	I/O L01P_0 VRN_0	I/O L09P_0	VCCAUX	I/O L19P_0 ◆	I/O L24P_0	I/O L27P_0	I/O	I/O L32P_0 GCLK6
B	TDI	GND	HSWAP_EN	I/O L01N_0 VRP_0	I/O L09N_0	I/O L15P_0	I/O L19N_0 ◆	I/O L24N_0	I/O L27N_0	I/O L29P_0	I/O L32N_0 GCLK7
C	I/O L16P_7 VREF_7	I/O	I/O L01N_7 VRP_7	I/O L01P_7 VRN_7	I/O L06P_0	I/O L15N_0	IO VREF_0	VCCO_0	GND	I/O L29N_0	I/O L31P_0 VREF_0
D	I/O L16N_7	I/O L19P_7	I/O L19N_7 VREF_7	I/O L17P_7	I/O L06N_0	I/O L10P_0	I/O L16P_0	I/O L22P_0 ◆	I/O	I/O	I/O L31N_0
E	I/O L21N_7	I/O L21P_7	I/O L20P_7	I/O L17N_7	IO VREF_0 ◆	I/O L10N_0	I/O L16N_0	I/O L22N_0 ◆	I/O L25P_0	I/O L28P_0	I/O L30P_0
F	VCCAUX	I/O L23N_7	I/O L23P_7	I/O L20N_7	I/O L22P_7	I/O	IO VREF_0	VCCO_0	I/O L25N_0	I/O L28N_0	I/O L30N_0
G	I/O L27N_7	I/O L27P_7 VREF_7	I/O L26N_7 ◆	I/O L26P_7 ◆	I/O L24P_7	I/O L22N_7	VCCINT	VCCINT	VCCO_0	VCCO_0	VCCO_0
H	I/O L28N_7 ◆	I/O L28P_7 ◆	VCCO_7	I/O L29P_7 ◆	I/O L24N_7	VCCO_7	VCCINT				
J	I/O L32N_7 ◆	I/O L32P_7 ◆	GND	I/O L29N_7 ◆	I/O L31N_7 ◆	I/O L31P_7 ◆	VCCO_7		GND	GND	GND
K	I/O L35N_7	I/O L35P_7	I/O L34N_7	I/O L34P_7	I/O L33N_7 ◆	I/O L33P_7 ◆	VCCO_7		GND	GND	GND
L	I/O L40N_7 VREF_7	I/O L40P_7	I/O L39N_7	I/O L39P_7	I/O L38N_7	I/O L38P_7	VCCO_7		GND	GND	GND
M	I/O L40P_6 VREF_6	I/O L40N_6	I/O L39P_6	I/O L39N_6	I/O L38P_6	I/O L38N_6	VCCO_6		GND	GND	GND
N	I/O L35P_6	I/O L35N_6	I/O L34P_6	I/O L34N_6 VREF_6	I/O L33P_6 ◆	I/O L33N_6 ◆	VCCO_6		GND	GND	GND
P	I/O L32P_6 ◆	I/O L32N_6 ◆	GND	I/O L31P_6 ◆	I/O L31N_6 ◆	I/O L28P_6 ◆	VCCO_6		GND	GND	GND
R	I/O L29P_6 ◆	I/O L29N_6 ◆	VCCO_6	I/O L26P_6 ◆	I/O L28N_6 ◆	VCCO_6	VCCINT				
T	I/O L27P_6	I/O L27N_6	I/O L26N_6 ◆	I/O L23P_6	I/O L22P_6	I/O L22N_6	VCCINT	VCCINT	VCCO_5	VCCO_5	VCCO_5
U	VCCAUX	I/O L24P_6	I/O L24N_6 VREF_6	I/O L23N_6	I/O L19P_6	IO VREF_5	I/O	VCCO_5	I/O ◆	I/O	I/O
V	I/O L21P_6	I/O L21N_6	I/O L20P_6	I/O L20N_6	I/O L19N_6	I/O L15P_5	I/O	I/O L24P_5	I/O L27P_5	I/O	I/O L31P_5 D5
W	I/O L17P_6 VREF_6	I/O L17N_6	I/O L16P_6	I/O L16N_6	I/O L09P_5	I/O L15N_5	I/O L19P_5 VREF_5 ◆	I/O L24N_5	I/O L27N_5 VREF_5	I/O L29P_5 VREF_5	I/O L31N_5 D4
Y	I/O	I/O L01P_6 VRN_6	I/O L01N_6 VRP_6	I/O L01N_5 RDWR_B	I/O L09N_5	I/O L16P_5	I/O L19N_5 ◆	VCCO_5	GND	I/O L29N_5	I/O L32P_5 GCLK2
AA	M1	GND	I/O L01P_5 CS_B	I/O L06P_5	I/O L10P_5 VRN_5	I/O L16N_5	I/O L22P_5 ◆	I/O L25P_5	I/O L28P_5 D7	I/O L30P_5	I/O L32N_5 GCLK3
AB	GND	M0	M2	I/O L06N_5	I/O L10N_5 VRP_5	VCCAUX	I/O L22N_5 ◆	I/O L25N_5	I/O L28N_5 D6	I/O L30N_5	IO VREF_5

Bank 7 (rows G–L) · Bank 6 (rows M–T) · Bank 5 (columns 7–11)

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Figure 51: **FG456 Package Footprint (Top View)**

FG676: 676-lead Fine-pitch Ball Grid Array

The 676-lead fine-pitch ball grid array package, FG676, supports five different Spartan-3 devices, including the XC3S1000, XC3S1500, XC3S2000, XC3S4000, and XC3S5000. All five have nearly identical footprints but are slightly different, primarily due to unconnected pins on the XC3S1000 and XC3S1500. For example, because the XC3S1000 has fewer I/O pins, this device has 98 unconnected pins on the FG676 package, labeled as "N.C." In Table 103 and Figure 53, these unconnected pins are indicated with a black diamond symbol (◆). The XC3S1500, however, has only two unconnected pins, also labeled "N.C." in the pinout table but indicated with a black square symbol (■).

All the package pins appear in Table 103 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

If there is a difference between the XC3S1000, XC3S1500, XC3S2000, XC3S4000, and XC3S5000 pinouts, then that difference is highlighted in Table 103. If the table entry is shaded grey, then there is an unconnected pin on either the XC3S1000 or XC3S1500 that maps to a user-I/O pin on the XC3S2000, XC3S4000, and XC3S5000. If the table entry is shaded tan, then the unconnected pin on either the XC3S1000 or XC3S1500 maps to a VREF-type pin on the XC3S2000, XC3S4000, and XC3S5000. If the other VREF pins in the bank all connect to a voltage reference to support a special I/O standard, then also connect the N.C. pin on the XC3S1000 or XC3S1500 to the same VREF voltage. This provides maximum flexibility as you could potentially migrate a design from the XC3S1000 through to the XC3S5000 FPGA without changing the printed circuit board.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

Pinout Table

Table 103: **FG676 Package Pinout**

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
0	IO	IO	IO	IO	IO_L04N_0(3)	A3	I/O
0	IO	IO	IO	IO	IO	A5	I/O
0	IO	IO	IO	IO	IO	A6	I/O
0	IO	IO	IO	IO	IO_L04P_0(3)	C4	I/O
0	N.C. (◆)	IO	IO	IO	IO_L13N_0(3)	C8	I/O
0	IO	IO	IO	IO	IO	C12	I/O
0	IO	IO	IO	IO	IO	E13	I/O
0	IO	IO	IO	IO	IO	H11	I/O
0	IO	IO	IO	IO	IO	H12	I/O
0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	B3	VREF
0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	F7	VREF
0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	G10	VREF
0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	E5	DCI
0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	D5	DCI
0	IO_L05N_0	IO_L05N_0	IO_L05N_0	IO_L05N_0	IO_L05N_0	B4	I/O
0	IO_L05P_0/VREF_0	IO_L05P_0/VREF_0	IO_L05P_0/VREF_0	IO_L05P_0/VREF_0	IO_L05P_0/VREF_0	A4	VREF
0	IO_L06N_0	IO_L06N_0	IO_L06N_0	IO_L06N_0	IO_L06N_0	C5	I/O
0	IO_L06P_0	IO_L06P_0	IO_L06P_0	IO_L06P_0	IO_L06P_0	B5	I/O
0	IO_L07N_0	IO_L07N_0	IO_L07N_0	IO_L07N_0	IO_L07N_0	E6	I/O
0	IO_L07P_0	IO_L07P_0	IO_L07P_0	IO_L07P_0	IO_L07P_0	D6	I/O
0	IO_L08N_0	IO_L08N_0	IO_L08N_0	IO_L08N_0	IO_L08N_0	C6	I/O
0	IO_L08P_0	IO_L08P_0	IO_L08P_0	IO_L08P_0	IO_L08P_0	B6	I/O

FG900: 900-lead Fine-pitch Ball Grid Array

The 900-lead fine-pitch ball grid array package, FG900, supports three different Spartan-3 devices, including the XC3S2000, the XC3S4000, and the XC3S5000. The footprints for the XC3S4000 and XC3S5000 are identical, as shown in Table 107 and Figure 55. The XC3S2000, however, has fewer I/O pins which consequently results in 68 unconnected pins on the FG900 package, labeled as “N.C.” In Table 107 and Figure 55, these unconnected pins are indicated with a black diamond symbol (◆).

All the package pins appear in Table 107 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

If there is a difference between the XC3S2000 pinout and the pinout for the XC3S4000 and XC3S5000, then that difference is highlighted in Table 107. If the table entry is shaded, then there is an unconnected pin on the XC3S2000 that maps to a user-I/O pin on the XC3S4000 and XC3S5000.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

Pinout Table

Table 107: **FG900 Package Pinout**

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
0	IO	IO	E15	I/O
0	IO	IO	K15	I/O
0	IO	IO	D13	I/O
0	IO	IO	K13	I/O
0	IO	IO	G8	I/O
0	IO/VREF_0	IO/VREF_0	F9	VREF
0	IO/VREF_0	IO/VREF_0	C4	VREF
0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	B4	DCI
0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	A4	DCI
0	IO_L02N_0	IO_L02N_0	B5	I/O
0	IO_L02P_0	IO_L02P_0	A5	I/O
0	IO_L03N_0	IO_L03N_0	D5	I/O
0	IO_L03P_0	IO_L03P_0	E6	I/O
0	IO_L04N_0	IO_L04N_0	C6	I/O
0	IO_L04P_0	IO_L04P_0	B6	I/O
0	IO_L05N_0	IO_L05N_0	F6	I/O
0	IO_L05P_0/VREF_0	IO_L05P_0/VREF_0	F7	VREF
0	IO_L06N_0	IO_L06N_0	D7	I/O
0	IO_L06P_0	IO_L06P_0	C7	I/O
0	IO_L07N_0	IO_L07N_0	F8	I/O
0	IO_L07P_0	IO_L07P_0	E8	I/O
0	IO_L08N_0	IO_L08N_0	D8	I/O
0	IO_L08P_0	IO_L08P_0	C8	I/O
0	IO_L09N_0	IO_L09N_0	B8	I/O
0	IO_L09P_0	IO_L09P_0	A8	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
2	IO_L28N_2	IO_L28N_2	M26	I/O
2	IO_L28P_2	IO_L28P_2	N25	I/O
2	IO_L29N_2	IO_L29N_2	N26	I/O
2	IO_L29P_2	IO_L29P_2	N27	I/O
2	IO_L31N_2	IO_L31N_2	N29	I/O
2	IO_L31P_2	IO_L31P_2	N30	I/O
2	IO_L32N_2	IO_L32N_2	P21	I/O
2	IO_L32P_2	IO_L32P_2	P22	I/O
2	IO_L33N_2	IO_L33N_2	P24	I/O
2	IO_L33P_2	IO_L33P_2	P25	I/O
2	IO_L34N_2/VREF_2	IO_L34N_2/VREF_2	P28	VREF
2	IO_L34P_2	IO_L34P_2	P29	I/O
2	IO_L35N_2	IO_L35N_2	R21	I/O
2	IO_L35P_2	IO_L35P_2	R22	I/O
2	IO_L37N_2	IO_L37N_2	R23	I/O
2	IO_L37P_2	IO_L37P_2	R24	I/O
2	IO_L38N_2	IO_L38N_2	R25	I/O
2	IO_L38P_2	IO_L38P_2	R26	I/O
2	IO_L39N_2	IO_L39N_2	R27	I/O
2	IO_L39P_2	IO_L39P_2	R28	I/O
2	IO_L40N_2	IO_L40N_2	R29	I/O
2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	R30	VREF
2	N.C. (◆)	IO_L41N_2	E27	I/O
2	N.C. (◆)	IO_L41P_2	F26	I/O
2	N.C. (◆)	IO_L45N_2	K28	I/O
2	N.C. (◆)	IO_L45P_2	K29	I/O
2	N.C. (◆)	IO_L46N_2	K21	I/O
2	N.C. (◆)	IO_L46P_2	L21	I/O
2	N.C. (◆)	IO_L47N_2	L23	I/O
2	N.C. (◆)	IO_L47P_2	L24	I/O
2	N.C. (◆)	IO_L50N_2	M29	I/O
2	N.C. (◆)	IO_L50P_2	M30	I/O
2	VCCO_2	VCCO_2	M20	VCCO
2	VCCO_2	VCCO_2	N20	VCCO
2	VCCO_2	VCCO_2	P20	VCCO
2	VCCO_2	VCCO_2	L22	VCCO
2	VCCO_2	VCCO_2	J24	VCCO
2	VCCO_2	VCCO_2	N24	VCCO
2	VCCO_2	VCCO_2	G26	VCCO
2	VCCO_2	VCCO_2	E28	VCCO

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
2	VCCO_2	VCCO_2	J28	VCCO
2	VCCO_2	VCCO_2	N28	VCCO
3	IO	IO	AB25	I/O
3	IO_L01N_3/VRP_3	IO_L01N_3/VRP_3	AH30	DCI
3	IO_L01P_3/VRN_3	IO_L01P_3/VRN_3	AH29	DCI
3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	AG28	VREF
3	IO_L02P_3	IO_L02P_3	AG27	I/O
3	IO_L03N_3	IO_L03N_3	AG30	I/O
3	IO_L03P_3	IO_L03P_3	AG29	I/O
3	IO_L04N_3	IO_L04N_3	AF30	I/O
3	IO_L04P_3	IO_L04P_3	AF29	I/O
3	IO_L05N_3	IO_L05N_3	AE26	I/O
3	IO_L05P_3	IO_L05P_3	AF27	I/O
3	IO_L06N_3	IO_L06N_3	AE29	I/O
3	IO_L06P_3	IO_L06P_3	AE28	I/O
3	IO_L07N_3	IO_L07N_3	AD28	I/O
3	IO_L07P_3	IO_L07P_3	AD27	I/O
3	IO_L08N_3	IO_L08N_3	AD30	I/O
3	IO_L08P_3	IO_L08P_3	AD29	I/O
3	IO_L09N_3	IO_L09N_3	AC24	I/O
3	IO_L09P_3/VREF_3	IO_L09P_3/VREF_3	AD25	VREF
3	IO_L10N_3	IO_L10N_3	AC26	I/O
3	IO_L10P_3	IO_L10P_3	AC25	I/O
3	IO_L11N_3	IO_L11N_3	AC28	I/O
3	IO_L11P_3	IO_L11P_3	AC27	I/O
3	IO_L13N_3/VREF_3	IO_L13N_3/VREF_3	AC30	VREF
3	IO_L13P_3	IO_L13P_3	AC29	I/O
3	IO_L14N_3	IO_L14N_3	AB27	I/O
3	IO_L14P_3	IO_L14P_3	AB26	I/O
3	IO_L15N_3	IO_L15N_3	AB30	I/O
3	IO_L15P_3	IO_L15P_3	AB29	I/O
3	IO_L16N_3	IO_L16N_3	AA22	I/O
3	IO_L16P_3	IO_L16P_3	AB23	I/O
3	IO_L17N_3	IO_L17N_3	AA25	I/O
3	IO_L17P_3/VREF_3	IO_L17P_3/VREF_3	AA24	VREF
3	IO_L19N_3	IO_L19N_3	AA29	I/O
3	IO_L19P_3	IO_L19P_3	AA28	I/O
3	IO_L20N_3	IO_L20N_3	Y21	I/O
3	IO_L20P_3	IO_L20P_3	AA21	I/O
3	IO_L21N_3	IO_L21N_3	Y24	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
3	N.C. (◆)	IO_L50P_3	V26	I/O
3	VCCO_3	VCCO_3	U20	VCCO
3	VCCO_3	VCCO_3	V20	VCCO
3	VCCO_3	VCCO_3	W20	VCCO
3	VCCO_3	VCCO_3	Y22	VCCO
3	VCCO_3	VCCO_3	V24	VCCO
3	VCCO_3	VCCO_3	AB24	VCCO
3	VCCO_3	VCCO_3	AD26	VCCO
3	VCCO_3	VCCO_3	V28	VCCO
3	VCCO_3	VCCO_3	AB28	VCCO
3	VCCO_3	VCCO_3	AF28	VCCO
4	IO	IO	AA16	I/O
4	IO	IO	AG18	I/O
4	IO	IO	AA18	I/O
4	IO	IO	AE22	I/O
4	IO	IO	AD23	I/O
4	IO	IO	AH27	I/O
4	IO/VREF_4	IO/VREF_4	AF16	VREF
4	IO/VREF_4	IO/VREF_4	AK28	VREF
4	IO_L01N_4/VRP_4	IO_L01N_4/VRP_4	AJ27	DCI
4	IO_L01P_4/VRN_4	IO_L01P_4/VRN_4	AK27	DCI
4	IO_L02N_4	IO_L02N_4	AJ26	I/O
4	IO_L02P_4	IO_L02P_4	AK26	I/O
4	IO_L03N_4	IO_L03N_4	AG26	I/O
4	IO_L03P_4	IO_L03P_4	AF25	I/O
4	IO_L04N_4	IO_L04N_4	AD24	I/O
4	IO_L04P_4	IO_L04P_4	AC23	I/O
4	IO_L05N_4	IO_L05N_4	AE23	I/O
4	IO_L05P_4	IO_L05P_4	AF23	I/O
4	IO_L06N_4/VREF_4	IO_L06N_4/VREF_4	AG23	VREF
4	IO_L06P_4	IO_L06P_4	AH23	I/O
4	IO_L07N_4	IO_L07N_4	AJ23	I/O
4	IO_L07P_4	IO_L07P_4	AK23	I/O
4	IO_L08N_4	IO_L08N_4	AB22	I/O
4	IO_L08P_4	IO_L08P_4	AC22	I/O
4	IO_L09N_4	IO_L09N_4	AF22	I/O
4	IO_L09P_4	IO_L09P_4	AG22	I/O
4	IO_L10N_4	IO_L10N_4	AJ22	I/O
4	IO_L10P_4	IO_L10P_4	AK22	I/O
4	IO_L11N_4	IO_L11N_4	AD21	I/O

Right Half of FG900 Package (Top View)

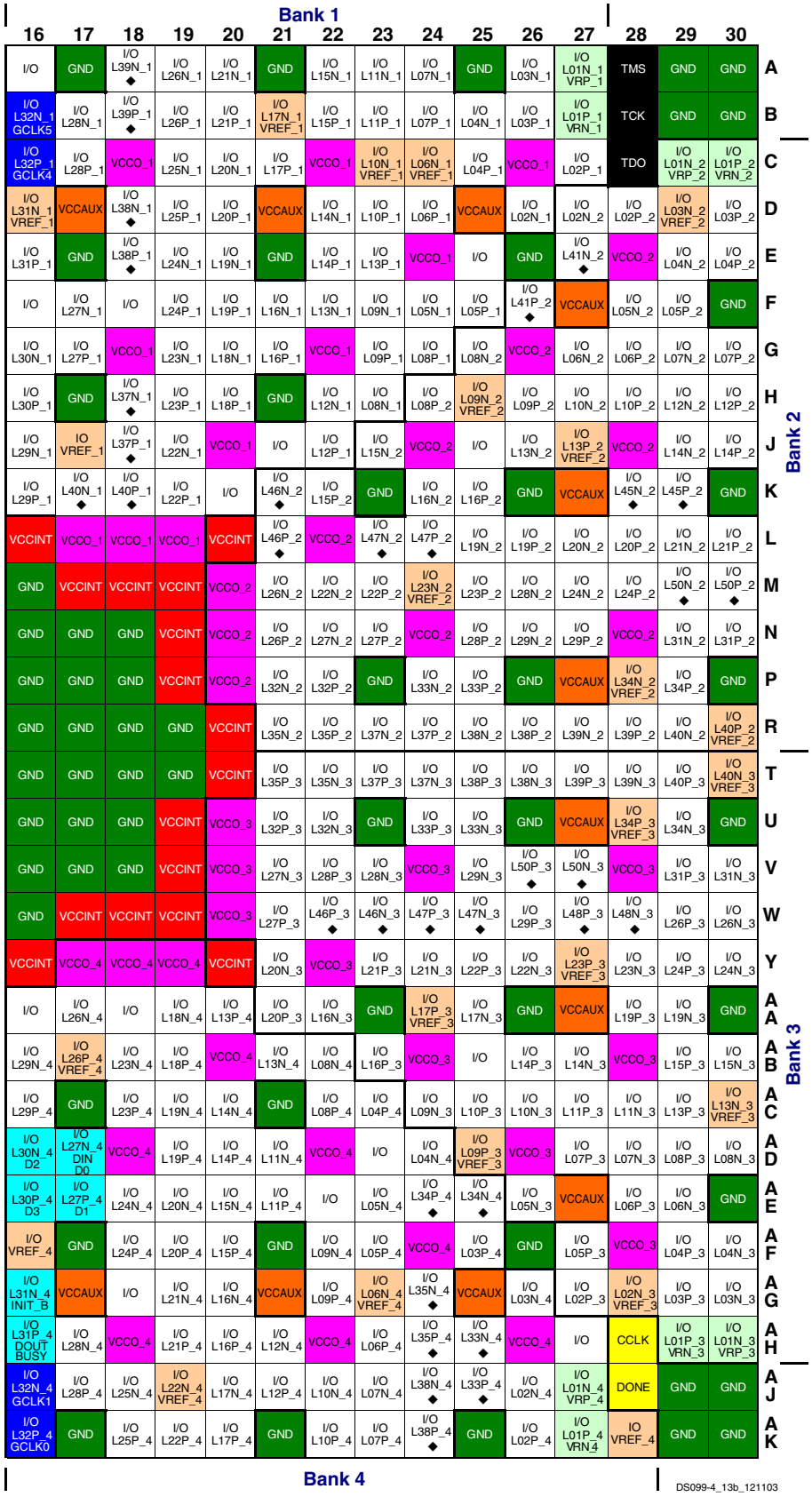

Figure 56: FG900 Package Footprint (Top View) Continued

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
1	VCCO_1	VCCO_1	M22	VCCO
2	IO	IO	G33	I/O
2	IO	IO	G34	I/O
2	IO	IO	U25	I/O
2	IO	IO	U26	I/O
2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	C33	DCI
2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	C34	DCI
2	IO_L02N_2	IO_L02N_2	D33	I/O
2	IO_L02P_2	IO_L02P_2	D34	I/O
2	IO_L03N_2/VREF_2	IO_L03N_2/VREF_2	E32	VREF
2	IO_L03P_2	IO_L03P_2	E33	I/O
2	IO_L04N_2	IO_L04N_2	F31	I/O
2	IO_L04P_2	IO_L04P_2	F32	I/O
2	IO_L05N_2	IO_L05N_2	G29	I/O
2	IO_L05P_2	IO_L05P_2	G30	I/O
2	IO_L06N_2	IO_L06N_2	H29	I/O
2	IO_L06P_2	IO_L06P_2	H30	I/O
2	IO_L07N_2	IO_L07N_2	H33	I/O
2	IO_L07P_2	IO_L07P_2	H34	I/O
2	IO_L08N_2	IO_L08N_2	J28	I/O
2	IO_L08P_2	IO_L08P_2	J29	I/O
2	IO_L09N_2/VREF_2	IO_L09N_2/VREF_2	H31	VREF
2	IO_L09P_2	IO_L09P_2	J31	I/O
2	IO_L10N_2	IO_L10N_2	J32	I/O
2	IO_L10P_2	IO_L10P_2	J33	I/O
2	IO_L11N_2	IO_L11N_2	J27	I/O
2	IO_L11P_2	IO_L11P_2	K26	I/O
2	IO_L12N_2	IO_L12N_2	K27	I/O
2	IO_L12P_2	IO_L12P_2	K28	I/O
2	IO_L13N_2	IO_L13N_2	K29	I/O
2	IO_L13P_2/VREF_2	IO_L13P_2/VREF_2	K30	VREF
2	IO_L14N_2	IO_L14N_2	K31	I/O
2	IO_L14P_2	IO_L14P_2	K32	I/O
2	IO_L15N_2	IO_L15N_2	K33	I/O
2	IO_L15P_2	IO_L15P_2	K34	I/O
2	IO_L16N_2	IO_L16N_2	L25	I/O
2	IO_L16P_2	IO_L16P_2	L26	I/O
2	N.C. (◆)	IO_L17N_2	L28	I/O
2	N.C. (◆)	IO_L17P_2/ VREF_2	L29	VREF

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
3	IO_L24P_3	IO_L24P_3	AC26	I/O
3	IO_L26N_3	IO_L26N_3	AA28	I/O
3	IO_L26P_3	IO_L26P_3	AA27	I/O
3	IO_L27N_3	IO_L27N_3	AA30	I/O
3	IO_L27P_3	IO_L27P_3	AA29	I/O
3	IO_L28N_3	IO_L28N_3	AA32	I/O
3	IO_L28P_3	IO_L28P_3	AA31	I/O
3	IO_L29N_3	IO_L29N_3	AA34	I/O
3	IO_L29P_3	IO_L29P_3	AA33	I/O
3	IO_L30N_3	IO_L30N_3	Y29	I/O
3	IO_L30P_3	IO_L30P_3	Y28	I/O
3	IO_L31N_3	IO_L31N_3	Y32	I/O
3	IO_L31P_3	IO_L31P_3	Y31	I/O
3	IO_L32N_3	IO_L32N_3	Y34	I/O
3	IO_L32P_3	IO_L32P_3	Y33	I/O
3	IO_L33N_3	IO_L33N_3	W25	I/O
3	IO_L33P_3	IO_L33P_3	Y26	I/O
3	IO_L34N_3	IO_L34N_3	W29	I/O
3	IO_L34P_3/VREF_3	IO_L34P_3/VREF_3	W28	VREF
3	IO_L35N_3	IO_L35N_3	W33	I/O
3	IO_L35P_3	IO_L35P_3	W32	I/O
3	IO_L37N_3	IO_L37N_3	V28	I/O
3	IO_L37P_3	IO_L37P_3	V27	I/O
3	IO_L38N_3	IO_L38N_3	V30	I/O
3	IO_L38P_3	IO_L38P_3	V29	I/O
3	IO_L39N_3	IO_L39N_3	V32	I/O
3	IO_L39P_3	IO_L39P_3	V31	I/O
3	IO_L40N_3/VREF_3	IO_L40N_3/VREF_3	V34	VREF
3	IO_L40P_3	IO_L40P_3	V33	I/O
3	N.C. (◆)	IO_L41N_3	AH32	I/O
3	N.C. (◆)	IO_L41P_3	AH31	I/O
3	N.C. (◆)	IO_L44N_3	AD29	I/O
3	N.C. (◆)	IO_L44P_3	AD28	I/O
3	IO_L45N_3	IO_L45N_3	AC34	I/O
3	IO_L45P_3	IO_L45P_3	AC33	I/O
3	IO_L46N_3	IO_L46N_3	AB28	I/O
3	IO_L46P_3	IO_L46P_3	AB27	I/O
3	IO_L47N_3	IO_L47N_3	AB32	I/O
3	IO_L47P_3	IO_L47P_3	AB31	I/O
3	IO_L48N_3	IO_L48N_3	AA24	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
N/A	GND	GND	J22	GND
N/A	GND	GND	J30	GND
N/A	GND	GND	J34	GND
N/A	GND	GND	J5	GND
N/A	GND	GND	K10	GND
N/A	GND	GND	K25	GND
N/A	GND	GND	L3	GND
N/A	GND	GND	L32	GND
N/A	GND	GND	N1	GND
N/A	GND	GND	N17	GND
N/A	GND	GND	N18	GND
N/A	GND	GND	N26	GND
N/A	GND	GND	N30	GND
N/A	GND	GND	N34	GND
N/A	GND	GND	N5	GND
N/A	GND	GND	N9	GND
N/A	GND	GND	P14	GND
N/A	GND	GND	P15	GND
N/A	GND	GND	P16	GND
N/A	GND	GND	P17	GND
N/A	GND	GND	P18	GND
N/A	GND	GND	P19	GND
N/A	GND	GND	P20	GND
N/A	GND	GND	P21	GND
N/A	GND	GND	R14	GND
N/A	GND	GND	R15	GND
N/A	GND	GND	R16	GND
N/A	GND	GND	R17	GND
N/A	GND	GND	R18	GND
N/A	GND	GND	R19	GND
N/A	GND	GND	R20	GND
N/A	GND	GND	R21	GND
N/A	GND	GND	T1	GND
N/A	GND	GND	T14	GND
N/A	GND	GND	T15	GND
N/A	GND	GND	T16	GND
N/A	GND	GND	T17	GND
N/A	GND	GND	T18	GND
N/A	GND	GND	T19	GND
N/A	GND	GND	T20	GND