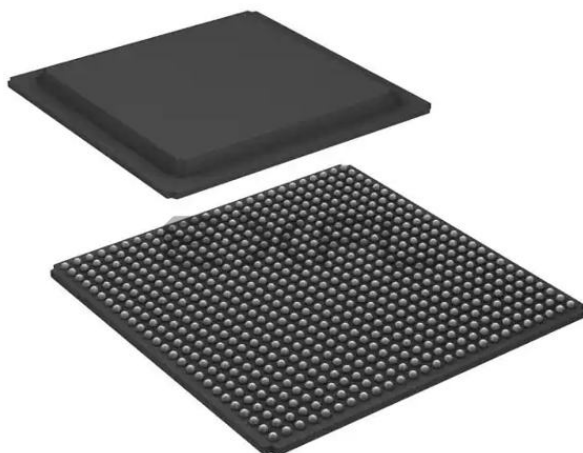




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	6912
Number of Logic Elements/Cells	62208
Total RAM Bits	1769472
Number of I/O	489
Number of Gates	4000000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s4000-5fg676c

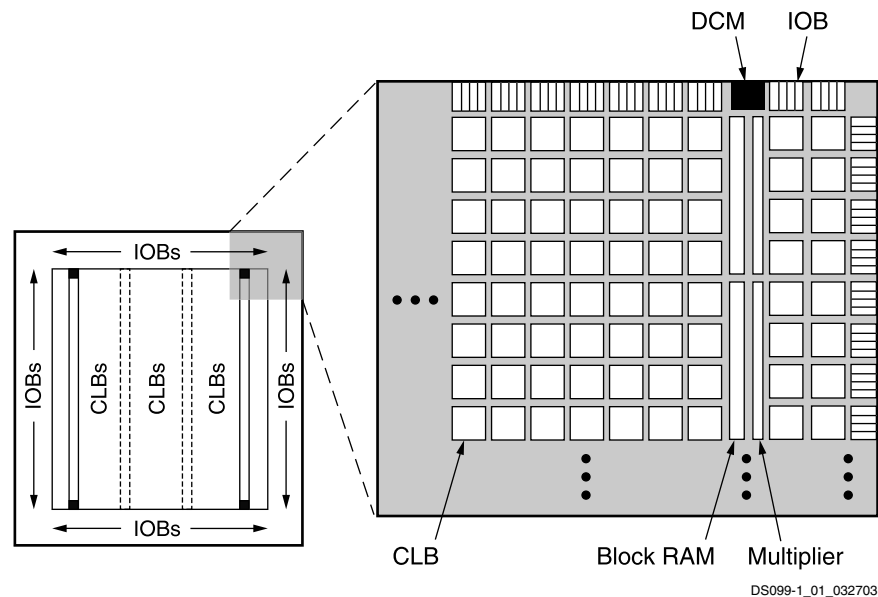
Architectural Overview

The Spartan-3 family architecture consists of five fundamental programmable functional elements:

- Configurable Logic Blocks (CLBs) contain RAM-based Look-Up Tables (LUTs) to implement logic and storage elements that can be used as flip-flops or latches. CLBs can be programmed to perform a wide variety of logical functions as well as to store data.
- Input/Output Blocks (IOBs) control the flow of data between the I/O pins and the internal logic of the device. Each IOB supports bidirectional data flow plus 3-state operation. Twenty-six different signal standards, including eight high-performance differential standards, are available as shown in Table 2. Double Data-Rate (DDR) registers are included. The Digitally Controlled Impedance (DCI) feature provides automatic on-chip terminations, simplifying board designs.
- Block RAM provides data storage in the form of 18-Kbit dual-port blocks.
- Multiplier blocks accept two 18-bit binary numbers as inputs and calculate the product.
- Digital Clock Manager (DCM) blocks provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase shifting clock signals.

These elements are organized as shown in Figure 1. A ring of IOBs surrounds a regular array of CLBs. The XC3S50 has a single column of block RAM embedded in the array. Those devices ranging from the XC3S200 to the XC3S2000 have two columns of block RAM. The XC3S4000 and XC3S5000 devices have four RAM columns. Each column is made up of several 18-Kbit RAM blocks; each block is associated with a dedicated multiplier. The DCMs are positioned at the ends of the outer block RAM columns.

The Spartan-3 family features a rich network of traces and switches that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.



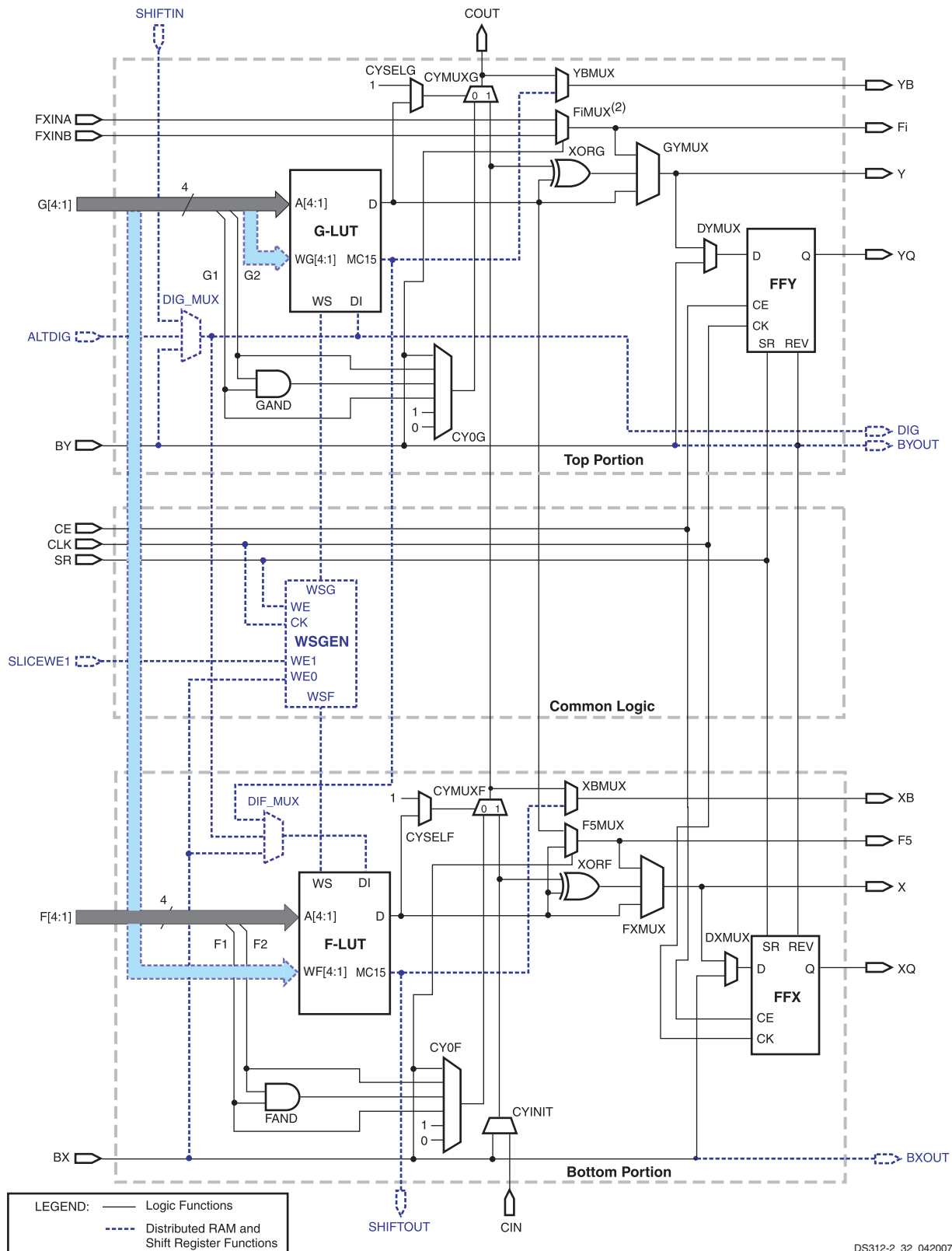
Notes:

1. The two additional block RAM columns of the XC3S4000 and XC3S5000 devices are shown with dashed lines. The XC3S50 has only the block RAM column on the far left.

Figure 1: Spartan-3 Family Architecture

Configuration

Spartan-3 FPGAs are programmed by loading configuration data into robust reprogrammable static CMOS configuration latches (CCLs) that collectively control all functional elements and routing resources. Before powering on the FPGA, configuration data is stored externally in a PROM or some other nonvolatile medium either on or off the board. After applying



DS312-2_32_042007

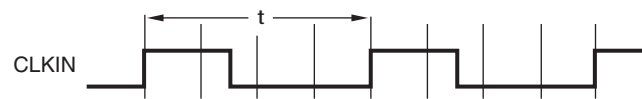
Notes:

- Options to invert signal polarity as well as other options that enable lines for various functions are not shown.
- The index i can be 6, 7, or 8, depending on the slice. In this position, the upper right-hand slice has an F8MUX, and the upper left-hand slice has an F7MUX. The lower right-hand and left-hand slices both have an F6MUX.

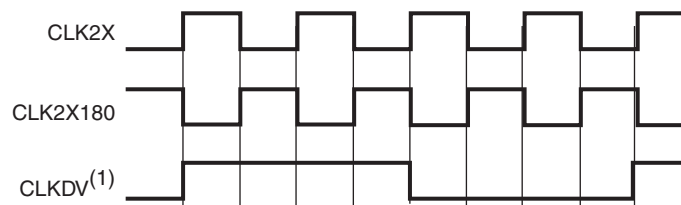
Figure 12: Simplified Diagram of the Left-Hand SLICEM

Phase: 0° 90° 180° 270° 0° 90° 180° 270° 0°

Input Signal (40% Duty Cycle)

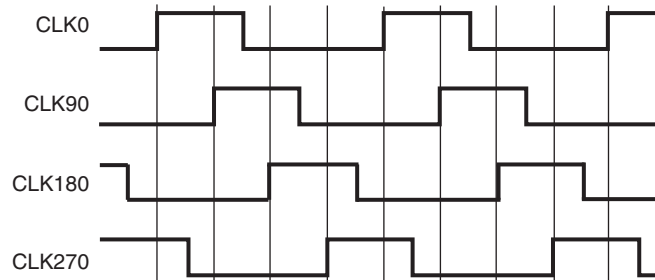


Output Signal - Duty Cycle is Always Corrected

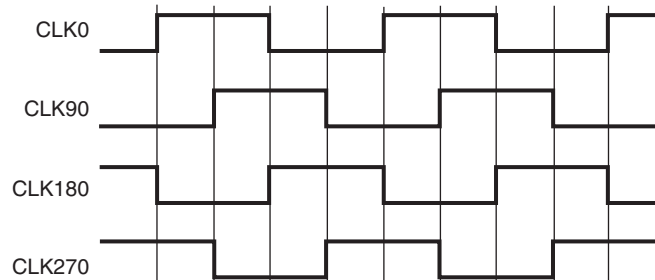


Output Signal - Attribute Corrects Duty Cycle

DUTY_CYCLE_CORRECTION = FALSE



DUTY_CYCLE_CORRECTION = TRUE



DS099-2_10_051907

Figure 22: Characteristics of the DLL Clock Outputs

Digital Frequency Synthesizer (DFS)

The DFS component generates clock signals the frequency of which is a product of the clock frequency at the CLKIN input and a ratio of two user-determined integers. Because of the wide range of possible output frequencies such a ratio permits, the DFS feature provides still further flexibility than the DLL's basic synthesis options as described in the preceding section. The DFS component's two dedicated outputs, CLKFX and CLKFX180, are defined in Table 19.

The signal at the CLKFX180 output is essentially an inversion of the CLKFX signal. These two outputs always exhibit a 50% duty cycle. This is true even when the CLKIN signal does not. These DFS clock outputs are driven at the same time as the DLL's seven clock outputs.

The numerator of the ratio is the integer value assigned to the attribute CLKFX_MULTIPLY and the denominator is the integer value assigned to the attribute CLKFX_DIVIDE. These attributes are described in Table 18.

Configuration

Spartan-3 devices are configured by loading application specific configuration data into the internal configuration memory. Configuration is carried out using a subset of the device pins, some of which are "Dedicated" to one function only, while others, indicated by the term "Dual-Purpose", can be re-used as general-purpose User I/Os once configuration is complete.

Depending on the system design, several configuration modes are supported, selectable via mode pins. The mode pins M0, M1, and M2 are Dedicated pins. The mode pin settings are shown in [Table 26](#).

Table 26: Spartan-3 FPGAs Configuration Mode Pin Settings

Configuration Mode ⁽¹⁾	M0	M1	M2	Synchronizing Clock	Data Width	Serial DOUT ⁽²⁾
Master Serial	0	0	0	CCLK Output	1	Yes
Slave Serial	1	1	1	CCLK Input	1	Yes
Master Parallel	1	1	0	CCLK Output	8	No
Slave Parallel	0	1	1	CCLK Input	8	No
JTAG	1	0	1	TCK Input	1	No

Notes:

1. The voltage levels on the M0, M1, and M2 pins select the configuration mode.
2. The daisy chain is possible only in the Serial modes when DOUT is used.

The HSWAP_EN input pin defines whether the I/O pins that are not actively used during configuration have pull-up resistors during configuration. By default, HSWAP_EN is tied High (via an internal pull-up resistor if left floating) which shuts off the pull-up resistors on the user I/O pins during configuration. When HSWAP_EN is tied Low, user I/Os have pull-ups during configuration. The Dedicated configuration pins (CCLK, DONE, PROG_B, M2, M1, M0, HSWAP_EN) and the JTAG pins (TDI, TMS, TCK, and TDO) always have a pull-up resistor to VCCAUX during configuration, regardless of the value on the HSWAP_EN pin. Similarly, the dual-purpose INIT_B pin has an internal pull-up resistor to VCCO_4 or VCCO_BOTTOM, depending on the package style.

Depending on the chosen configuration mode, the FPGA either generates a CCLK output, or CCLK is an input accepting an externally generated clock.

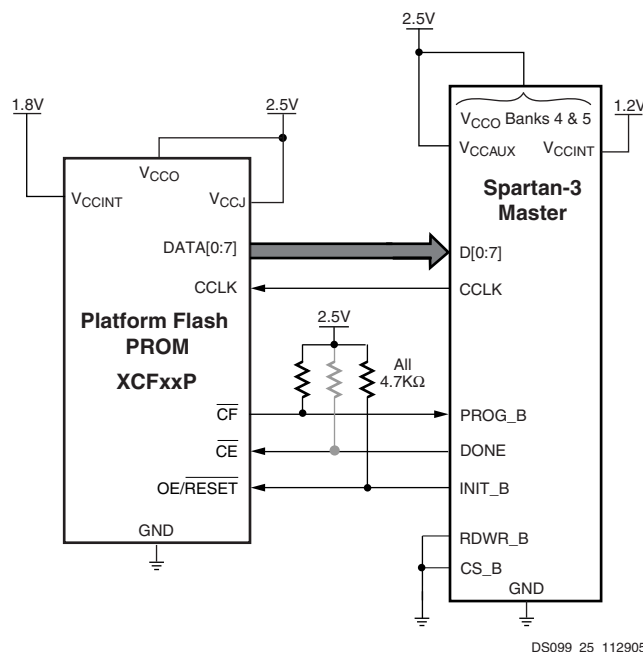
A persist option is available which can be used to force the configuration pins to retain their configuration function even after device configuration is complete. If the persist option is not selected then the configuration pins with the exception of CCLK, PROG_B, and DONE can be used as user I/O in normal operation. The persist option does not apply to the boundary-scan related pins. The persist feature is valuable in applications that readback configuration data after entering the User mode.

[Table 27](#) lists the total number of bits required to configure each FPGA as well as the PROMs suitable for storing those bits. See [DS123: Platform Flash In-System Programmable Configuration PROMs](#) data sheet for more information.

Table 27: Spartan-3 FPGA Configuration Data

Device	File Sizes	Xilinx Platform Flash PROM	
		Serial Configuration	Parallel Configuration
XC3S50	439,264	XCF01S	XCF08P
XC3S200	1,047,616	XCF01S	XCF08P
XC3S400	1,699,136	XCF02S	XCF08P
XC3S1000	3,223,488	XCF04S	XCF08P
XC3S1500	5,214,784	XCF08P	XCF08P
XC3S2000	7,673,024	XCF08P	XCF08P
XC3S4000	11,316,864	XCF16P	XCF16P
XC3S5000	13,271,936	XCF16P	XCF16P

The maximum bitstream length that Spartan-3 FPGAs support in serial daisy-chains is 4,294,967,264 bits (4 Gbits), roughly equivalent to a daisy-chain with 323 XC3S5000 FPGAs. This is a limit only for serial daisy-chains where configuration data is passed via the FPGA's DOUT pin. There is no such limit for JTAG chains.



Notes:

1. There are two ways to use the DONE line. First, one may set the BitGen option DriveDone to "Yes" only for the last FPGA to be configured in the chain shown above (or for the single FPGA as may be the case). This enables the DONE pin to drive High; thus, no pull-up resistor is necessary. DriveDone is set to "No" for the remaining FPGAs in the chain. Second, DriveDone can be set to "No" for all FPGAs. Then all DONE lines are open-drain and require the pull-up resistor shown in grey. In most cases, a value between 3.3KΩ to 4.7KΩ is sufficient. However, when using DONE synchronously with a long chain of FPGAs, cumulative capacitance may necessitate lower resistor values (e.g. down to 330Ω) in order to ensure a rise time within one clock cycle.

Figure 28: Connection Diagram for Master Parallel Configuration

Master Parallel Mode

In this mode, the FPGA configures from byte-wide data, and the FPGA supplies the CCLK configuration clock. In Master configuration modes, CCLK behaves as a bidirectional I/O pin. Timing is similar to the Slave Parallel mode except that CCLK is supplied by the FPGA. The device connections are shown in Figure 28.

Boundary-Scan (JTAG) Mode

In Boundary-Scan mode, dedicated pins are used for configuring the FPGA. The configuration is done entirely through the IEEE 1149.1 Test Access Port (TAP). FPGA configuration using the Boundary-Scan mode is compatible with the IEEE Std 1149.1-1993 standard and IEEE Std 1532 for In-System Configurable (ISC) devices.

Configuration through the boundary-scan port is always available, regardless of the selected configuration mode. In some cases, however, the mode pin setting may affect proper programming of the device due to various interactions. For example, if the mode pins are set to Master Serial or Master Parallel mode, and the associated PROM is already programmed with a valid configuration image, then there is potential for configuration interference between the JTAG and PROM data. Selecting the Boundary-Scan mode disables the other modes and is the most reliable mode when programming via JTAG.

Configuration Sequence

The configuration of Spartan-3 devices is a three-stage process that occurs after Power-On Reset or the assertion of PROG_B. POR occurs after the V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 4 supplies have reached their respective maximum input threshold levels (see Table 29, page 59). After POR, the three-stage process begins.

First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process. A flow diagram for the configuration sequence of the Serial and Parallel modes is shown in Figure 29. The flow diagram for the Boundary-Scan configuration sequence appears in Figure 30.

Table 35: Recommended Operating Conditions for User I/Os Using Single-Ended Standards

Signal Standard (IOSTANDARD)	V _{CCO}			V _{REF}			V _{IL}	V _{IH}
	Min (V)	Nom (V)	Max (V)	Min (V)	Nom (V)	Max (V)	Max (V)	Min (V)
GTL ⁽³⁾	—	—	—	0.74	0.8	0.86	V _{REF} – 0.05	V _{REF} + 0.05
GTL_DCI	—	1.2	—	0.74	0.8	0.86	V _{REF} – 0.05	V _{REF} + 0.05
GTLP ⁽³⁾	—	—	—	0.88	1	1.12	V _{REF} – 0.1	V _{REF} + 0.1
GTLP_DCI	—	1.5	—	0.88	1	1.12	V _{REF} – 0.1	V _{REF} + 0.1
HSLVDCI_15	1.4	1.5	1.6	—	0.75	—	V _{REF} – 0.1	V _{REF} + 0.1
HSLVDCI_18	1.7	1.8	1.9	—	0.9	—	V _{REF} – 0.1	V _{REF} + 0.1
HSLVDCI_25	2.3	2.5	2.7	—	1.25	—	V _{REF} – 0.1	V _{REF} + 0.1
HSLVDCI_33	3.0	3.3	3.465	—	1.65	—	V _{REF} – 0.1	V _{REF} + 0.1
HSTL_I, HSTL_I_DCI	1.4	1.5	1.6	0.68	0.75	0.9	V _{REF} – 0.1	V _{REF} + 0.1
HSTL_III, HSTL_III_DCI	1.4	1.5	1.6	—	0.9	—	V _{REF} – 0.1	V _{REF} + 0.1
HSTL_I_18, HSTL_I_DCI_18	1.7	1.8	1.9	0.8	0.9	1.1	V _{REF} – 0.1	V _{REF} + 0.1
HSTL_II_18, HSTL_II_DCI_18	1.7	1.8	1.9	—	0.9	—	V _{REF} – 0.1	V _{REF} + 0.1
HSTL_III_18, HSTL_III_DCI_18	1.7	1.8	1.9	—	1.1	—	V _{REF} – 0.1	V _{REF} + 0.1
LVC MOS12	1.14	1.2	1.3	—	—	—	0.37V _{CCO}	0.58V _{CCO}
LVC MOS15, LVDCI_15, LVDCI_DV2_15	1.4	1.5	1.6	—	—	—	0.30V _{CCO}	0.70V _{CCO}
LVC MOS18, LVDCI_18, LVDCI_DV2_18	1.7	1.8	1.9	—	—	—	0.30V _{CCO}	0.70V _{CCO}
LVC MOS25 ^(4,5) , LVDCI_25, LVDCI_DV2_25 ⁽⁴⁾	2.3	2.5	2.7	—	—	—	0.7	1.7
LVC MOS33, LVDCI_33, LVDCI_DV2_33 ⁽⁴⁾	3.0	3.3	3.465	—	—	—	0.8	2.0
LVTTL	3.0	3.3	3.465	—	—	—	0.8	2.0
PCI33_3 ⁽⁷⁾	3.0	3.3	3.465	—	—	—	0.30V _{CCO}	0.50V _{CCO}
SSTL18_I, SSTL18_I_DCI	1.7	1.8	1.9	0.833	0.900	0.969	V _{REF} – 0.125	V _{REF} + 0.125
SSTL18_II	1.7	1.8	1.9	0.833	0.900	0.969	V _{REF} – 0.125	V _{REF} + 0.125
SSTL2_I, SSTL2_I_DCI	2.3	2.5	2.7	1.15	1.25	1.35	V _{REF} – 0.15	V _{REF} + 0.15
SSTL2_II, SSTL2_II_DCI	2.3	2.5	2.7	1.15	1.25	1.35	V _{REF} – 0.15	V _{REF} + 0.15

Notes:

- Descriptions of the symbols used in this table are as follows:
V_{CCO} – the supply voltage for output drivers as well as LVC MOS, LVTTL, and PCI inputs
V_{REF} – the reference voltage for setting the input switching threshold
V_{IL} – the input voltage that indicates a Low logic level
V_{IH} – the input voltage that indicates a High logic level
- For device operation, the maximum signal voltage (V_{IH} max) may be as high as V_{IN} max. See [Table 28](#).
- Because the GTL and GTLP standards employ open-drain output buffers, V_{CCO} lines do not supply current to the I/O circuit, rather this current is provided using an external pull-up resistor connected from the I/O pin to a termination voltage (V_{TT}). Nevertheless, the voltage applied to the associated V_{CCO} lines must always be at or above V_{TT} and I/O pad voltages.
- There is approximately 100 mV of hysteresis on inputs using LVC MOS25 or LVC MOS33 standards.
- All dedicated pins (M0-M2, CCLK, PROG_B, DONE, HSWAP_EN, TCK, TDI, TDO, and TMS) use the LVC MOS standard and draw power from the V_{CCAUX} rail (2.5V). The dual-purpose configuration pins (DIN/D0, D1-D7, CS_B, RDWR_B, BUSY/DOUT, and INIT_B) use the LVC MOS standard before the user mode. For these pins, apply 2.5V to the V_{CCO} Bank 4 and V_{CCO} Bank 5 rails at power-on and throughout configuration. For information concerning the use of 3.3V signals, see [3.3V-Tolerant Configuration Interface, page 47](#).
- The Global Clock Inputs (GCLK0-GCLK7) are dual-purpose pins to which any signal standard can be assigned.
- For more information, see [XAPP457](#).

Table 36: DC Characteristics of User I/Os Using Single-Ended Standards

Signal Standard (IOSTANDARD) and Current Drive Attribute (mA)		Test Conditions		Logic Level Characteristics	
		I _{OL} (mA)	I _{OH} (mA)	V _{OL} Max (V)	V _{OH} Min (V)
GTL		32	–	0.4	–
GTL_DCI		Note 3	Note 3		
GTLP		36	–	0.6	–
GTLP_DCI		Note 3	Note 3		
HSLVDCI_15		Note 3	Note 3	0.4	V _{CCO} – 0.4
HSLVDCI_18					
HSLVDCI_25					
HSLVDCI_33					
HSTL_I		8	–8	0.4	V _{CCO} – 0.4
HSTL_I_DCI		Note 3	Note 3		
HSTL_III		24	–8	0.4	V _{CCO} – 0.4
HSTL_III_DCI		Note 3	Note 3		
HSTL_I_18		8	–8	0.4	V _{CCO} – 0.4
HSTL_I_DCI_18		Note 3	Note 3		
HSTL_II_18		16	–16	0.4	V _{CCO} – 0.4
HSTL_II_DCI_18		Note 3	Note 3		
HSTL_III_18		24	–8	0.4	V _{CCO} – 0.4
HSTL_III_DCI_18		Note 3	Note 3		
LVCMOS12 ⁽⁴⁾	2	2	–2	0.4	V _{CCO} – 0.4
	4	4	–4		
	6	6	–6		
LVCMOS15 ⁽⁴⁾	2	2	–2	0.4	V _{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
LVDCI_15, LVDCI_DV2_15		Note 3	Note 3		
LVCMOS18 ⁽⁴⁾	2	2	–2	0.4	V _{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
LVDCI_18, LVDCI_DV2_18		Note 3	Note 3		
LVCMOS25 ^(4,5)	2	2	–2	0.4	V _{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24	24	–24		
LVDCI_25, LVDCI_DV2_25		Note 3	Note 3		

I/O Timing

Table 40: Pin-to-Pin Clock-to-Output Times for the IOB Output Path

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max ⁽²⁾	Max ⁽²⁾	
Clock-to-Output Times						
T _{ICKOFDCM}	When reading from the Output Flip-Flop (OFF), the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is in use.	LVCMOS25 ⁽³⁾ , 12 mA output drive, Fast slew rate, with DCM ⁽⁴⁾	XC3S50	2.04	2.35	ns
			XC3S200	1.45	1.75	ns
			XC3S400	1.45	1.75	ns
			XC3S1000	2.07	2.39	ns
			XC3S1500	2.05	2.36	ns
			XC3S2000	2.03	2.34	ns
			XC3S4000	1.94	2.24	ns
			XC3S5000	2.00	2.30	ns
T _{ICKOF}	When reading from OFF, the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is not in use.	LVCMOS25 ⁽³⁾ , 12 mA output drive, Fast slew rate, without DCM	XC3S50	3.70	4.24	ns
			XC3S200	3.89	4.46	ns
			XC3S400	3.91	4.48	ns
			XC3S1000	4.00	4.59	ns
			XC3S1500	4.07	4.66	ns
			XC3S2000	4.19	4.80	ns
			XC3S4000	4.44	5.09	ns
			XC3S5000	4.38	5.02	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32 and Table 35.
2. For minimums, use the values reported by the Xilinx timing analyzer.
3. This clock-to-output time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or a standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. If the former is true, add the appropriate Input adjustment from Table 44. If the latter is true, add the appropriate Output adjustment from Table 47.
4. DCM output jitter is included in all measurements.

Table 56: Block RAM Timing

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T _{BCKO}	When reading from the Block RAM, the time from the active transition at the CLK input to data appearing at the DOUT output	–	2.09	–	2.40	ns
Setup Times						
T _{BDCK}	Time from the setup of data at the DIN inputs to the active transition at the CLK input of the Block RAM	0.43	–	0.49	–	ns
Hold Times						
T _{BCKD}	Time from the active transition at the Block RAM's CLK input to the point where data is last held at the DIN inputs	0	–	0	–	ns
Clock Timing						
T _{BPWH}	Block RAM CLK signal High pulse width	1.19	∞	1.37	∞	ns
T _{BPWL}	Block RAM CLK signal Low pulse width	1.19	∞	1.37	∞	ns

Notes:

- The numbers in this table are based on the operating conditions set forth in [Table 32](#).
- For minimums, use the values reported by the Xilinx timing analyzer.

Clock Distribution Switching Characteristics

Table 57: Clock Distribution Switching Characteristics

Description	Symbol	Maximum		Units
		Speed Grade		
		-5	-4	
Global clock buffer (BUFG, BUFGMUX, BUFGCE) I-input to O-output delay	T _{GIO}	0.36	0.41	ns
Global clock multiplexer (BUFGMUX) select S-input setup to I0- and I1-inputs. Same as BUFGCE enable CE-input	T _{GSI}	0.53	0.60	ns

Notes:

- For minimums, use the values reported by the Xilinx timing analyzer.

Table 70: Spartan-3 FPGA Pin Definitions

Pin Name	Direction	Description
I/O: General-purpose I/O pins		
I/O	User-defined as input, output, bidirectional, three-state output, open-drain output, open-source output	User I/O: Unrestricted single-ended user-I/O pin. Supports all I/O standards except the differential standards.
I/O_Lxxy_#	User-defined as input, output, bidirectional, three-state output, open-drain output, open-source output	User I/O, Half of Differential Pair: Unrestricted single-ended user-I/O pin or half of a differential pair. Supports all I/O standards including the differential standards.
DUAL: Dual-purpose configuration pins		
IO_Lxxy_#/DIN/D0, IO_Lxxy_#/D1, IO_Lxxy_#/D2, IO_Lxxy_#/D3, IO_Lxxy_#/D4, IO_Lxxy_#/D5, IO_Lxxy_#/D6, IO_Lxxy_#/D7	Input during configuration Possible bidirectional I/O after configuration if SelectMap port is retained Otherwise, user I/O after configuration	Configuration Data Port: In Parallel (SelectMAP) modes, D0-D7 are byte-wide configuration data pins. These pins become user I/Os after configuration unless the SelectMAP port is retained via the Persist bitstream option. In Serial modes, DIN (D0) serves as the single configuration data input. This pin becomes a user I/O after configuration unless retained by the Persist bitstream option.
IO_Lxxy_#/CS_B	Input during Parallel mode configuration Possible input after configuration if SelectMap port is retained Otherwise, user I/O after configuration	Chip Select for Parallel Mode Configuration: In Parallel (SelectMAP) modes, this is the active-Low Chip Select signal. This pin becomes a user I/O after configuration unless the SelectMAP port is retained via the Persist bitstream option.
IO_Lxxy_#/RDWR_B	Input during Parallel mode configuration Possible input after configuration if SelectMap port is retained Otherwise, user I/O after configuration	Read/Write Control for Parallel Mode Configuration: In Parallel (SelectMAP) modes, this is the active-Low Write Enable, active-High Read Enable signal. This pin becomes a user I/O after configuration unless the SelectMAP port is retained via the Persist bitstream option.
IO_Lxxy_#/BUSY/DOUT	Output during configuration Possible output after configuration if SelectMap port is retained Otherwise, user I/O after configuration	Configuration Data Rate Control for Parallel Mode, Serial Data Output for Serial Mode: In Parallel (SelectMAP) modes, BUSY throttles the rate at which configuration data is loaded. This pin becomes a user I/O after configuration unless the SelectMAP port is retained via the Persist bitstream option. In Serial modes, DOUT provides preamble and configuration data to downstream devices in a multi-FPGA daisy-chain. This pin becomes a user I/O after configuration.
IO_Lxxy_#/INIT_B	Bidirectional (open-drain) during configuration User I/O after configuration	Initializing Configuration Memory/Detected Configuration Error: When Low, this pin indicates that configuration memory is being cleared. When held Low, this pin delays the start of configuration. After this pin is released or configuration memory is cleared, the pin goes High. During configuration, a Low on this output indicates that a configuration data error occurred. This pin always has an internal pull-up resistor to VCCO_4 or VCCO_BOTTOM during configuration, regardless of the HSWAP_EN pin. This pin becomes a user I/O after configuration.
DCI: Digitally Controlled Impedance reference resistor input pins		
IO_Lxxy_#/VRN_# or IO/VRN_#	Input when using DCI Otherwise, same as I/O	DCI Reference Resistor for NMOS I/O Transistor (per bank): If using DCI, a 1% precision impedance-matching resistor is connected between this pin and the VCCO supply for this bank. Otherwise, this pin is a user I/O.
IO_Lxxy_#/VRP_# or IO/VRP_#	Input when using DCI Otherwise, same as I/O	DCI Reference Resistor for PMOS I/O Transistor (per bank): If using DCI, a 1% precision impedance-matching resistor is connected between this pin and the ground supply. Otherwise, this pin is a user I/O.

Table 79: Pin Behavior After Power-Up, During Configuration (Cont'd)

Pin Name	Configuration Mode Settings <M2:M1:M0>					Bitstream Configuration Option
	Serial Modes		SelectMap Parallel Modes		JTAG Mode <1:0:1>	
	Master <0:0:0>	Slave <1:1:1>	Master <0:1:1>	Slave <1:1:0>		
JTAG: JTAG interface pins (pull-up resistor to VCCAUX always active during configuration, regardless of HSWAP_EN pin)						
TDI	TDI (I)	TDI (I)	TDI (I)	TDI (I)	TDI (I)	TdiPin
TMS	TMS (I)	TMS (I)	TMS (I)	TMS (I)	TMS (I)	TmsPin
TCK	TCK (I)	TCK (I)	TCK (I)	TCK (I)	TCK (I)	TckPin
TDO	TDO (O)	TDO (O)	TDO (O)	TDO (O)	TDO (O)	TdoPin

Table 89: CP132 Package Pinout (Cont'd)

Bank	XC3S50 Pin Name	CP132 Ball	Type
N/A	GND	M3	GND
N/A	GND	M13	GND
N/A	GND	N6	GND
N/A	GND	N11	GND
N/A	VCCAUX	A5	VCCAUX
N/A	VCCAUX	C10	VCCAUX
N/A	VCCAUX	M5	VCCAUX
N/A	VCCAUX	P10	VCCAUX
N/A	VCCINT	B10	VCCINT
N/A	VCCINT	C6	VCCINT
N/A	VCCINT	M9	VCCINT
N/A	VCCINT	N5	VCCINT
VCCAUX	CCLK	P14	CONFIG
VCCAUX	DONE	P13	CONFIG
VCCAUX	HSWAP_EN	B3	CONFIG
VCCAUX	M0	N1	CONFIG
VCCAUX	M1	M2	CONFIG
VCCAUX	M2	P1	CONFIG
VCCAUX	PROG_B	A2	CONFIG
VCCAUX	TCK	B14	JTAG
VCCAUX	TDI	A1	JTAG
VCCAUX	TDO	C13	JTAG
VCCAUX	TMS	A14	JTAG

User I/Os by Bank

Table 90 indicates how the 89 available user-I/O pins are distributed between the eight I/O banks on the CP132 package. There are only four output banks, each with its own VCCO voltage input.

Table 90: User I/Os Per Bank for XC3S50 in CP132 Package

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	10	5	0	2	1	2
	1	10	5	0	2	1	2
Right	2	12	8	0	2	2	0
	3	12	8	0	2	2	0
Bottom	4	11	0	6	2	1	2
	5	10	1	6	0	1	2
Left	6	12	8	0	2	2	0
	7	12	9	0	2	1	0

Notes:

- The CP132 and CPG132 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.

TQ144: 144-lead Thin Quad Flat Package

The XC3S50, the XC3S200, and the XC3S400 are available in the 144-lead thin quad flat package, TQ144. All devices share a common footprint for this package as shown in [Table 91](#) and [Figure 46](#).

The TQ144 package only has four separate VCCO inputs, unlike the BGA packages, which have eight separate VCCO inputs. The TQ144 package has a separate VCCO input for the top, bottom, left, and right. However, there are still eight separate I/O banks, as shown in [Table 91](#) and [Figure 46](#). Banks 0 and 1 share the VCCO_TOP input, Banks 2 and 3 share the VCCO_RIGHT input, Banks 4 and 5 share the VCCO_BOTTOM input, and Banks 6 and 7 share the VCCO_LEFT input.

All the package pins appear in [Table 91](#) and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_sheets/s3_pin.zip.

Pinout Table

Table 91: TQ144 Package Pinout

Bank	XC3S50, XC3S200, XC3S400 Pin Name	TQ144 Pin Number	Type
0	IO_L01N_0/VRP_0	P141	DCI
0	IO_L01P_0/VRN_0	P140	DCI
0	IO_L27N_0	P137	I/O
0	IO_L27P_0	P135	I/O
0	IO_L30N_0	P132	I/O
0	IO_L30P_0	P131	I/O
0	IO_L31N_0	P130	I/O
0	IO_L31P_0/VREF_0	P129	VREF
0	IO_L32N_0/GCLK7	P128	GCLK
0	IO_L32P_0/GCLK6	P127	GCLK
1	IO	P116	I/O
1	IO_L01N_1/VRP_1	P113	DCI
1	IO_L01P_1/VRN_1	P112	DCI
1	IO_L28N_1	P119	I/O
1	IO_L28P_1	P118	I/O
1	IO_L31N_1/VREF_1	P123	VREF
1	IO_L31P_1	P122	I/O
1	IO_L32N_1/GCLK5	P125	GCLK
1	IO_L32P_1/GCLK4	P124	GCLK
2	IO_L01N_2/VRP_2	P108	DCI
2	IO_L01P_2/VRN_2	P107	DCI
2	IO_L20N_2	P105	I/O
2	IO_L20P_2	P104	I/O
2	IO_L21N_2	P103	I/O
2	IO_L21P_2	P102	I/O
2	IO_L22N_2	P100	I/O
2	IO_L22P_2	P99	I/O

User I/Os by Bank

Table 97 indicates how the available user-I/O pins are distributed between the eight I/O banks on the FT256 package.

Table 97: User I/Os Per Bank in FT256 Package

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	20	13	0	2	3	2
	1	20	13	0	2	3	2
Right	2	23	18	0	2	3	0
	3	23	18	0	2	3	0
Bottom	4	21	8	6	2	3	2
	5	20	7	6	2	3	2
Left	6	23	18	0	2	3	0
	7	23	18	0	2	3	0

ds099-3 16 121103

156	I/O: Unrestricted, general-purpose user I/O	12	DUAL: Configuration pin, then possible user I/O	29	VREF: User I/O or input voltage reference for bank
16	DCI: User I/O or reference resistor input for bank	8	GCLK: User I/O or global clock buffer input	28	VCCO: Output voltage supply for bank
7	CONFIG: Dedicated configuration pins	4	JTAG: Dedicated JTAG port pins	12	VCCINT: Internal core voltage supply (+1.2V)
0	N.C.: No unconnected pins in this package	40	GND: Ground	8	VCCAUX: Auxiliary voltage supply (+2.5V)

Table 100: FG456 Package Pinout (Cont'd)

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
3	IO_L16P_3	IO_L16P_3	Y22	I/O
3	IO_L17N_3	IO_L17N_3	V19	I/O
3	IO_L17P_3/VREF_3	IO_L17P_3/VREF_3	W19	VREF
3	IO_L19N_3	IO_L19N_3	W21	I/O
3	IO_L19P_3	IO_L19P_3	W20	I/O
3	IO_L20N_3	IO_L20N_3	U19	I/O
3	IO_L20P_3	IO_L20P_3	V20	I/O
3	IO_L21N_3	IO_L21N_3	V22	I/O
3	IO_L21P_3	IO_L21P_3	V21	I/O
3	IO_L22N_3	IO_L22N_3	T17	I/O
3	IO_L22P_3	IO_L22P_3	U18	I/O
3	IO_L23N_3	IO_L23N_3	U21	I/O
3	IO_L23P_3/VREF_3	IO_L23P_3/VREF_3	U20	VREF
3	IO_L24N_3	IO_L24N_3	R18	I/O
3	IO_L24P_3	IO_L24P_3	T18	I/O
3	N.C. (◆)	IO_L26N_3	T20	I/O
3	N.C. (◆)	IO_L26P_3	T19	I/O
3	IO_L27N_3	IO_L27N_3	T22	I/O
3	IO_L27P_3	IO_L27P_3	T21	I/O
3	N.C. (◆)	IO_L28N_3	R22	I/O
3	N.C. (◆)	IO_L28P_3	R21	I/O
3	N.C. (◆)	IO_L29N_3	P19	I/O
3	N.C. (◆)	IO_L29P_3	R19	I/O
3	N.C. (◆)	IO_L31N_3	P18	I/O
3	N.C. (◆)	IO_L31P_3	P17	I/O
3	N.C. (◆)	IO_L32N_3	P22	I/O
3	N.C. (◆)	IO_L32P_3	P21	I/O
3	N.C. (◆)	IO_L33N_3	N18	I/O
3	N.C. (◆)	IO_L33P_3	N17	I/O
3	IO_L34N_3	IO_L34N_3	N20	I/O
3	IO_L34P_3/VREF_3	IO_L34P_3/VREF_3	N19	VREF
3	IO_L35N_3	IO_L35N_3	N22	I/O
3	IO_L35P_3	IO_L35P_3	N21	I/O
3	IO_L38N_3	IO_L38N_3	M18	I/O
3	IO_L38P_3	IO_L38P_3	M17	I/O
3	IO_L39N_3	IO_L39N_3	M20	I/O
3	IO_L39P_3	IO_L39P_3	M19	I/O
3	IO_L40N_3/VREF_3	IO_L40N_3/VREF_3	M22	VREF
3	IO_L40P_3	IO_L40P_3	M21	I/O
3	VCCO_3	VCCO_3	M16	VCCO

FG676: 676-lead Fine-pitch Ball Grid Array

The 676-lead fine-pitch ball grid array package, FG676, supports five different Spartan-3 devices, including the XC3S1000, XC3S1500, XC3S2000, XC3S4000, and XC3S5000. All five have nearly identical footprints but are slightly different, primarily due to unconnected pins on the XC3S1000 and XC3S1500. For example, because the XC3S1000 has fewer I/O pins, this device has 98 unconnected pins on the FG676 package, labeled as “N.C.” In [Table 103](#) and [Figure 53](#), these unconnected pins are indicated with a black diamond symbol (◆). The XC3S1500, however, has only two unconnected pins, also labeled “N.C.” in the pinout table but indicated with a black square symbol (■).

All the package pins appear in [Table 103](#) and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

If there is a difference between the XC3S1000, XC3S1500, XC3S2000, XC3S4000, and XC3S5000 pinouts, then that difference is highlighted in [Table 103](#). If the table entry is shaded grey, then there is an unconnected pin on either the XC3S1000 or XC3S1500 that maps to a user-I/O pin on the XC3S2000, XC3S4000, and XC3S5000. If the table entry is shaded tan, then the unconnected pin on either the XC3S1000 or XC3S1500 maps to a VREF-type pin on the XC3S2000, XC3S4000, and XC3S5000. If the other VREF pins in the bank all connect to a voltage reference to support a special I/O standard, then also connect the N.C. pin on the XC3S1000 or XC3S1500 to the same VREF voltage. This provides maximum flexibility as you could potentially migrate a design from the XC3S1000 through to the XC3S5000 FPGA without changing the printed circuit board.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_sheets/s3_pin.zip.

Pinout Table

Table 103: FG676 Package Pinout

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
0	IO	IO	IO	IO	IO_L04N_0 ⁽³⁾	A3	I/O
0	IO	IO	IO	IO	IO	A5	I/O
0	IO	IO	IO	IO	IO	A6	I/O
0	IO	IO	IO	IO	IO_L04P_0 ⁽³⁾	C4	I/O
0	N.C. (◆)	IO	IO	IO	IO_L13N_0 ⁽³⁾	C8	I/O
0	IO	IO	IO	IO	IO	C12	I/O
0	IO	IO	IO	IO	IO	E13	I/O
0	IO	IO	IO	IO	IO	H11	I/O
0	IO	IO	IO	IO	IO	H12	I/O
0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	B3	VREF
0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	F7	VREF
0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	G10	VREF
0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	E5	DCI
0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	D5	DCI
0	IO_L05N_0	IO_L05N_0	IO_L05N_0	IO_L05N_0	IO_L05N_0	B4	I/O
0	IO_L05P_0/VREF_0	IO_L05P_0/VREF_0	IO_L05P_0/VREF_0	IO_L05P_0/VREF_0	IO_L05P_0/VREF_0	A4	VREF
0	IO_L06N_0	IO_L06N_0	IO_L06N_0	IO_L06N_0	IO_L06N_0	C5	I/O
0	IO_L06P_0	IO_L06P_0	IO_L06P_0	IO_L06P_0	IO_L06P_0	B5	I/O
0	IO_L07N_0	IO_L07N_0	IO_L07N_0	IO_L07N_0	IO_L07N_0	E6	I/O
0	IO_L07P_0	IO_L07P_0	IO_L07P_0	IO_L07P_0	IO_L07P_0	D6	I/O
0	IO_L08N_0	IO_L08N_0	IO_L08N_0	IO_L08N_0	IO_L08N_0	C6	I/O
0	IO_L08P_0	IO_L08P_0	IO_L08P_0	IO_L08P_0	IO_L08P_0	B6	I/O

Table 107: FG900 Package Pinout (Cont'd)

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
6	IO_L05P_6	IO_L05P_6	AE5	I/O
6	IO_L06N_6	IO_L06N_6	AE3	I/O
6	IO_L06P_6	IO_L06P_6	AE2	I/O
6	IO_L07N_6	IO_L07N_6	AD4	I/O
6	IO_L07P_6	IO_L07P_6	AD3	I/O
6	IO_L08N_6	IO_L08N_6	AD2	I/O
6	IO_L08P_6	IO_L08P_6	AD1	I/O
6	IO_L09N_6/VREF_6	IO_L09N_6/VREF_6	AD6	VREF
6	IO_L09P_6	IO_L09P_6	AC7	I/O
6	IO_L10N_6	IO_L10N_6	AC6	I/O
6	IO_L10P_6	IO_L10P_6	AC5	I/O
6	IO_L11N_6	IO_L11N_6	AC4	I/O
6	IO_L11P_6	IO_L11P_6	AC3	I/O
6	IO_L13N_6	IO_L13N_6	AC2	I/O
6	IO_L13P_6/VREF_6	IO_L13P_6/VREF_6	AC1	VREF
6	IO_L14N_6	IO_L14N_6	AB5	I/O
6	IO_L14P_6	IO_L14P_6	AB4	I/O
6	IO_L15N_6	IO_L15N_6	AB2	I/O
6	IO_L15P_6	IO_L15P_6	AB1	I/O
6	IO_L16N_6	IO_L16N_6	AB8	I/O
6	IO_L16P_6	IO_L16P_6	AA9	I/O
6	IO_L17N_6	IO_L17N_6	AA7	I/O
6	IO_L17P_6/VREF_6	IO_L17P_6/VREF_6	AA6	VREF
6	IO_L19N_6	IO_L19N_6	AA3	I/O
6	IO_L19P_6	IO_L19P_6	AA2	I/O
6	IO_L20N_6	IO_L20N_6	AA10	I/O
6	IO_L20P_6	IO_L20P_6	Y10	I/O
6	IO_L21N_6	IO_L21N_6	Y8	I/O
6	IO_L21P_6	IO_L21P_6	Y7	I/O
6	IO_L22N_6	IO_L22N_6	Y6	I/O
6	IO_L22P_6	IO_L22P_6	Y5	I/O
6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	Y2	VREF
6	IO_L24P_6	IO_L24P_6	Y1	I/O
6	N.C. (◆)	IO_L25N_6	W9	I/O
6	N.C. (◆)	IO_L25P_6	W8	I/O
6	IO_L26N_6	IO_L26N_6	W7	I/O
6	IO_L26P_6	IO_L26P_6	W6	I/O
6	IO_L27N_6	IO_L27N_6	W4	I/O
6	IO_L27P_6	IO_L27P_6	W3	I/O
6	IO_L28N_6	IO_L28N_6	W2	I/O

Table 110: FG1156 Package Pinout (Cont'd)

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
6	IO_L16N_6	IO_L16N_6	AE2	I/O
6	IO_L16P_6	IO_L16P_6	AE1	I/O
6	IO_L17N_6	IO_L17N_6	AD10	I/O
6	IO_L17P_6/VREF_6	IO_L17P_6/VREF_6	AD9	VREF
6	IO_L19N_6	IO_L19N_6	AD2	I/O
6	IO_L19P_6	IO_L19P_6	AD1	I/O
6	IO_L20N_6	IO_L20N_6	AC11	I/O
6	IO_L20P_6	IO_L20P_6	AC10	I/O
6	IO_L21N_6	IO_L21N_6	AC8	I/O
6	IO_L21P_6	IO_L21P_6	AC7	I/O
6	IO_L22N_6	IO_L22N_6	AC6	I/O
6	IO_L22P_6	IO_L22P_6	AC5	I/O
6	IO_L23N_6	IO_L23N_6	AC2	I/O
6	IO_L23P_6	IO_L23P_6	AC1	I/O
6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	AC9	VREF
6	IO_L24P_6	IO_L24P_6	AB10	I/O
6	IO_L25N_6	IO_L25N_6	AB8	I/O
6	IO_L25P_6	IO_L25P_6	AB7	I/O
6	IO_L26N_6	IO_L26N_6	AB4	I/O
6	IO_L26P_6	IO_L26P_6	AB3	I/O
6	IO_L27N_6	IO_L27N_6	AB11	I/O
6	IO_L27P_6	IO_L27P_6	AA11	I/O
6	IO_L28N_6	IO_L28N_6	AA8	I/O
6	IO_L28P_6	IO_L28P_6	AA7	I/O
6	IO_L29N_6	IO_L29N_6	AA6	I/O
6	IO_L29P_6	IO_L29P_6	AA5	I/O
6	IO_L30N_6	IO_L30N_6	AA4	I/O
6	IO_L30P_6	IO_L30P_6	AA3	I/O
6	IO_L31N_6	IO_L31N_6	AA2	I/O
6	IO_L31P_6	IO_L31P_6	AA1	I/O
6	IO_L32N_6	IO_L32N_6	Y11	I/O
6	IO_L32P_6	IO_L32P_6	Y10	I/O
6	IO_L33N_6	IO_L33N_6	Y4	I/O
6	IO_L33P_6	IO_L33P_6	Y3	I/O
6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	Y2	VREF
6	IO_L34P_6	IO_L34P_6	Y1	I/O
6	IO_L35N_6	IO_L35N_6	Y9	I/O
6	IO_L35P_6	IO_L35P_6	W10	I/O
6	IO_L36N_6	IO_L36N_6	W7	I/O
6	IO_L36P_6	IO_L36P_6	W6	I/O

Table 110: FG1156 Package Pinout (Cont'd)

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
7	IO_L22P_7	IO_L22P_7	M6	I/O
7	IO_L23N_7	IO_L23N_7	M3	I/O
7	IO_L23P_7	IO_L23P_7	M4	I/O
7	IO_L24N_7	IO_L24N_7	N10	I/O
7	IO_L24P_7	IO_L24P_7	M9	I/O
7	IO_L25N_7	IO_L25N_7	N3	I/O
7	IO_L25P_7	IO_L25P_7	N4	I/O
7	IO_L26N_7	IO_L26N_7	P11	I/O
7	IO_L26P_7	IO_L26P_7	N11	I/O
7	IO_L27N_7	IO_L27N_7	P7	I/O
7	IO_L27P_7/VREF_7	IO_L27P_7/VREF_7	P8	VREF
7	IO_L28N_7	IO_L28N_7	P5	I/O
7	IO_L28P_7	IO_L28P_7	P6	I/O
7	IO_L29N_7	IO_L29N_7	P3	I/O
7	IO_L29P_7	IO_L29P_7	P4	I/O
7	IO_L30N_7	IO_L30N_7	R6	I/O
7	IO_L30P_7	IO_L30P_7	R7	I/O
7	IO_L31N_7	IO_L31N_7	R3	I/O
7	IO_L31P_7	IO_L31P_7	R4	I/O
7	IO_L32N_7	IO_L32N_7	R1	I/O
7	IO_L32P_7	IO_L32P_7	R2	I/O
7	IO_L33N_7	IO_L33N_7	T10	I/O
7	IO_L33P_7	IO_L33P_7	R9	I/O
7	IO_L34N_7	IO_L34N_7	T6	I/O
7	IO_L34P_7	IO_L34P_7	T7	I/O
7	IO_L35N_7	IO_L35N_7	T2	I/O
7	IO_L35P_7	IO_L35P_7	T3	I/O
7	IO_L37N_7	IO_L37N_7	U7	I/O
7	IO_L37P_7/VREF_7	IO_L37P_7/VREF_7	U8	VREF
7	IO_L38N_7	IO_L38N_7	U5	I/O
7	IO_L38P_7	IO_L38P_7	U6	I/O
7	IO_L39N_7	IO_L39N_7	U3	I/O
7	IO_L39P_7	IO_L39P_7	U4	I/O
7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	U1	VREF
7	IO_L40P_7	IO_L40P_7	U2	I/O
7	N.C. (◆)	IO_L41N_7	G3	I/O
7	N.C. (◆)	IO_L41P_7	G4	I/O
7	N.C. (◆)	IO_L44N_7	L6	I/O
7	N.C. (◆)	IO_L44P_7	L7	I/O
7	IO_L45N_7	IO_L45N_7	M1	I/O