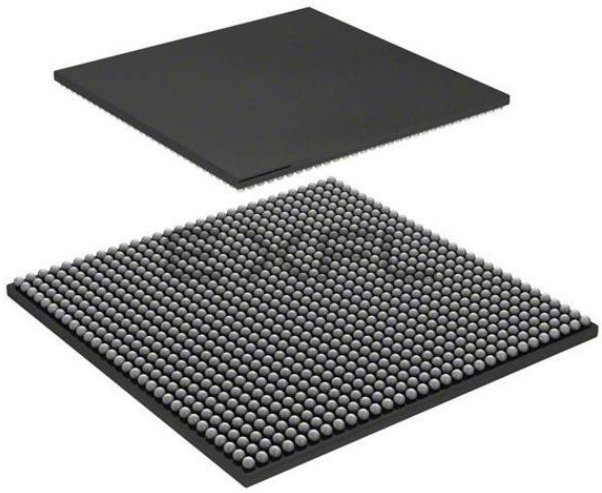
AMD Xilinx - XC3S4000-5FGG900C Datasheet



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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	6912
Number of Logic Elements/Cells	62208
Total RAM Bits	1769472
Number of I/O	633
Number of Gates	4000000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	900-BBGA
Supplier Device Package	900-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s4000-5fgg900c

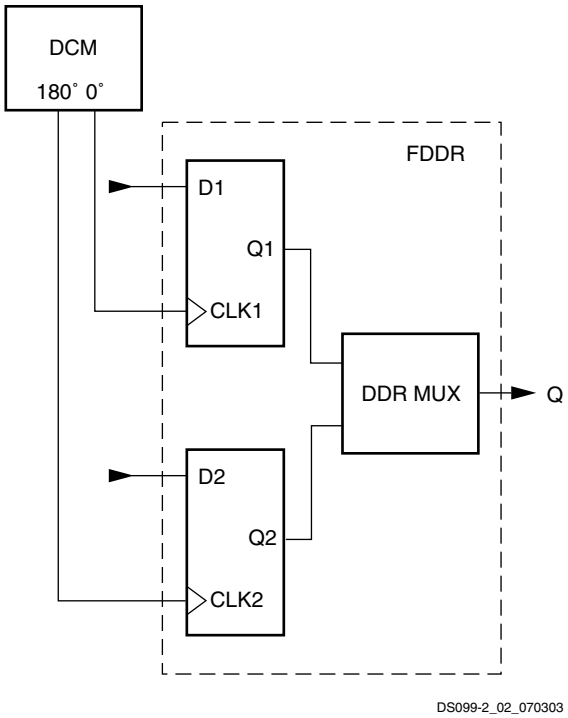


Figure 8: **Clocking the DDR Register**

Aside from high bandwidth data transfers, DDR can also be used to reproduce, or “mirror”, a clock signal on the output. This approach is used to transmit clock and data signals together. A similar approach is used to reproduce a clock signal at multiple outputs. The advantage for both approaches is that skew across the outputs will be minimal.

Some adjacent I/O blocks (IOBs) share common routing connecting the ICLK1, ICLK2, OTCLK1, and OTCLK2 clock inputs of both IOBs. These IOB pairs are identified by their differential pair names IO_LxxN_# and IO_LxxP_#, where "xx" is an I/O pair number and ‘#’ is an I/O bank number. Two adjacent IOBs containing DDR registers must share common clock inputs, otherwise one or more of the clock signals will be unroutable.

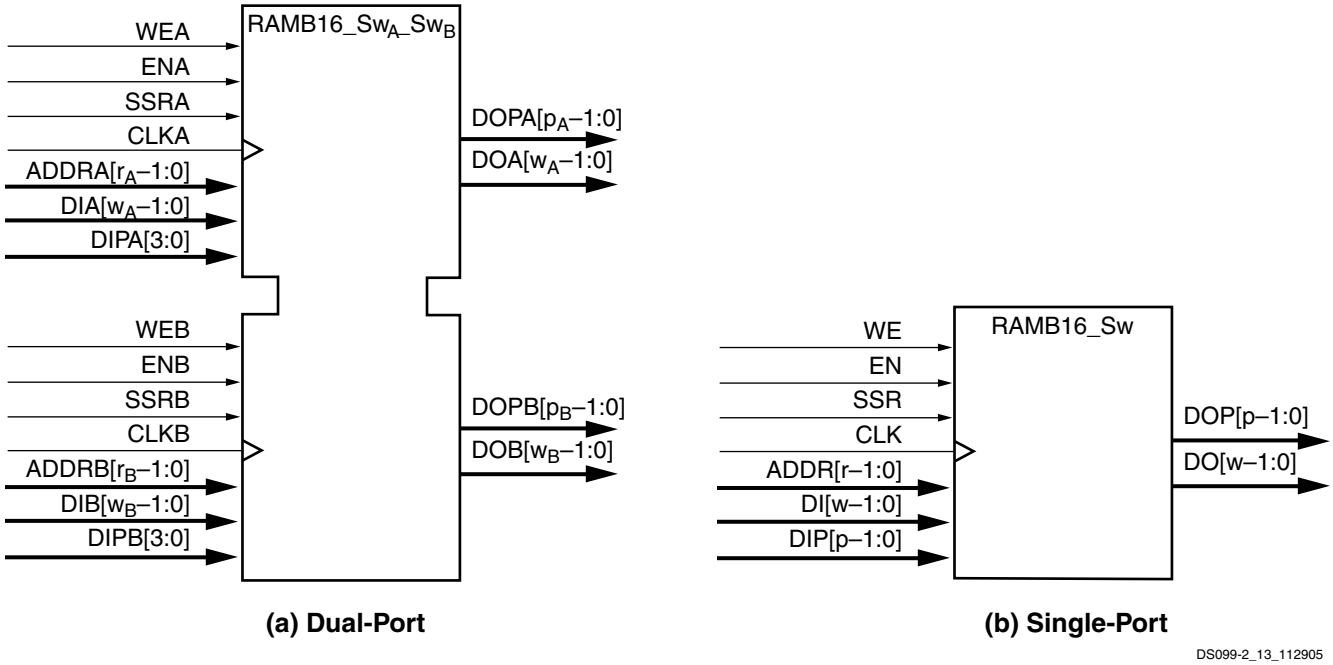
Pull-Up and Pull-Down Resistors

The optional pull-up and pull-down resistors are intended to establish High and Low levels, respectively, at unused I/Os. The pull-up resistor optionally connects each IOB pad to V_{CCO}. A pull-down resistor optionally connects each pad to GND. These resistors are placed in a design using the PULLUP and PULLDOWN symbols in a schematic, respectively. They can also be instantiated as components, set as constraints or passed as attributes in HDL code. These resistors can also be selected for all unused I/O using the Bitstream Generator (BitGen) option UnusedPin. A Low logic level on HSWAP_EN activates the pull-up resistors on all I/Os during configuration (see The I/Os During Power-On, Configuration, and User Mode, page 21).

The Spartan-3 FPGAs I/O pull-up and pull-down resistors are significantly stronger than the "weak" pull-up/pull-down resistors used in previous Xilinx FPGA families. See Table 33, page 61 for equivalent resistor strengths.

Keeper Circuit

Each I/O has an optional keeper circuit that retains the last logic level on a line after all drivers have been turned off. This is useful to keep bus lines from floating when all connected drivers are in a high-impedance state. This function is placed in a design using the KEEPER symbol. Pull-up and pull-down resistors override the keeper circuit.



Notes:

1. w_A and w_B are integers representing the total data path width (i.e., data bits plus parity bits) at ports A and B, respectively.
2. p_A and p_B are integers that indicate the number of data path lines serving as parity bits.
3. r_A and r_B are integers representing the address bus width at ports A and B, respectively.
4. The control signals CLK, WE, EN, and SSR on both ports have the option of inverted polarity.

Figure 14: **Block RAM Primitives**

Table 13: **Block RAM Port Signals**

Signal Description	Port A Signal Name	Port B Signal Name	Direction	Function
Address Bus	ADDRA	ADDRB	Input	The Address Bus selects a memory location for read or write operations. The width (w) of the port's associated data path determines the number of available address lines (r). Whenever a port is enabled (ENA or ENB = High), address transitions must meet the data sheet setup and hold times with respect to the port clock (CLKA or CLKB). This requirement must be met, even if the RAM read output is of no interest.
Data Input Bus	DIA	DIB	Input	Data at the DI input bus is written to the addressed memory location addressed on an enabled active CLK edge. It is possible to configure a port's total data path width (w) to be 1, 2, 4, 9, 18, or 36 bits. This selection applies to both the DI and DO paths of a given port. Each port is independent. For a port assigned a width (w), the number of addressable locations is 16,384/(w-p) where "p" is the number of parity bits. Each memory location has a width of "w" (including parity bits). See the DIP signal description for more information of parity.
Parity Data Input(s)	DIPA	DIPB	Input	Parity inputs represent additional bits included in the data input path to support error detection. The number of parity bits "p" included in the DI (same as for the DO bus) depends on a port's total data path width (w). See Table 14.

DFS Clock Output Connections

There are two basic cases that determine how to connect the DFS clock outputs: on-chip and off-chip, which are illustrated in sections [a] and [c], respectively, of Figure 21. This is similar to what has already been described for the DLL component. See DLL Clock Output and Feedback Connections, page 34.

In the on-chip case, it is possible to connect either of the DFS's two output clock signals through general routing resources to the FPGA's internal registers. Either a Global Clock Buffer (BUFG) or a BUFGMUX affords access to the global clock network. The optional feedback loop is formed in this way, routing CLK0 to a global clock net, which in turn drives the CLKFB input.

In the off-chip case, the DFS's two output clock signals, plus CLK0 for an optional feedback loop, can exit the FPGA using output buffers (OBUF) to drive a clock network plus registers on the board. The feedback loop is formed by feeding the CLK0 signal back into the FPGA using an IBUFG, which directly accesses the global clock network, or an IBUF. Then, the global clock net is connected directly to the CLKFB input.

Phase Shifter (PS)

The DCM provides two approaches to controlling the phase of a DCM clock output signal relative to the CLKIN signal: First, there are nine clock outputs that employ the DLL to achieve a desired phase relationship: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, CLKDV CLKFX, and CLKFX180. These outputs afford "coarse" phase control.

The second approach uses the PS component described in this section to provide a still finer degree of control. The PS component is only available when the DLL is operating in its low-frequency mode. The PS component phase shifts the DCM output clocks by introducing a "fine phase shift" (T_{PS}) between the CLKFB and CLKIN signals inside the DLL component. The user can control this fine phase shift down to a resolution of 1/256 of a CLKIN cycle or one tap delay (DCM_TAP), whichever is greater. When in use, the PS component shifts the phase of all nine DCM clock output signals together. If the PS component is used together with a DCM clock output such as the CLK90, CLK180, CLK270, CLK2X180 and CLKFX180, then the fine phase shift of the former gets added to the coarse phase shift of the latter.

PS Component Enabling and Mode Selection

The CLKOUT_PHASE_SHIFT attribute enables the PS component for use in addition to selecting between two operating modes. As described in Table 20, this attribute has three possible values: NONE, FIXED and VARIABLE. When CLKOUT_PHASE_SHIFT is set to NONE, the PS component is disabled and its inputs, PSEN, PSCLK, and PSINCDEC, must be tied to GND. The set of waveforms in section [a] of Figure 22 shows the disabled case, where the DLL maintains a zero-phase alignment of signals CLKFB and CLKIN upon which the PS component has no effect. The PS component is enabled by setting the attribute to either the FIXED or VARIABLE values, which select the Fixed Phase mode and the Variable Phase mode, respectively. These two modes are described in the sections that follow

Determining the Fine Phase Shift

The user controls the phase shift of CLKFB relative to CLKIN by setting and/or adjusting the value of the PHASE_SHIFT attribute. This value must be an integer ranging from –255 to +255. The PS component uses this value to calculate the desired fine phase shift (T_{PS}) as a fraction of the CLKIN period (T_{CLKIN}). Given values for PHASE-SHIFT and T_{CLKIN}, it is possible to calculate T_{PS} as follows:

$$T_{PS} = T_{CLKIN}(PHASE\_SHIFT/256) \qquad \textit{Equation 4}$$

Both the Fixed Phase and Variable Phase operating modes employ this calculation. If the PHASE_SHIFT value is zero, then CLKFB and CLKIN will be in phase, the same as when the PS component is disabled. When the PHASE_SHIFT value is positive, the CLKFB signal will be shifted later in time with respect to CLKIN. If the attribute value is negative, the CLKFB signal will be shifted earlier in time with respect to CLKIN.

The Fixed Phase Mode

This mode fixes the desired fine phase shift to a fraction of the T_{CLKIN}, as determined by Equation 4 and its user-selected PHASE_SHIFT value P. The set of waveforms insection [b] of Figure 22 illustrates the relationship between CLKFB and CLKIN in the Fixed Phase mode. In the Fixed Phase mode, the PSEN, PSCLK and PSINCDEC inputs are not used and must be tied to GND. Fixed phase shift requires ISE software version 10.1.03 or later.

Table 28: **Absolute Maximum Ratings *(Cont'd)***

Symbol	Description	Conditions	Min	Max	Units
I_{IK}	Input clamp current per I/O pin	–0.5 V < V_{IN} < (V_{CCO} + 0.5 V)	–	±100	mA
V_{ESD}	Electrostatic Discharge Voltage pins relative to GND	Human body model	–	±2000	V
		Charged device model	–	±500	V
		Machine model	–	±200	V
T_J	Junction temperature		–	125	°C
T_{SOL}	Soldering temperature(4)		–	220	°C
T_{STG}	Storage temperature		–65	150	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time adversely affects device reliability.
2. All User I/O and Dual-Purpose pins (DIN/D0, D1–D7, CS_B, RDWR_B, BUSY/DOUT, and INIT_B) draw power from the V_{CCO} power rail of the associated bank. Keeping VIN within 500 mV of the associated V_{CCO} rails or ground rail ensures that the internal diode junctions that exist between each of these pins and the V_{CCO} and GND rails do not turn on. Table 32 specifies the V_{CCO} range used to determine the max limit. Input voltages outside the –0.5V to V_{CCO}+0.5V voltage range are permissible provided that the I_{IK} input clamp diode rating is met and no more than 100 pins exceed the range simultaneously. Prolonged exposure to such current may compromise device reliability. A sustained current of 10 mA will not compromise device reliability. See XAPP459, *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Generation FPGAs* for more details. The VIN limits apply to both the DC and AC components of signals. Simple application solutions are available that show how to handle overshoot/undershoot as well as achieve PCI compliance. Refer to the following application notes: XAPP457, *Powering and Configuring Spartan-3 Generation FPGAs in Compliant PCI Applications* and XAPP659, *Virtex®-II Pro / Virtex-II Pro X 3.3V I/O Design Guidelines*.
3. All Dedicated pins (M0–M2, CCLK, PROG_B, DONE, HSWAP_EN, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail (2.5V). Meeting the V_{IN} max limit ensures that the internal diode junctions that exist between each of these pins and the V_{CCAUX} rail do not turn on. Table 32 specifies the V_{CCAUX} range used to determine the max limit. When V_{CCAUX} is at its maximum recommended operating level (2.625V), V_{IN} max < 3.125V. As long as the V_{IN} max specification is met, oxide stress is not possible. For information concerning the use of 3.3V signals, see the 3.3V-Tolerant Configuration Interface, page 47. See also XAPP459.
4. For soldering guidelines, see UG112, *Device Packaging and Thermal Characteristics* and XAPP427, *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

Table 29: **Supply Voltage Thresholds for Power-On Reset**

Symbol	Description	Min	Max	Units
V_{CCINTT}	Threshold for the V_{CCINT} supply	0.4	1.0	V
V_{CCAUXT}	Threshold for the V_{CCAUX} supply	0.8	2.0	V
V_{CCO4T}	Threshold for the V_{CCO} Bank 4 supply	0.4	1.0	V

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies may be applied in any order. When applying V_{CCINT} power before V_{CCAUX} power, the FPGA may draw a *surplus* current in addition to the quiescent current levels specified in Table 34. Applying V_{CCAUX} eliminates the surplus current. The FPGA does not use any of the surplus current for the power-on process. For this power sequence, make sure that regulators with foldback features will not shut down inadvertently.
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 4, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.
3. If a brown-out condition occurs where V_{CCAUX} or V_{CCINT} drops below the retention voltage indicated in Table 31, then V_{CCAUX} or V_{CCINT} must drop below the minimum power-on reset voltage in order to clear out the device configuration content.

Table 30: **Power Voltage Ramp Time Requirements**

Symbol	Description	Device	Package	Min	Max	Units
T_{CCO}	V_{CCO} ramp time for all eight banks	All	All	No limit(4)	–	N/A
T_{CCINT}	V_{CCINT} ramp time, only if V_{CCINT} is last in three-rail power-on sequence	All	All	No limit	No limit(5)	N/A

Notes:

1. If a limit exists, this specification is based on characterization.
2. The ramp time is measured from 10% to 90% of the full nominal voltage swing for all I/O standards.
3. For information on power-on current needs, see Power-On Behavior, page 54
4. For mask revisions earlier than revision E (see Mask and Fab Revisions, page 58), T_{CCO} min is limited to 2.0 ms for the XC3S200 and XC3S400 devices in QFP packages, and limited to 0.6 ms for the XC3S200, XC3S400, XC3S1500, and XC3S4000 devices in the FT and FG packages.
5. For earlier device versions with the FQ fabrication/process code (see Mask and Fab Revisions, page 58), T_{CCINT} max is limited to 500 µs.

Table 31: **Power Voltage Levels Necessary for Preserving RAM Contents**

Symbol	Description	Min	Units
V_{DRINT}	V_{CCINT} level required to retain RAM data	1.0	V
V_{DRAUX}	V_{CCAUX} level required to retain RAM data	2.0	V

Notes:

1. RAM contents include data stored in CMOS configuration latches.
2. The level of the V_{CCO} supply has no effect on data retention.
3. If a brown-out condition occurs where V_{CCAUX} or V_{CCINT} drops below the retention voltage, then V_{CCAUX} or V_{CCINT} must drop below the minimum power-on reset voltage indicated in Table 29 in order to clear out the device configuration content.

Table 32: **General Recommended Operating Conditions**

Symbol	Description		Min	Nom	Max	Units
T_J	Junction temperature	Commercial	0	25	85	°C
		Industrial	–40	25	100	°C
V_{CCINT}	Internal supply voltage		1.140	1.200	1.260	V
V_{CCO}(1)	Output driver supply voltage		1.140	–	3.465	V
V_{CCAUX}	Auxiliary supply voltage		2.375	2.500	2.625	V
ΔV_{CCAUX}(2)	Voltage variance on VCCAUX when using a DCM		–	–	10	mV/ms
V_{IN}(3)	Voltage applied to all User I/O pins and Dual-Purpose pins relative to GND(4)(6)	V_{CCO} = 3.3V, IO	–0.3	–	3.75	V
		V_{CCO} = 3.3V, IO_Lxxy(7)	–0.3	–	3.75	V
		$V_{CCO} \le$ 2.5V, IO	–0.3	–	V_{CCO} + 0.3(4)	V
		$V_{CCO} \le$ 2.5V, IO_Lxxy(7)	–0.3	–	V_{CCO} + 0.3(4)	V
	Voltage applied to all Dedicated pins relative to GND(5)		–0.3	–	V_{CCAUX} + 0.3(5)	V

Notes:

1. The V_{CCO} range given here spans the lowest and highest operating voltages of all supported I/O standards. The recommended V_{CCO} range specific to each of the single-ended I/O standards is given in Table 35, and that specific to the differential standards is given in Table 37.
2. Only during DCM operation is it recommended that the rate of change of V_{CCAUX} not exceed 10 mV/ms.
3. Input voltages outside the recommended range are permissible provided that the I_{IK} input diode clamp diode rating is met. Refer to Table 28.
4. Each of the User I/O and Dual-Purpose pins is associated with one of the V_{CCO} rails. Meeting the V_{IN} limit ensures that the internal diode junctions that exist between these pins and their associated V_{CCO} and GND rails do not turn on. The absolute maximum rating is provided in Table 28.
5. All Dedicated pins (PROG_B, DONE, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail (2.5V). Meeting the V_{IN} max limit ensures that the internal diode junctions that exist between each of these pins and the V_{CCAUX} and GND rails do not turn on.
6. See XAPP459, *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Generation FPGAs*.
7. For single-ended signals that are placed on a differential-capable I/O, V_{IN} of –0.2V to –0.3V is supported but can cause increased leakage between the two pins. See the *Parasitic Leakage* section in UG331, *Spartan-3 Generation FPGA User Guide*.

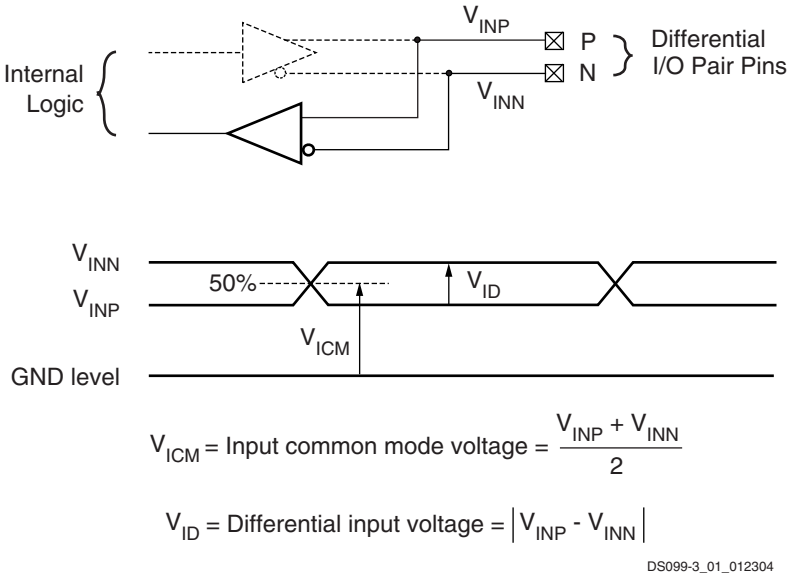


Figure 32: **Differential Input Voltages**

Table 37: **Recommended Operating Conditions for User I/Os Using Differential Signal Standards**

Signal Standard (IOSTANDARD)	V_{CCO}[1]			V_{ID}[3]			V_{ICM}		
	Min (V)	Nom (V)	Max (V)	Min (mV)	Nom (mV)	Max (mV)	Min (V)	Nom (V)	Max (V)
LDT_25 (ULVDS_25)	2.375	2.50	2.625	200	600	1000	0.44	0.60	0.78
LVDS_25, LVDS_25_DCI	2.375	2.50	2.625	100	350	600	0.30	1.25	2.20
BLVDS_25	2.375	2.50	2.625	-	350	-	-	1.25	-
LVDSEXT_25, LVDSEXT_25_DCI	2.375	2.50	2.625	100	540	1000	0.30	1.20	2.20
LVPECL_25	2.375	2.50	2.625	100	-	-	0.30	1.20	2.00
RSDS_25	2.375	2.50	2.625	100	200	-	-	1.20	-
DIFF_HSTL_II_18, DIFF_HSTL_II_18_DCI	1.70	1.80	1.90	200	-	-	0.80	-	1.00
DIFF_SSTL2_II, DIFF_SSTL2_II_DCI	2.375	2.50	2.625	300	-	-	1.05	-	1.45

Notes:

1. V_{CCO} only supplies differential output drivers, not input circuits.
2. V_{REF} inputs are not used for any of the differential I/O standards.
3. V_{ID} is a differential measurement.

Table 41: **System-Synchronous Pin-to-Pin Setup and Hold Times for the IOB Input Path *(Cont'd)***

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Min	Min	
T_{PHFD}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(3), IOBDELAY = IFD, without DCM	XC3S50	–0.98	–0.93	ns
			XC3S200	–0.40	–0.35	ns
			XC3S400	–0.27	–0.22	ns
			XC3S1000	–1.19	–1.14	ns
			XC3S1500	–1.43	–1.38	ns
			XC3S2000	–2.33	–2.28	ns
			XC3S4000	–2.47	–2.42	ns
			XC3S5000	–2.66	–2.61	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32 and Table 35.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, *subtract* the appropriate adjustment from Table 44. If this is true of the data Input, *add* the appropriate Input adjustment from the same table.
3. This hold time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, *add* the appropriate Input adjustment from Table 44. If this is true of the data Input, *subtract* the appropriate Input adjustment from the same table. When the hold time is negative, it is possible to change the data before the clock's active edge.
4. DCM output jitter is included in all measurements.

Table 42: **Setup and Hold Times for the IOB Input Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Min	Min	
Setup Times						
T_{IOPICK}	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). No Input Delay is programmed.	LVCMOS25(2), IOBDELAY = NONE	XC3S50	1.65	1.89	ns
			XC3S200	1.37	1.57	ns
			XC3S400	1.37	1.57	ns
			XC3S1000	1.65	1.89	ns
			XC3S1500	1.65	1.89	ns
			XC3S2000	1.65	1.89	ns
			XC3S4000	1.73	1.99	ns
			XC3S5000	1.82	2.09	ns
$T_{IOPICKD}$	Time from the setup of data at the Input pin to the active transition at the IFF's ICLK input. The Input Delay is programmed.	LVCMOS25(2), IOBDELAY = IFD	XC3S50	4.39	5.04	ns
			XC3S200	4.76	5.47	ns
			XC3S400	4.63	5.32	ns
			XC3S1000	5.02	5.76	ns
			XC3S1500	5.40	6.20	ns
			XC3S2000	6.68	7.68	ns
			XC3S4000	7.16	8.24	ns
			XC3S5000	7.33	8.42	ns

Table 48: **Test Methods for Timing Measurement at I/Os *(Cont'd)***

Signal Standard (IOSTANDARD)		Inputs			Outputs		Inputs and Outputs
		V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
HSTL_III_18		1.1	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{REF}
HSTL_III_DCI_18							
LVCMOS12		-	0	1.2	1M	0	0.6
LVCMOS15		-	0	1.5	1M	0	0.75
LVDCI_15							
LVDCI_DV2_15							
HSLVDCI_15							
LVCMOS18		-	0	1.8	1M	0	0.9
LVDCI_18							
LVDCI_DV2_18							
HSLVDCI_18							
LVCMOS25		-	0	2.5	1M	0	1.25
LVDCI_25							
LVDCI_DV2_25							
HSLVDCI_25							
LVCMOS33		-	0	3.3	1M	0	1.65
LVDCI_33							
LVDCI_DV2_33							
HSLVDCI_33							
LVTTL		-	0	3.3	1M	0	1.4
PCI33_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
SSTL18_I		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL18_I_DCI							
SSTL18_II		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL2_I		1.25	V_{REF} – 0.75	V_{REF} + 0.75	50	1.25	V_{REF}
SSTL2_I_DCI							
SSTL2_II		1.25	V_{REF} – 0.75	V_{REF} + 0.75	25	1.25	V_{REF}
SSTL2_II_DCI					50	1.25	
Differential							
LDT_25 (ULVDS_25)		-	V_{ICM} – 0.125	V_{ICM} + 0.125	60	0.6	V_{ICM}
LVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVDS_25_DCI					N/A	N/A	
BLVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	1M	0	V_{ICM}
LVDSEXT_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVDSEXT_25_DCI					N/A	N/A	
LVPECL_25		-	V_{ICM} – 0.3	V_{ICM} + 0.3	1M	0	V_{ICM}
RSDS_25		-	V_{ICM} – 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}
DIFF_HSTL_II_18		-	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.8	V_{ICM}
DIFF_HSTL_II_18_DCI							

Date	Version	Description
05/25/07	2.2	Improved absolute maximum voltage specifications in Table 28, providing additional overshoot allowance. Improved XC3S50 HBM ESD to 2000V in Table 28. Based on extensive 90 nm production data, improved (reduced) the maximum quiescent current limits for the I_{CCINTQ} and I_{CCOQ} specifications in Table 34. Widened the recommended voltage range for the PCI standard and clarified the hysteresis footnote in Table 35. Noted restriction on combining differential outputs in Table 38. Updated footnote 1 in Table 64.
11/30/07	2.3	Updated 3.3V VCCO max from 3.45V to 3.465V in Table 32 and elsewhere. Reduced t_{ICCK} minimum from 0.50µs to 0.25µs in Table 65. Updated links to technical documentation.
06/25/08	2.4	Clarified dual marking. Added Mask and Fab Revisions. Added references to XAPP459 in Table 28 and Table 32. Removed absolute minimum and added footnote referring to timing analyzer for minimum delay values. Added HSLVDCI to Table 48 and Table 50. Updated t_{DICK} in Table 51 to match largest possible value in speed file. Updated formatting and links.
12/04/09	2.5	Updated notes 2 and 3 in Table 28. Removed silicon process specific information and revised notes in Table 30. Updated note 3 in Table 32. Updated note 3 in Table 34. Updated note 5 in Table 35. Updated V_{OL} max and V_{OH} min for SSTL2_II in Table 36. Updated note 5 in Table 36. Updated JTAG Waveforms in Figure 39. Updated V_{ICM} max for LVPECL_25 in Table 37. Updated RT and VT for LVDS_25_DCI in Table 48. Updated Simultaneously Switching Output Guidelines. Noted that the CP132 package is being discontinued in Table 49. Removed minimum values for T_{MULTCK} clock-to-output times in Table 54. Updated footnote 3 in Table 58. Removed minimum values for T_{MULT} propagation times in Table 55. Removed silicon process specific information and revised notes in Table 61. Updated Phase Shifter (PS).
10/29/12	3.0	Added Notice of Disclaimer. Per XCN07022, updated the discontinued FG1156 and FGG1156 package discussion throughout document. Per XCN08011, updated the discontinued CP132 and CPG132 package discussion throughout document. Revised description of V_{IN} in Table 32 and added note 7. Added note 4 to Table 33. This product is not recommended for new designs.

Differential Pair Labeling

A pin supports differential standards if the pin is labeled in the format “Lxxy_#”. The pin name suffix has the following significance. Figure 40 provides a specific example showing a differential input to and a differential output from Bank 2.

- ‘L’ indicates differential capability.
- "xx" is a two-digit integer, unique for each bank, that identifies a differential pin-pair.
- ‘y’ is replaced by ‘P’ for the true signal or ‘N’ for the inverted. These two pins form one differential pin-pair.
- ‘#’ is an integer, 0 through 7, indicating the associated I/O bank.

If unused, these pins are in a high impedance state. The Bitstream generator option UnusedPin enables a pull-up or pull-down resistor on all unused I/O pins.

Behavior from Power-On through End of Configuration

During the configuration process, all pins that are not actively involved in the configuration process are in a high-impedance state. The CONFIG- and JTAG-type pins have an internal pull-up resistor to VCCAUX during configuration. For all other I/O pins, the HSWAP_EN input determines whether or not pull-up resistors are activated during configuration. HSWAP_EN = 0 enables the pull-up resistors. HSWAP_EN = 1 disables the pull-up resistors allowing the pins to float, which is the desired state for hot-swap applications.

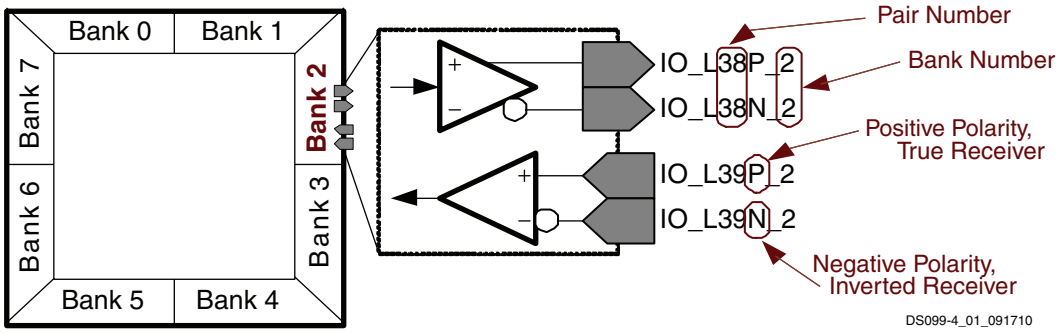


Figure 40: **Differential Pair Labelling**

DUAL Type: Dual-Purpose Configuration and I/O Pins

These pins serve dual purposes. The user-I/O pins are temporarily borrowed during the configuration process to load configuration data into the FPGA. After configuration, these pins are then usually available as a user I/O in the application. If a pin is not applicable to the specific configuration mode—controlled by the mode select pins M2, M1, and M0—then the pin behaves as an I/O-type pin.

There are 12 dual-purpose configuration pins on every package, six of which are part of I/O Bank 4, the other six part of I/O Bank 5. Only a few of the pins in Bank 4 are used in the Serial configuration modes.

See Pin Behavior During Configuration, page 122.

Serial Configuration Modes

This section describes the dual-purpose pins used during either Master or Slave Serial mode. See Table 75 for Mode Select pin settings required for Serial modes. All such pins are in Bank 4 and powered by VCCO_4.

In both the Master and Slave Serial modes, DIN is the serial configuration data input. The D1-D7 inputs are unused in serial mode and behave like general-purpose I/O pins.

In all the cases, the configuration data is synchronized to the rising edge of the CCLK clock signal.

The DIN, DOUT, and INIT_B pins can be retained in the application to support reconfiguration by setting the Persist bitstream generation option. However, the serial modes do not support device readback.

TQ144 Footprint

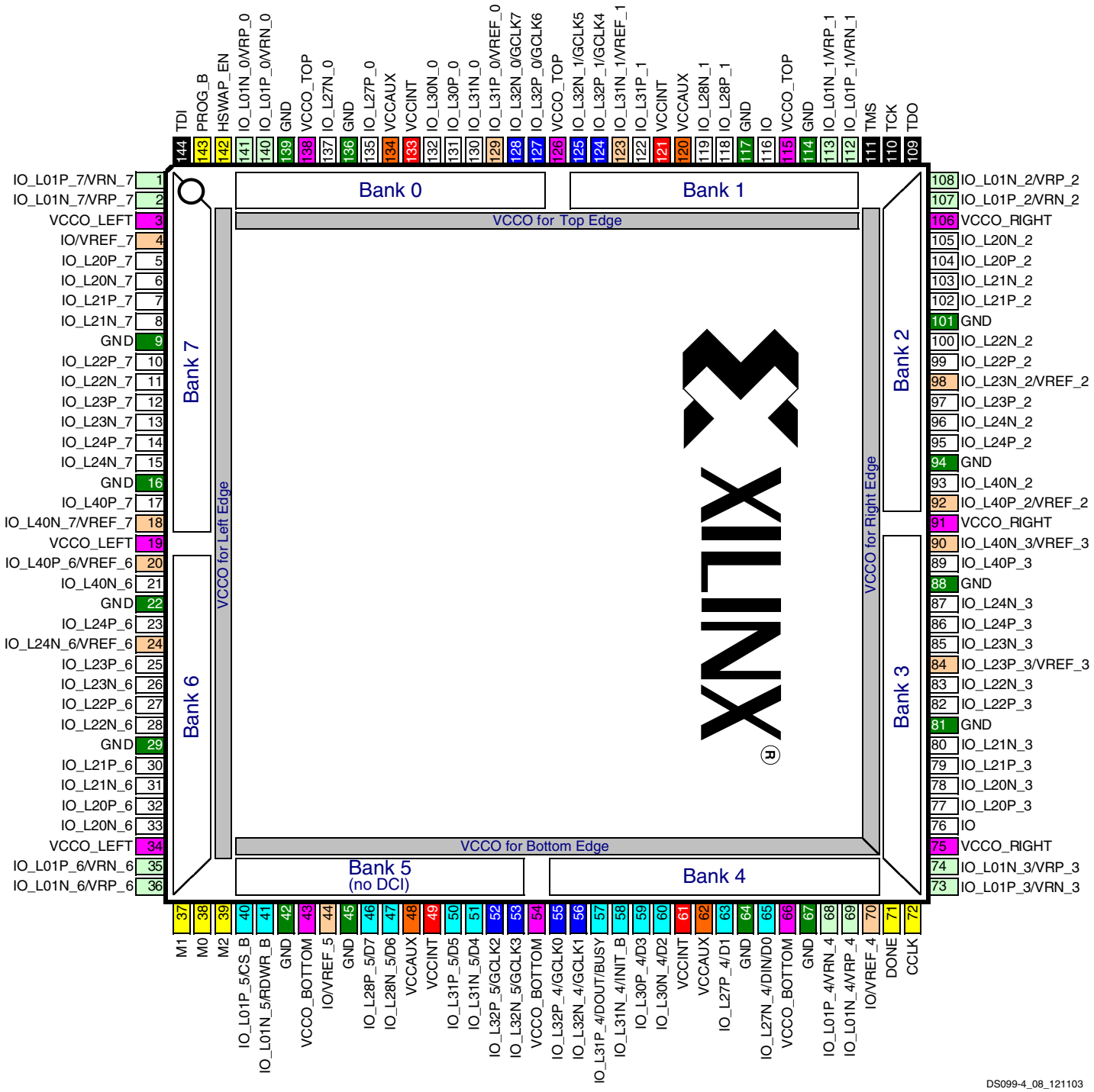


Figure 46: **TQ144 Package Footprint (Top View). Note pin 1 indicator in top-left corner and logo orientation.**

51 **I/O:** Unrestricted, general-purpose user I/O	12 **DUAL:** Configuration pin, then possible user I/O	12 **VREF:** User I/O or input voltage reference for bank
14 **DCI:** User I/O or reference resistor input for bank	8 **GCLK:** User I/O or global clock buffer input	12 **VCCO:** Output voltage supply for bank
7 **CONFIG:** Dedicated configuration pins	4 **JTAG:** Dedicated JTAG port pins	4 **VCCINT:** Internal core voltage supply (+1.2V)
0 **N.C.:** No unconnected pins in this package	16 **GND:** Ground	4 **VCCAUX:** Auxiliary voltage supply (+2.5V)

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
N/A	GND	J3	GND
N/A	GND	J8	GND
N/A	GND	K11	GND
N/A	GND	K16	GND
N/A	GND	K3	GND
N/A	GND	K8	GND
N/A	GND	L10	GND
N/A	GND	L11	GND
N/A	GND	L8	GND
N/A	GND	L9	GND
N/A	GND	M12	GND
N/A	GND	M7	GND
N/A	GND	N1	GND
N/A	GND	N18	GND
N/A	GND	T10	GND
N/A	GND	T9	GND
N/A	GND	U17	GND
N/A	GND	U2	GND
N/A	GND	V1	GND
N/A	GND	V13	GND
N/A	GND	V18	GND
N/A	GND	V6	GND
N/A	VCCAUX	B12	VCCAUX
N/A	VCCAUX	B7	VCCAUX
N/A	VCCAUX	G17	VCCAUX
N/A	VCCAUX	G2	VCCAUX
N/A	VCCAUX	M17	VCCAUX
N/A	VCCAUX	M2	VCCAUX
N/A	VCCAUX	U12	VCCAUX
N/A	VCCAUX	U7	VCCAUX
N/A	VCCINT	F12	VCCINT
N/A	VCCINT	F13	VCCINT
N/A	VCCINT	F6	VCCINT
N/A	VCCINT	F7	VCCINT
N/A	VCCINT	G13	VCCINT
N/A	VCCINT	G6	VCCINT
N/A	VCCINT	M13	VCCINT
N/A	VCCINT	M6	VCCINT
N/A	VCCINT	N12	VCCINT
N/A	VCCINT	N13	VCCINT

FG900: 900-lead Fine-pitch Ball Grid Array

The 900-lead fine-pitch ball grid array package, FG900, supports three different Spartan-3 devices, including the XC3S2000, the XC3S4000, and the XC3S5000. The footprints for the XC3S4000 and XC3S5000 are identical, as shown in Table 107 and Figure 55. The XC3S2000, however, has fewer I/O pins which consequently results in 68 unconnected pins on the FG900 package, labeled as “N.C.” In Table 107 and Figure 55, these unconnected pins are indicated with a black diamond symbol (◆).

All the package pins appear in Table 107 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

If there is a difference between the XC3S2000 pinout and the pinout for the XC3S4000 and XC3S5000, then that difference is highlighted in Table 107. If the table entry is shaded, then there is an unconnected pin on the XC3S2000 that maps to a user-I/O pin on the XC3S4000 and XC3S5000.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

Pinout Table

Table 107: **FG900 Package Pinout**

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
0	IO	IO	E15	I/O
0	IO	IO	K15	I/O
0	IO	IO	D13	I/O
0	IO	IO	K13	I/O
0	IO	IO	G8	I/O
0	IO/VREF_0	IO/VREF_0	F9	VREF
0	IO/VREF_0	IO/VREF_0	C4	VREF
0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	B4	DCI
0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	A4	DCI
0	IO_L02N_0	IO_L02N_0	B5	I/O
0	IO_L02P_0	IO_L02P_0	A5	I/O
0	IO_L03N_0	IO_L03N_0	D5	I/O
0	IO_L03P_0	IO_L03P_0	E6	I/O
0	IO_L04N_0	IO_L04N_0	C6	I/O
0	IO_L04P_0	IO_L04P_0	B6	I/O
0	IO_L05N_0	IO_L05N_0	F6	I/O
0	IO_L05P_0/VREF_0	IO_L05P_0/VREF_0	F7	VREF
0	IO_L06N_0	IO_L06N_0	D7	I/O
0	IO_L06P_0	IO_L06P_0	C7	I/O
0	IO_L07N_0	IO_L07N_0	F8	I/O
0	IO_L07P_0	IO_L07P_0	E8	I/O
0	IO_L08N_0	IO_L08N_0	D8	I/O
0	IO_L08P_0	IO_L08P_0	C8	I/O
0	IO_L09N_0	IO_L09N_0	B8	I/O
0	IO_L09P_0	IO_L09P_0	A8	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
2	IO_L28N_2	IO_L28N_2	M26	I/O
2	IO_L28P_2	IO_L28P_2	N25	I/O
2	IO_L29N_2	IO_L29N_2	N26	I/O
2	IO_L29P_2	IO_L29P_2	N27	I/O
2	IO_L31N_2	IO_L31N_2	N29	I/O
2	IO_L31P_2	IO_L31P_2	N30	I/O
2	IO_L32N_2	IO_L32N_2	P21	I/O
2	IO_L32P_2	IO_L32P_2	P22	I/O
2	IO_L33N_2	IO_L33N_2	P24	I/O
2	IO_L33P_2	IO_L33P_2	P25	I/O
2	IO_L34N_2/VREF_2	IO_L34N_2/VREF_2	P28	VREF
2	IO_L34P_2	IO_L34P_2	P29	I/O
2	IO_L35N_2	IO_L35N_2	R21	I/O
2	IO_L35P_2	IO_L35P_2	R22	I/O
2	IO_L37N_2	IO_L37N_2	R23	I/O
2	IO_L37P_2	IO_L37P_2	R24	I/O
2	IO_L38N_2	IO_L38N_2	R25	I/O
2	IO_L38P_2	IO_L38P_2	R26	I/O
2	IO_L39N_2	IO_L39N_2	R27	I/O
2	IO_L39P_2	IO_L39P_2	R28	I/O
2	IO_L40N_2	IO_L40N_2	R29	I/O
2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	R30	VREF
2	N.C. (◆)	IO_L41N_2	E27	I/O
2	N.C. (◆)	IO_L41P_2	F26	I/O
2	N.C. (◆)	IO_L45N_2	K28	I/O
2	N.C. (◆)	IO_L45P_2	K29	I/O
2	N.C. (◆)	IO_L46N_2	K21	I/O
2	N.C. (◆)	IO_L46P_2	L21	I/O
2	N.C. (◆)	IO_L47N_2	L23	I/O
2	N.C. (◆)	IO_L47P_2	L24	I/O
2	N.C. (◆)	IO_L50N_2	M29	I/O
2	N.C. (◆)	IO_L50P_2	M30	I/O
2	VCCO_2	VCCO_2	M20	VCCO
2	VCCO_2	VCCO_2	N20	VCCO
2	VCCO_2	VCCO_2	P20	VCCO
2	VCCO_2	VCCO_2	L22	VCCO
2	VCCO_2	VCCO_2	J24	VCCO
2	VCCO_2	VCCO_2	N24	VCCO
2	VCCO_2	VCCO_2	G26	VCCO
2	VCCO_2	VCCO_2	E28	VCCO

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
N/A	GND	GND	R17	GND
N/A	GND	GND	T17	GND
N/A	GND	GND	U17	GND
N/A	GND	GND	V17	GND
N/A	GND	GND	AC17	GND
N/A	GND	GND	AF17	GND
N/A	GND	GND	AK17	GND
N/A	GND	GND	N18	GND
N/A	GND	GND	P18	GND
N/A	GND	GND	R18	GND
N/A	GND	GND	T18	GND
N/A	GND	GND	U18	GND
N/A	GND	GND	V18	GND
N/A	GND	GND	R19	GND
N/A	GND	GND	T19	GND
N/A	GND	GND	A21	GND
N/A	GND	GND	E21	GND
N/A	GND	GND	H21	GND
N/A	GND	GND	AC21	GND
N/A	GND	GND	AF21	GND
N/A	GND	GND	AK21	GND
N/A	GND	GND	K23	GND
N/A	GND	GND	P23	GND
N/A	GND	GND	U23	GND
N/A	GND	GND	AA23	GND
N/A	GND	GND	A25	GND
N/A	GND	GND	AK25	GND
N/A	GND	GND	E26	GND
N/A	GND	GND	K26	GND
N/A	GND	GND	P26	GND
N/A	GND	GND	U26	GND
N/A	GND	GND	AA26	GND
N/A	GND	GND	AF26	GND
N/A	GND	GND	A29	GND
N/A	GND	GND	B29	GND
N/A	GND	GND	AJ29	GND
N/A	GND	GND	AK29	GND
N/A	GND	GND	A30	GND
N/A	GND	GND	B30	GND
N/A	GND	GND	F30	GND

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
N/A	VCCINT	VCCINT	V12	VCCINT
N/A	VCCINT	VCCINT	W12	VCCINT
N/A	VCCINT	VCCINT	M13	VCCINT
N/A	VCCINT	VCCINT	W13	VCCINT
N/A	VCCINT	VCCINT	M14	VCCINT
N/A	VCCINT	VCCINT	W14	VCCINT
N/A	VCCINT	VCCINT	L15	VCCINT
N/A	VCCINT	VCCINT	Y15	VCCINT
N/A	VCCINT	VCCINT	L16	VCCINT
N/A	VCCINT	VCCINT	Y16	VCCINT
N/A	VCCINT	VCCINT	M17	VCCINT
N/A	VCCINT	VCCINT	W17	VCCINT
N/A	VCCINT	VCCINT	M18	VCCINT
N/A	VCCINT	VCCINT	W18	VCCINT
N/A	VCCINT	VCCINT	M19	VCCINT
N/A	VCCINT	VCCINT	N19	VCCINT
N/A	VCCINT	VCCINT	P19	VCCINT
N/A	VCCINT	VCCINT	U19	VCCINT
N/A	VCCINT	VCCINT	V19	VCCINT
N/A	VCCINT	VCCINT	W19	VCCINT
N/A	VCCINT	VCCINT	L20	VCCINT
N/A	VCCINT	VCCINT	R20	VCCINT
N/A	VCCINT	VCCINT	T20	VCCINT
N/A	VCCINT	VCCINT	Y20	VCCINT
VCCAUX	CCLK	CCLK	AH28	CONFIG
VCCAUX	DONE	DONE	AJ28	CONFIG
VCCAUX	HSWAP_EN	HSWAP_EN	A3	CONFIG
VCCAUX	M0	M0	AJ3	CONFIG
VCCAUX	M1	M1	AH3	CONFIG
VCCAUX	M2	M2	AK3	CONFIG
VCCAUX	PROG_B	PROG_B	B3	CONFIG
VCCAUX	TCK	TCK	B28	JTAG
VCCAUX	TDI	TDI	C3	JTAG
VCCAUX	TDO	TDO	C28	JTAG
VCCAUX	TMS	TMS	A28	JTAG

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
2	IO_L19N_2	IO_L19N_2	M29	I/O
2	IO_L19P_2	IO_L19P_2	M30	I/O
2	IO_L20N_2	IO_L20N_2	M31	I/O
2	IO_L20P_2	IO_L20P_2	M32	I/O
2	IO_L21N_2	IO_L21N_2	M26	I/O
2	IO_L21P_2	IO_L21P_2	N25	I/O
2	IO_L22N_2	IO_L22N_2	N27	I/O
2	IO_L22P_2	IO_L22P_2	N28	I/O
2	IO_L23N_2/VREF_2	IO_L23N_2VREF_2	N31	VREF
2	IO_L23P_2	IO_L23P_2	N32	I/O
2	IO_L24N_2	IO_L24N_2	N24	I/O
2	IO_L24P_2	IO_L24P_2	P24	I/O
2	IO_L26N_2	IO_L26N_2	P29	I/O
2	IO_L26P_2	IO_L26P_2	P30	I/O
2	IO_L27N_2	IO_L27N_2	P31	I/O
2	IO_L27P_2	IO_L27P_2	P32	I/O
2	IO_L28N_2	IO_L28N_2	P33	I/O
2	IO_L28P_2	IO_L28P_2	P34	I/O
2	IO_L29N_2	IO_L29N_2	R24	I/O
2	IO_L29P_2	IO_L29P_2	R25	I/O
2	IO_L30N_2	IO_L30N_2	R28	I/O
2	IO_L30P_2	IO_L30P_2	R29	I/O
2	IO_L31N_2	IO_L31N_2	R31	I/O
2	IO_L31P_2	IO_L31P_2	R32	I/O
2	IO_L32N_2	IO_L32N_2	R33	I/O
2	IO_L32P_2	IO_L32P_2	R34	I/O
2	IO_L33N_2	IO_L33N_2	R26	I/O
2	IO_L33P_2	IO_L33P_2	T25	I/O
2	IO_L34N_2/VREF_2	IO_L34N_2/VREF_2	T28	VREF
2	IO_L34P_2	IO_L34P_2	T29	I/O
2	IO_L35N_2	IO_L35N_2	T32	I/O
2	IO_L35P_2	IO_L35P_2	T33	I/O
2	IO_L37N_2	IO_L37N_2	U27	I/O
2	IO_L37P_2	IO_L37P_2	U28	I/O
2	IO_L38N_2	IO_L38N_2	U29	I/O
2	IO_L38P_2	IO_L38P_2	U30	I/O
2	IO_L39N_2	IO_L39N_2	U31	I/O
2	IO_L39P_2	IO_L39P_2	U32	I/O
2	IO_L40N_2	IO_L40N_2	U33	I/O
2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	U34	VREF

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
4	IO_L01N_4/VRP_4	IO_L01N_4/VRP_4	AN32	DCI
4	IO_L01P_4/VRN_4	IO_L01P_4/VRN_4	AP32	DCI
4	IO_L02N_4	IO_L02N_4	AN31	I/O
4	IO_L02P_4	IO_L02P_4	AP31	I/O
4	IO_L03N_4	IO_L03N_4	AM30	I/O
4	IO_L03P_4	IO_L03P_4	AN30	I/O
4	IO_L04N_4	IO_L04N_4	AN27	I/O
4	IO_L04P_4	IO_L04P_4	AP27	I/O
4	IO_L05N_4	IO_L05N_4	AH26	I/O
4	IO_L05P_4	IO_L05P_4	AJ26	I/O
4	IO_L06N_4/VREF_4	IO_L06N_4/VREF_4	AL26	VREF
4	IO_L06P_4	IO_L06P_4	AM26	I/O
4	IO_L07N_4	IO_L07N_4	AF25	I/O
4	IO_L07P_4	IO_L07P_4	AG25	I/O
4	IO_L08N_4	IO_L08N_4	AH25	I/O
4	IO_L08P_4	IO_L08P_4	AJ25	I/O
4	IO_L09N_4	IO_L09N_4	AL25	I/O
4	IO_L09P_4	IO_L09P_4	AM25	I/O
4	IO_L10N_4	IO_L10N_4	AN25	I/O
4	IO_L10P_4	IO_L10P_4	AP25	I/O
4	IO_L11N_4	IO_L11N_4	AD23	I/O
4	IO_L11P_4	IO_L11P_4	AE23	I/O
4	IO_L12N_4	IO_L12N_4	AF23	I/O
4	IO_L12P_4	IO_L12P_4	AG23	I/O
4	IO_L13N_4	IO_L13N_4	AJ23	I/O
4	IO_L13P_4	IO_L13P_4	AK23	I/O
4	IO_L14N_4	IO_L14N_4	AL23	I/O
4	IO_L14P_4	IO_L14P_4	AM23	I/O
4	IO_L15N_4	IO_L15N_4	AN23	I/O
4	IO_L15P_4	IO_L15P_4	AP23	I/O
4	IO_L16N_4	IO_L16N_4	AG22	I/O
4	IO_L16P_4	IO_L16P_4	AH22	I/O
4	IO_L17N_4	IO_L17N_4	AL22	I/O
4	IO_L17P_4	IO_L17P_4	AM22	I/O
4	IO_L18N_4	IO_L18N_4	AD21	I/O
4	IO_L18P_4	IO_L18P_4	AE21	I/O
4	IO_L19N_4	IO_L19N_4	AG21	I/O
4	IO_L19P_4	IO_L19P_4	AH21	I/O
4	IO_L20N_4	IO_L20N_4	AJ21	I/O
4	IO_L20P_4	IO_L20P_4	AK21	I/O

User I/Os by Bank

Note: The FG(G)1156 package is discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

Table 111 indicates how the available user-I/O pins are distributed between the eight I/O banks for the XC3S4000 in the FG1156 package. Similarly, Table 112 shows how the available user-I/O pins are distributed between the eight I/O banks for the XC3S5000 in the FG1156 package.

Table 111: **User I/Os Per Bank for XC3S4000 in FG1156 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	90	79	0	2	7	2
	1	90	79	0	2	7	2
Right	2	88	80	0	2	6	0
	3	88	79	0	2	7	0
Bottom	4	90	73	6	2	7	2
	5	90	73	6	2	7	2
Left	6	88	79	0	2	7	0
	7	88	79	0	2	7	0

Notes:

1. The FG1156 and FGG1156 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.

Table 112: **User I/Os Per Bank for XC3S5000 in FG1156 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	100	89	0	2	7	2
	1	100	89	0	2	7	2
Right	2	96	87	0	2	7	0
	3	96	87	0	2	7	0
Bottom	4	100	83	6	2	7	2
	5	100	83	6	2	7	2
Left	6	96	87	0	2	7	0
	7	96	87	0	2	7	0

Notes:

1. The FG1156 and FGG1156 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.

Revision History

Date	Version	Description
04/03/03	1.0	Initial Xilinx release.
04/21/03	1.1	Added information on the VQ100 package footprint, including a complete pinout table (Table 87) and footprint diagram (Figure 44). Updated Table 85 with final I/O counts for the VQ100 package. Also added final differential I/O pair counts for the TQ144 package. Added clarifying comments to HSWAP_EN pin description on page 119. Updated the footprint diagram for the FG900 package shown in Figure 55a and Figure 55b. Some thick lines separating I/O banks were incorrect. Made cosmetic changes to Figure 40, Figure 42, and Figure 43. Updated Xilinx hypertext links. Added XC3S200 and XC3S400 to Pin Name column in Table 91.
05/12/03	1.1.1	AM32 pin was missing GND label in FG1156 package diagram (Figure 53).
07/11/03	1.1.2	Corrected misspellings of GCLK in Table 69 and Table 70. Changed CMOS25 to LVCMOS25 in Dual-Purpose Pin I/O Standard During Configuration section. Clarified references to Module 2. For XC3S5000 in FG1156 package, corrected N.C. symbol to a black square in Table 110, key, and package drawing.
07/29/03	1.2	Corrected pin names on FG1156 package. Some package balls incorrectly included LVDS pair names. The affected balls on the FG1156 package include G1, G2, G33, G34, U9, U10, U25, U26, V9, V10, V25, V26, AH1, AH2, AH33, AH34. The number of LVDS pairs is unaffected. Modified affected balls and re-sorted rows in Table 110. Updated affected balls in Figure 53. Also updated ASCII and Excel electronic versions of FG1156 pinout.
08/19/03	1.2.1	Removed 100 MHz ConfigRate option in CCLK: Configuration Clock section and in Table 80. Added note that TDO is a totem-pole output in Table 77.
10/09/03	1.2.2	Some pins had incorrect bank designations and were improperly sorted in Table 93. No pin names or functions changed. Renamed DCI_IN to DCI and added black diamond to N.C. pins in Table 93. In Figure 47, removed some extraneous text from pin 106 and corrected spelling of pins 45, 48, and 81.
12/17/03	1.3	Added FG320 pin tables and pinout diagram (FG320: 320-lead Fine-pitch Ball Grid Array). Made cosmetic changes to the TQ144 footprint (Figure 46), the PQ208 footprint (Figure 47), the FG676 footprint (Figure 53), and the FG900 footprint (Figure 55). Clarified wording in Precautions When Using the JTAG Port in 3.3V Environments section.
02/27/04	1.4	Clarified wording in Using JTAG Port After Configuration section. In Table 81, reduced package height for FG320 and increased maximum I/O values for the FG676, FG900, and FG1156 packages.
07/13/04	1.5	Added information on lead-free (Pb-free) package options to the Package Overview section plus Table 81 and Table 83. Clarified the VRN_# reference resistor requirements for I/O standards that use single termination as described in the DCI Termination Types section and in Figure 42b. Graduated from Advance Product Specification to Product Specification.
08/24/04	1.5.1	Removed XC3S2000 references from FG1156: 1156-lead Fine-pitch Ball Grid Array.
01/17/05	1.6	Added XC3S50 in CP132 package option. Added XC3S2000 in FG456 package option. Added XC3S4000 in FG676 package option. Added Selecting the Right Package Option section. Modified or added Table 81, Table 83, Table 84, Table 85, Table 89, Table 90, Table 100, Table 102, Table 103, Table 106, Figure 45, and Figure 53.
08/19/05	1.7	Removed term “weak” from the description of pull-up and pull-down resistors. Added IDCODE Register values. Added signal integrity precautions to CCLK: Configuration Clock and indicated that CCLK should be treated as an I/O during Master mode in Table 79.
04/03/06	2.0	Added Package Thermal Characteristics. Updated Figure 41 to make it a more obvious example. Added detail about which pins have dedicated pull-up resistors during configuration, regardless of the HSWAP_EN value to Table 70 and to Pin Behavior During Configuration. Updated Precautions When Using the JTAG Port in 3.3V Environments.
04/26/06	2.1	Corrected swapped data row in Table 86. The Theta-JA with zero airflow column was swapped with the Theta-JC column. Made additional notations on CONFIG and JTAG pins that have pull-up resistors during configuration, regardless of the HSWAP_EN input.
05/25/07	2.2	Added link on page 128 to Material Declaration Data Sheets. Corrected units typo in Table 74. Added Note 1 to Table 103 about VREF for XC3S1500 in FG676.