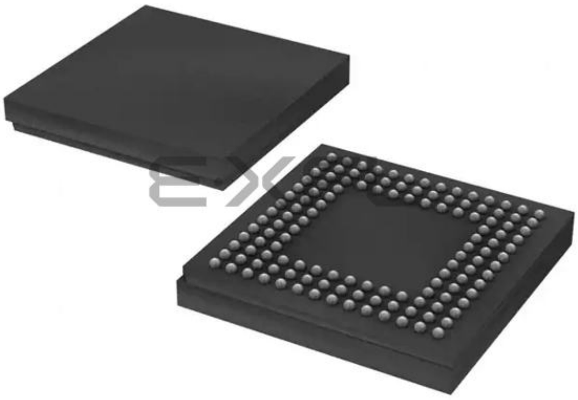
AMD Xilinx - XC3S50-4CPG132C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	192
Number of Logic Elements/Cells	1728
Total RAM Bits	73728
Number of I/O	89
Number of Gates	50000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	132-TFBGA, CSPBGA
Supplier Device Package	132-CSPBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s50-4cpg132c

power, the configuration data is written to the FPGA using any of five different modes: Master Parallel, Slave Parallel, Master Serial, Slave Serial, and Boundary Scan (JTAG). The Master and Slave Parallel modes use an 8-bit-wide SelectMAP port.

The recommended memory for storing the configuration data is the low-cost Xilinx Platform Flash PROM family, which includes the XCF00S PROMs for serial configuration and the higher density XCF00P PROMs for parallel or serial configuration.

I/O Capabilities

The SelectIO feature of Spartan-3 devices supports eighteen single-ended standards and eight differential standards as listed in Table 2. Many standards support the DCI feature, which uses integrated terminations to eliminate unwanted signal reflections.

Table 2: **Signal Standards Supported by the Spartan-3 Family**

Standard Category	Description	V_{CCO} (V)	Class	Symbol (IOSTANDARD)	DCI Option
Single-Ended					
GTL	Gunning Transceiver Logic	N/A	Terminated	GTL	Yes
			Plus	GTLP	Yes
HSTL	High-Speed Transceiver Logic	1.5	I	HSTL_I	Yes
			III	HSTL_III	Yes
		1.8	I	HSTL_I_18	Yes
			II	HSTL_II_18	Yes
			III	HSTL_III_18	Yes
LVCMOS	Low-Voltage CMOS	1.2	N/A	LVCMOS12	No
		1.5	N/A	LVCMOS15	Yes
		1.8	N/A	LVCMOS18	Yes
		2.5	N/A	LVCMOS25	Yes
		3.3	N/A	LVCMOS33	Yes
LVTTL	Low-Voltage Transistor-Transistor Logic	3.3	N/A	LVTTL	No
PCI	Peripheral Component Interconnect	3.0	33 MHz[(1)]	PCI33_3	No
SSTL	Stub Series Terminated Logic	1.8	N/A (±6.7 mA)	SSTL18_I	Yes
			N/A (±13.4 mA)	SSTL18_II	No
		2.5	I	SSTL2_I	Yes
			II	SSTL2_II	Yes
Differential					
LDT (ULVDS)	Lightning Data Transport (HyperTransport™) Logic	2.5	N/A	LDT_25	No
LVDS	Low-Voltage Differential Signaling		Standard	LVDS_25	Yes
			Bus	BLVDS_25	No
			Extended Mode	LVDSEXT_25	Yes
LVPECL	Low-Voltage Positive Emitter-Coupled Logic	2.5	N/A	LVPECL_25	No
RSDS	Reduced-Swing Differential Signaling	2.5	N/A	RSDS_25	No
HSTL	Differential High-Speed Transceiver Logic	1.8	II	DIFF_HSTL_II_18	Yes
SSTL	Differential Stub Series Terminated Logic	2.5	II	DIFF_SSTL2_II	Yes

Notes:

1. 66 MHz PCI is not supported by the Xilinx IP core although PCI66_3 is an available I/O standard.

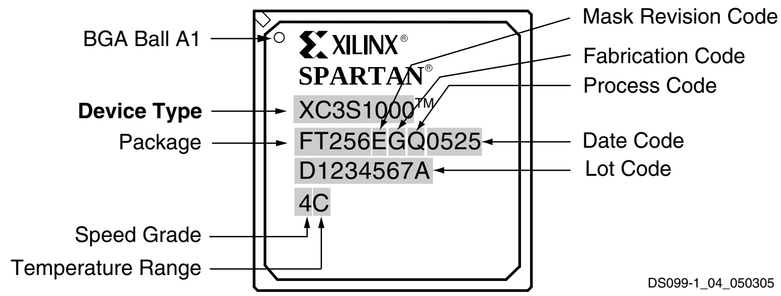

Figure 3: **Spartan-3 FPGA BGA Package Marking Example for Part Number XC3S1000-4FT256C**

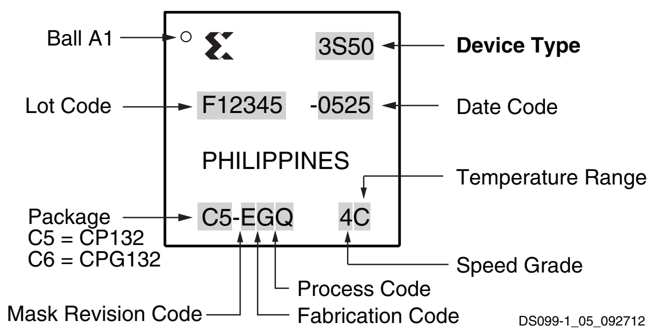

Figure 4: **Spartan-3 FPGA CP132 and CPG132 Package Marking Example for XC3S50-4CP132C**

Ordering Information

Spartan-3 FPGAs are available in both standard (Figure 5) and Pb-free (Figure 6) packaging options for all device/package combinations. The Pb-free packages include a special 'G' character in the ordering code.

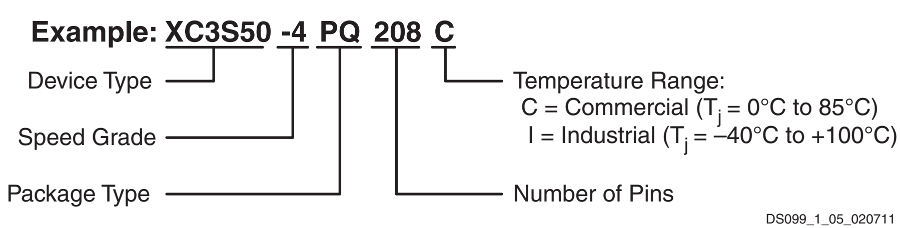

Figure 5: **Standard Packaging**

For additional information on Pb-free packaging, see XAPP427: *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

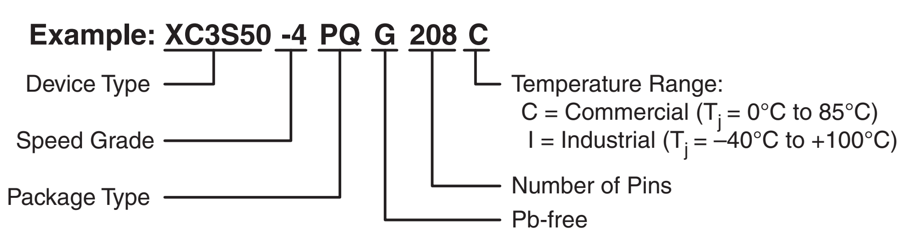

Figure 6: **Pb-Free Packaging**

Table 28: **Absolute Maximum Ratings *(Cont'd)***

Symbol	Description	Conditions	Min	Max	Units
I_{IK}	Input clamp current per I/O pin	$-0.5\ V < V_{IN} < (V_{CCO} + 0.5\ V)$	–	±100	mA
V_{ESD}	Electrostatic Discharge Voltage pins relative to GND	Human body model	–	±2000	V
		Charged device model	–	±500	V
		Machine model	–	±200	V
T_J	Junction temperature		–	125	°C
T_{SOL}	Soldering temperature[4]		–	220	°C
T_{STG}	Storage temperature		–65	150	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time adversely affects device reliability.
2. All User I/O and Dual-Purpose pins (DIN/D0, D1–D7, CS_B, RDWR_B, BUSY/DOUT, and INIT_B) draw power from the V_{CCO} power rail of the associated bank. Keeping VIN within 500 mV of the associated V_{CCO} rails or ground rail ensures that the internal diode junctions that exist between each of these pins and the V_{CCO} and GND rails do not turn on. Table 32 specifies the V_{CCO} range used to determine the max limit. Input voltages outside the –0.5V to V_{CCO}+0.5V voltage range are permissible provided that the I_{IK} input clamp diode rating is met and no more than 100 pins exceed the range simultaneously. Prolonged exposure to such current may compromise device reliability. A sustained current of 10 mA will not compromise device reliability. See XAPP459, *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Generation FPGAs* for more details. The VIN limits apply to both the DC and AC components of signals. Simple application solutions are available that show how to handle overshoot/undershoot as well as achieve PCI compliance. Refer to the following application notes: XAPP457, *Powering and Configuring Spartan-3 Generation FPGAs in Compliant PCI Applications* and XAPP659, *Virtex®-II Pro / Virtex-II Pro X 3.3V I/O Design Guidelines*.
3. All Dedicated pins (M0–M2, CCLK, PROG_B, DONE, HSWAP_EN, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail (2.5V). Meeting the V_{IN} max limit ensures that the internal diode junctions that exist between each of these pins and the V_{CCAUX} rail do not turn on. Table 32 specifies the V_{CCAUX} range used to determine the max limit. When V_{CCAUX} is at its maximum recommended operating level (2.625V), V_{IN} max < 3.125V. As long as the V_{IN} max specification is met, oxide stress is not possible. For information concerning the use of 3.3V signals, see the 3.3V-Tolerant Configuration Interface, page 47. See also XAPP459.
4. For soldering guidelines, see UG112, *Device Packaging and Thermal Characteristics* and XAPP427, *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

Table 29: **Supply Voltage Thresholds for Power-On Reset**

Symbol	Description	Min	Max	Units
V_{CCINTT}	Threshold for the V_{CCINT} supply	0.4	1.0	V
V_{CCAUXT}	Threshold for the V_{CCAUX} supply	0.8	2.0	V
V_{CCO4T}	Threshold for the V_{CCO} Bank 4 supply	0.4	1.0	V

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies may be applied in any order. When applying V_{CCINT} power before V_{CCAUX} power, the FPGA may draw a *surplus* current in addition to the quiescent current levels specified in Table 34. Applying V_{CCAUX} eliminates the surplus current. The FPGA does not use any of the surplus current for the power-on process. For this power sequence, make sure that regulators with foldback features will not shut down inadvertently.
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 4, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.
3. If a brown-out condition occurs where V_{CCAUX} or V_{CCINT} drops below the retention voltage indicated in Table 31, then V_{CCAUX} or V_{CCINT} must drop below the minimum power-on reset voltage in order to clear out the device configuration content.

Table 42: **Setup and Hold Times for the IOB Input Path *(Cont'd)***

Symbol	Description	Conditions	Device	Speed Grade -5 Min	Speed Grade -4 Min	Units
Hold Times						
T_{IOICKP}	Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. No Input Delay is programmed.	LVCMOS25[(3)], IOBDELAY = NONE	XC3S50	-0.55	-0.55	ns
			XC3S200	-0.29	-0.29	ns
			XC3S400	-0.29	-0.29	ns
			XC3S1000	-0.55	-0.55	ns
			XC3S1500	-0.55	-0.55	ns
			XC3S2000	-0.55	-0.55	ns
			XC3S4000	-0.61	-0.61	ns
			XC3S5000	-0.68	-0.68	ns
$T_{IOICKPD}$	Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. The Input Delay is programmed.	LVCMOS25[(3)], IOBDELAY = IFD	XC3S50	-2.74	-2.74	ns
			XC3S200	-3.00	-3.00	ns
			XC3S400	-2.90	-2.90	ns
			XC3S1000	-3.24	-3.24	ns
			XC3S1500	-3.55	-3.55	ns
			XC3S2000	-4.57	-4.57	ns
			XC3S4000	-4.96	-4.96	ns
			XC3S5000	-5.09	-5.09	ns
Set/Reset Pulse Width						
T_{RPW_IOB}	Minimum pulse width to SR control input on IOB		All	0.66	0.76	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32 and Table 35.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, add the appropriate Input adjustment from Table 44.
3. These hold times require adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, subtract the appropriate Input adjustment from Table 44. When the hold time is negative, it is possible to change the data before the clock's active edge.

Table 44: **Input Timing Adjustments for IOB *(Cont'd)***

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
LVCMOS15	0.42	0.49	ns
LVDCI_15	0.38	0.43	ns
LVDCI_DV2_15	0.38	0.44	ns
LVCMOS18	0.24	0.28	ns
LVDCI_18	0.29	0.33	ns
LVDCI_DV2_18	0.28	0.33	ns
LVCMOS25	0	0	ns
LVDCI_25	0.05	0.05	ns
LVDCI_DV2_25	0.04	0.04	ns
LVCMOS33, LVDCI_33, LVDCI_DV2_33	–0.05	–0.02	ns
LVTTL	0.18	0.21	ns
PCI33_3	0.20	0.22	ns
SSTL18_I, SSTL18_I_DCI	0.39	0.45	ns
SSTL18_II	0.39	0.45	ns
SSTL2_I, SSTL2_I_DCI	0.40	0.46	ns
SSTL2_II, SSTL2_II_DCI	0.36	0.41	ns
Differential Standards			
LDT_25 (ULVDS_25)	0.76	0.88	ns
LVDS_25, LVDS_25_DCI	0.65	0.75	ns
BLVDS_25	0.34	0.39	ns
LVDSEXT_25, LVDSEXT_25_DCI	0.80	0.92	ns
LVPECL_25	0.18	0.21	ns
RSDS_25	0.43	0.50	ns
DIFF_HSTL_II_18, DIFF_HSTL_II_18_DCI	0.34	0.39	ns
DIFF_SSTL2_II, DIFF_SSTL2_II_DCI	0.65	0.75	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32, Table 35, and Table 37.
2. These adjustments are used to convert input path times originally specified for the LVCMOS25 standard to times that correspond to other signal standards.

Table 54: **Synchronous 18 x 18 Multiplier Timing**

Symbol	Description	P Outputs	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Clock-to-Output Times							
T_{MULTCK}	When reading from the Multiplier, the time from the active transition at the C clock input to data appearing at the P outputs	P[0]	–	1.00	–	1.15	ns
		P[15]	–	1.15	–	1.32	ns
		P[17]	–	1.30	–	1.50	ns
		P[19]	–	1.45	–	1.67	ns
		P[23]	–	1.76	–	2.02	ns
		P[31]	–	2.37	–	2.72	ns
		P[35]	–	2.67	–	3.07	ns
Setup Times							
$T_{MULIDCK}$	Time from the setup of data at the A and B inputs to the active transition at the C input of the Multiplier	-	1.84	–	2.11	–	ns
Hold Times							
$T_{MULCKID}$	Time from the active transition at the Multiplier's C input to the point where data is last held at the A and B inputs	-	0	–	0	–	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32.

Table 55: **Asynchronous 18 x 18 Multiplier Timing**

Symbol	Description	P Outputs	Speed Grade		Units
			-5	-4	
			Max	Max	
Propagation Times					
T_{MULT}	The time it takes for data to travel from the A and B inputs to the P outputs	P[0]	1.55	1.78	ns
		P[15]	3.15	3.62	ns
		P[17]	3.36	3.86	ns
		P[19]	3.49	4.01	ns
		P[23]	3.73	4.29	ns
		P[31]	4.23	4.86	ns
		P[35]	4.47	5.14	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32.

Package Overview

Table 81 shows the 10 low-cost, space-saving production package styles for the Spartan-3 family. Each package style is available as a standard and an environmentally-friendly lead-free (Pb-free) option. The Pb-free packages include an extra 'G' in the package style name. For example, the standard "VQ100" package becomes "VQG100" when ordered as the Pb-free option. The mechanical dimensions of the standard and Pb-free packages are similar, as shown in the mechanical drawings provided in Table 83.

Not all Spartan-3 device densities are available in all packages. However, for a specific package there is a common footprint that supports the various devices available in that package. See the footprint diagrams that follow.

Table 81: **Spartan-3 Family Package Options**

Package	Leads	Type	Maximum I/O	Pitch (mm)	Footprint (mm)	Height (mm)
VQ100 / VQG100	100	Very-thin Quad Flat Pack	63	0.5	16 x 16	1.20
CP132 / CPG132(1)	132	Chip-Scale Package	89	0.5	8 x 8	1.10
TQ144 / TQG144	144	Thin Quad Flat Pack	97	0.5	22 x 22	1.60
PQ208 / PQG208	208	Quad Flat Pack	141	0.5	30.6 x 30.6	4.10
FT256 / FTG256	256	Fine-pitch, Thin Ball Grid Array	173	1.0	17 x 17	1.55
FG320 / FGG320	320	Fine-pitch Ball Grid Array	221	1.0	19 x 19	2.00
FG456 / FGG456	456	Fine-pitch Ball Grid Array	333	1.0	23 x 23	2.60
FG676 / FGG676	676	Fine-pitch Ball Grid Array	489	1.0	27 x 27	2.60
FG900 / FGG900	900	Fine-pitch Ball Grid Array	633	1.0	31 x 31	2.60
FG1156 / FGG1156(1)	1156	Fine-pitch Ball Grid Array	784	1.0	35 x 35	2.60

Notes:
1. The CP132, CPG132, FG1156, and FGG1156 packages are discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

Selecting the Right Package Option

Spartan-3 FPGAs are available in both quad-flat pack (QFP) and ball grid array (BGA) packaging options. While QFP packaging offers the lowest absolute cost, the BGA packages are superior in almost every other aspect, as summarized in Table 82. Consequently, Xilinx recommends using BGA packaging whenever possible.

Table 82: **Comparing Spartan-3 Device Packaging Options**

Characteristic	Quad Flat-Pack (QFP)	Ball Grid Array (BGA)
Maximum User I/O	141	633
Packing Density (Logic/Area)	Good	Better
Signal Integrity	Fair	Better
Simultaneous Switching Output (SSO) Support	Limited	Better
Thermal Dissipation	Fair	Better
Minimum Printed Circuit Board (PCB) Layers	4	6
Hand Assembly/Rework	Possible	Very Difficult

TQ144: 144-lead Thin Quad Flat Package

The XC3S50, the XC3S200, and the XC3S400 are available in the 144-lead thin quad flat package, TQ144. All devices share a common footprint for this package as shown in Table 91 and Figure 46.

The TQ144 package only has four separate VCCO inputs, unlike the BGA packages, which have eight separate VCCO inputs. The TQ144 package has a separate VCCO input for the top, bottom, left, and right. However, there are still eight separate I/O banks, as shown in Table 91 and Figure 46. Banks 0 and 1 share the VCCO_TOP input, Banks 2 and 3 share the VCCO_RIGHT input, Banks 4 and 5 share the VCCO_BOTTOM input, and Banks 6 and 7 share the VCCO_LEFT input.

All the package pins appear in Table 91 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

Pinout Table

Table 91: **TQ144 Package Pinout**

Bank	XC3S50, XC3S200, XC3S400 Pin Name	TQ144 Pin Number	Type
0	IO_L01N_0/VRP_0	P141	DCI
0	IO_L01P_0/VRN_0	P140	DCI
0	IO_L27N_0	P137	I/O
0	IO_L27P_0	P135	I/O
0	IO_L30N_0	P132	I/O
0	IO_L30P_0	P131	I/O
0	IO_L31N_0	P130	I/O
0	IO_L31P_0/VREF_0	P129	VREF
0	IO_L32N_0/GCLK7	P128	GCLK
0	IO_L32P_0/GCLK6	P127	GCLK
1	IO	P116	I/O
1	IO_L01N_1/VRP_1	P113	DCI
1	IO_L01P_1/VRN_1	P112	DCI
1	IO_L28N_1	P119	I/O
1	IO_L28P_1	P118	I/O
1	IO_L31N_1/VREF_1	P123	VREF
1	IO_L31P_1	P122	I/O
1	IO_L32N_1/GCLK5	P125	GCLK
1	IO_L32P_1/GCLK4	P124	GCLK
2	IO_L01N_2/VRP_2	P108	DCI
2	IO_L01P_2/VRN_2	P107	DCI
2	IO_L20N_2	P105	I/O
2	IO_L20P_2	P104	I/O
2	IO_L21N_2	P103	I/O
2	IO_L21P_2	P102	I/O
2	IO_L22N_2	P100	I/O
2	IO_L22P_2	P99	I/O

Table 91: **TQ144 Package Pinout *(Cont'd)***

Bank	XC3S50, XC3S200, XC3S400 Pin Name	TQ144 Pin Number	Type
6,7	VCCO_LEFT	P34	VCCO
6,7	VCCO_LEFT	P3	VCCO
N/A	GND	P136	GND
N/A	GND	P139	GND
N/A	GND	P114	GND
N/A	GND	P117	GND
N/A	GND	P94	GND
N/A	GND	P101	GND
N/A	GND	P81	GND
N/A	GND	P88	GND
N/A	GND	P64	GND
N/A	GND	P67	GND
N/A	GND	P42	GND
N/A	GND	P45	GND
N/A	GND	P22	GND
N/A	GND	P29	GND
N/A	GND	P9	GND
N/A	GND	P16	GND
N/A	VCCAUX	P134	VCCAUX
N/A	VCCAUX	P120	VCCAUX
N/A	VCCAUX	P62	VCCAUX
N/A	VCCAUX	P48	VCCAUX
N/A	VCCINT	P133	VCCINT
N/A	VCCINT	P121	VCCINT
N/A	VCCINT	P61	VCCINT
N/A	VCCINT	P49	VCCINT
VCCAUX	CCLK	P72	CONFIG
VCCAUX	DONE	P71	CONFIG
VCCAUX	HSWAP_EN	P142	CONFIG
VCCAUX	M0	P38	CONFIG
VCCAUX	M1	P37	CONFIG
VCCAUX	M2	P39	CONFIG
VCCAUX	PROG_B	P143	CONFIG
VCCAUX	TCK	P110	JTAG
VCCAUX	TDI	P144	JTAG
VCCAUX	TDO	P109	JTAG
VCCAUX	TMS	P111	JTAG

TQ144 Footprint

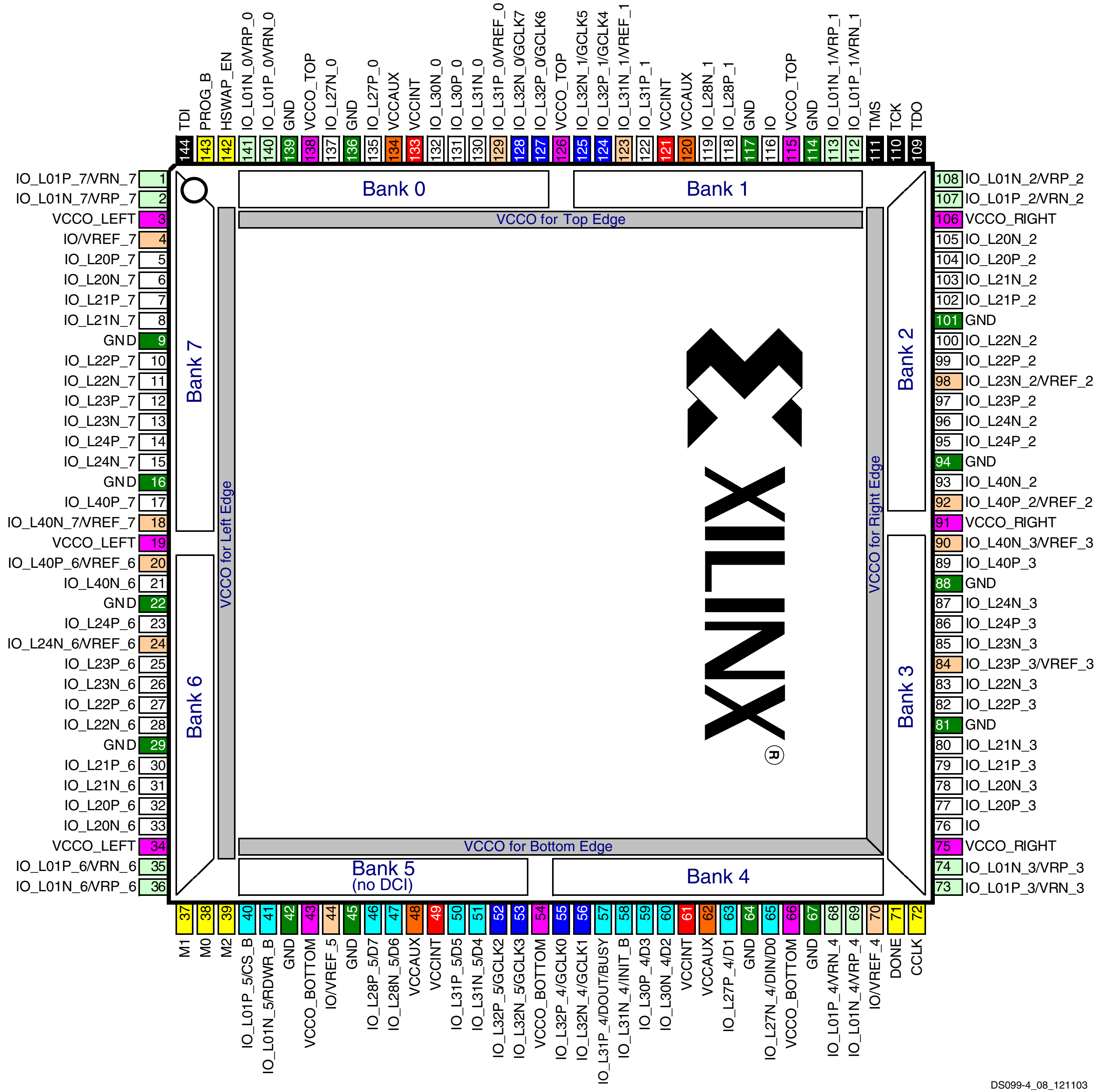

Figure 46: **TQ144 Package Footprint (Top View). Note pin 1 indicator in top-left corner and logo orientation.**

51	**I/O:** Unrestricted, general-purpose user I/O	12	**DUAL:** Configuration pin, then possible user I/O	12	**VREF:** User I/O or input voltage reference for bank
14	**DCI:** User I/O or reference resistor input for bank	8	**GCLK:** User I/O or global clock buffer input	12	**VCCO:** Output voltage supply for bank
7	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	4	**VCCINT:** Internal core voltage supply (+1.2V)
0	**N.C.:** No unconnected pins in this package	16	**GND:** Ground	4	**VCCAUX:** Auxiliary voltage supply (+2.5V)

Table 93: **PQ208 Package Pinout *(Cont'd)***

Bank	XC3S50 Pin Name	XC3S200, XC3S400 Pin Names	PQ208 Pin Number	Type
3	IO_L20P_3	IO_L20P_3	P114	I/O
3	IO_L21N_3	IO_L21N_3	P117	I/O
3	IO_L21P_3	IO_L21P_3	P116	I/O
3	IO_L22N_3	IO_L22N_3	P120	I/O
3	IO_L22P_3	IO_L22P_3	P119	I/O
3	IO_L23N_3	IO_L23N_3	P123	I/O
3	IO_L23P_3/VREF_3	IO_L23P_3/VREF_3	P122	VREF
3	IO_L24N_3	IO_L24N_3	P125	I/O
3	IO_L24P_3	IO_L24P_3	P124	I/O
3	N.C. (◆)	IO_L39N_3	P128	I/O
3	N.C. (◆)	IO_L39P_3	P126	I/O
3	IO_L40N_3/VREF_3	IO_L40N_3/VREF_3	P131	VREF
3	IO_L40P_3	IO_L40P_3	P130	I/O
3	VCCO_3	VCCO_3	P110	VCCO
3	VCCO_3	VCCO_3	P127	VCCO
4	IO	IO	P93	I/O
4	N.C. (◆)	IO	P97	I/O
4	IO/VREF_4	IO/VREF_4	P85	VREF
4	N.C. (◆)	IO/VREF_4	P96	VREF
4	IO/VREF_4	IO/VREF_4	P102	VREF
4	IO_L01N_4/VRP_4	IO_L01N_4/VRP_4	P101	DCI
4	IO_L01P_4/VRN_4	IO_L01P_4/VRN_4	P100	DCI
4	IO_L25N_4	IO_L25N_4	P95	I/O
4	IO_L25P_4	IO_L25P_4	P94	I/O
4	IO_L27N_4/DIN/D0	IO_L27N_4/DIN/D0	P92	DUAL
4	IO_L27P_4/D1	IO_L27P_4/D1	P90	DUAL
4	IO_L30N_4/D2	IO_L30N_4/D2	P87	DUAL
4	IO_L30P_4/D3	IO_L30P_4/D3	P86	DUAL
4	IO_L31N_4/INIT_B	IO_L31N_4/INIT_B	P83	DUAL
4	IO_L31P_4/DOUT/BUSY	IO_L31P_4/DOUT/BUSY	P81	DUAL
4	IO_L32N_4/GCLK1	IO_L32N_4/GCLK1	P80	GCLK
4	IO_L32P_4/GCLK0	IO_L32P_4/GCLK0	P79	GCLK
4	VCCO_4	VCCO_4	P84	VCCO
4	VCCO_4	VCCO_4	P98	VCCO
5	IO	IO	P63	I/O
5	IO	IO	P71	I/O
5	IO/VREF_5	IO/VREF_5	P78	VREF
5	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	P58	DUAL
5	IO_L01P_5/CS_B	IO_L01P_5/CS_B	P57	DUAL
5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	P62	DCI

Table 96: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S200, XC3S400, XC3S1000 Pin Name	FT256 Pin Number	Type
6	IO_L16P_6	N3	I/O
6	IO_L17N_6	N2	I/O
6	IO_L17P_6/VREF_6	N1	VREF
6	IO_L19N_6	M4	I/O
6	IO_L19P_6	M3	I/O
6	IO_L20N_6	M2	I/O
6	IO_L20P_6	M1	I/O
6	IO_L21N_6	L5	I/O
6	IO_L21P_6	L4	I/O
6	IO_L22N_6	L3	I/O
6	IO_L22P_6	L2	I/O
6	IO_L23N_6	K5	I/O
6	IO_L23P_6	K4	I/O
6	IO_L24N_6/VREF_6	K3	VREF
6	IO_L24P_6	K2	I/O
6	IO_L39N_6	J4	I/O
6	IO_L39P_6	J3	I/O
6	IO_L40N_6	J2	I/O
6	IO_L40P_6/VREF_6	J1	VREF
6	VCCO_6	J5	VCCO
6	VCCO_6	J6	VCCO
6	VCCO_6	K6	VCCO
7	IO	G2	I/O
7	IO_L01N_7/VRP_7	C1	DCI
7	IO_L01P_7/VRN_7	B1	DCI
7	IO_L16N_7	C2	I/O
7	IO_L16P_7/VREF_7	C3	VREF
7	IO_L17N_7	D1	I/O
7	IO_L17P_7	D2	I/O
7	IO_L19N_7/VREF_7	E3	VREF
7	IO_L19P_7	D3	I/O
7	IO_L20N_7	E1	I/O
7	IO_L20P_7	E2	I/O
7	IO_L21N_7	F4	I/O
7	IO_L21P_7	E4	I/O
7	IO_L22N_7	F2	I/O
7	IO_L22P_7	F3	I/O
7	IO_L23N_7	G5	I/O
7	IO_L23P_7	F5	I/O
7	IO_L24N_7	G3	I/O

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
N/A	VCCINT	N6	VCCINT
N/A	VCCINT	N7	VCCINT
VCCAUX	CCLK	T15	CONFIG
VCCAUX	DONE	R15	CONFIG
VCCAUX	HSWAP_EN	E6	CONFIG
VCCAUX	M0	P5	CONFIG
VCCAUX	M1	U3	CONFIG
VCCAUX	M2	R4	CONFIG
VCCAUX	PROG_B	E5	CONFIG
VCCAUX	TCK	E14	JTAG
VCCAUX	TDI	D4	JTAG
VCCAUX	TDO	D15	JTAG
VCCAUX	TMS	B16	JTAG

User I/Os by Bank

Table 99 indicates how the available user-I/O pins are distributed between the eight I/O banks on the FG320 package.

Table 99: **User I/Os Per Bank in FG320 Package**

Package Edge	I/O Bank	Maximum I/O	Maximum LVDS Pairs	All Possible I/O Pins by Type				
				I/O	DUAL	DCI	VREF	GCLK
Top	0	26	11	19	0	2	3	2
	1	26	11	19	0	2	3	2
Right	2	29	14	23	0	2	4	0
	3	29	14	23	0	2	4	0
Bottom	4	27	11	13	6	2	4	2
	5	26	11	13	6	2	3	2
Left	6	29	14	23	0	2	4	0
	7	29	14	23	0	2	4	0

FG456: 456-lead Fine-pitch Ball Grid Array

The 456-lead fine-pitch ball grid array package, FG456, supports four different Spartan-3 devices, including the XC3S400, the XC3S1000, the XC3S1500, and the XC3S2000. The footprints for the XC3S1000, the XC3S1500, and the XC3S2000 are identical, as shown in Table 100 and Figure 51. The XC3S400, however, has fewer I/O pins which consequently results in 69 unconnected pins on the FG456 package, labeled as "N.C." In Table 100 and Figure 51, these unconnected pins are indicated with a black diamond symbol (◆).

All the package pins appear in Table 100 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

If there is a difference between the XC3S400 pinout and the pinout for the XC3S1000, the XC3S1500, or the XC3S2000, then that difference is highlighted in Table 100. If the table entry is shaded grey, then there is an unconnected pin on the XC3S400 that maps to a user-I/O pin on the XC3S1000, XC3S1500, and XC3S2000. If the table entry is shaded tan, then the unconnected pin on the XC3S400 maps to a VREF-type pin on the XC3S1000, the XC3S1500, or the XC3S2000. If the other VREF pins in the bank all connect to a voltage reference to support a special I/O standard, then also connect the N.C. pin on the XC3S400 to the same VREF voltage. This provides maximum flexibility as you could potentially migrate a design from the XC3S400 device to an XC3S1000, an XC3S1500, or an XC3S2000 FPGA without changing the printed circuit board.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

Pinout Table

Table 100: **FG456 Package Pinout**

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
0	IO	IO	A10	I/O
0	IO	IO	D9	I/O
0	IO	IO	D10	I/O
0	IO	IO	F6	I/O
0	IO/VREF_0	IO/VREF_0	A3	VREF
0	IO/VREF_0	IO/VREF_0	C7	VREF
0	N.C. (◆)	IO/VREF_0	E5	VREF
0	IO/VREF_0	IO/VREF_0	F7	VREF
0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	B4	DCI
0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	A4	DCI
0	IO_L06N_0	IO_L06N_0	D5	I/O
0	IO_L06P_0	IO_L06P_0	C5	I/O
0	IO_L09N_0	IO_L09N_0	B5	I/O
0	IO_L09P_0	IO_L09P_0	A5	I/O
0	IO_L10N_0	IO_L10N_0	E6	I/O
0	IO_L10P_0	IO_L10P_0	D6	I/O
0	IO_L15N_0	IO_L15N_0	C6	I/O
0	IO_L15P_0	IO_L15P_0	B6	I/O
0	IO_L16N_0	IO_L16N_0	E7	I/O
0	IO_L16P_0	IO_L16P_0	D7	I/O
0	N.C. (◆)	IO_L19N_0	B7	I/O
0	N.C. (◆)	IO_L19P_0	A7	I/O

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
2	IO_L21P_2	IO_L21P_2	E22	I/O
2	IO_L22N_2	IO_L22N_2	G17	I/O
2	IO_L22P_2	IO_L22P_2	G18	I/O
2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	F19	VREF
2	IO_L23P_2	IO_L23P_2	G19	I/O
2	IO_L24N_2	IO_L24N_2	F20	I/O
2	IO_L24P_2	IO_L24P_2	F21	I/O
2	N.C. (◆)	IO_L26N_2	G20	I/O
2	N.C. (◆)	IO_L26P_2	H19	I/O
2	IO_L27N_2	IO_L27N_2	G21	I/O
2	IO_L27P_2	IO_L27P_2	G22	I/O
2	N.C. (◆)	IO_L28N_2	H18	I/O
2	N.C. (◆)	IO_L28P_2	J17	I/O
2	N.C. (◆)	IO_L29N_2	H21	I/O
2	N.C. (◆)	IO_L29P_2	H22	I/O
2	N.C. (◆)	IO_L31N_2	J18	I/O
2	N.C. (◆)	IO_L31P_2	J19	I/O
2	N.C. (◆)	IO_L32N_2	J21	I/O
2	N.C. (◆)	IO_L32P_2	J22	I/O
2	N.C. (◆)	IO_L33N_2	K17	I/O
2	N.C. (◆)	IO_L33P_2	K18	I/O
2	IO_L34N_2/VREF_2	IO_L34N_2/VREF_2	K19	VREF
2	IO_L34P_2	IO_L34P_2	K20	I/O
2	IO_L35N_2	IO_L35N_2	K21	I/O
2	IO_L35P_2	IO_L35P_2	K22	I/O
2	IO_L38N_2	IO_L38N_2	L17	I/O
2	IO_L38P_2	IO_L38P_2	L18	I/O
2	IO_L39N_2	IO_L39N_2	L19	I/O
2	IO_L39P_2	IO_L39P_2	L20	I/O
2	IO_L40N_2	IO_L40N_2	L21	I/O
2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	L22	VREF
2	VCCO_2	VCCO_2	H17	VCCO
2	VCCO_2	VCCO_2	H20	VCCO
2	VCCO_2	VCCO_2	J16	VCCO
2	VCCO_2	VCCO_2	K16	VCCO
2	VCCO_2	VCCO_2	L16	VCCO
3	IO	IO	Y21	I/O
3	IO_L01N_3/VRP_3	IO_L01N_3/VRP_3	Y20	DCI
3	IO_L01P_3/VRN_3	IO_L01P_3/VRN_3	Y19	DCI
3	IO_L16N_3	IO_L16N_3	W22	I/O

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
3	VCCO_3	VCCO_3	N16	VCCO
3	VCCO_3	VCCO_3	P16	VCCO
3	VCCO_3	VCCO_3	R17	VCCO
3	VCCO_3	VCCO_3	R20	VCCO
4	IO	IO	U16	I/O
4	IO	IO	U17	I/O
4	IO	IO	W13	I/O
4	IO	IO	W14	I/O
4	IO/VREF_4	IO/VREF_4	AB13	VREF
4	IO/VREF_4	IO/VREF_4	V18	VREF
4	IO/VREF_4	IO/VREF_4	Y16	VREF
4	IO_L01N_4/VRP_4	IO_L01N_4/VRP_4	AA20	DCI
4	IO_L01P_4/VRN_4	IO_L01P_4/VRN_4	AB20	DCI
4	N.C. (◆)	IO_L05N_4	AA19	I/O
4	N.C. (◆)	IO_L05P_4	AB19	I/O
4	IO_L06N_4/VREF_4	IO_L06N_4/VREF_4	W18	VREF
4	IO_L06P_4	IO_L06P_4	Y18	I/O
4	IO_L09N_4	IO_L09N_4	AA18	I/O
4	IO_L09P_4	IO_L09P_4	AB18	I/O
4	IO_L10N_4	IO_L10N_4	V17	I/O
4	IO_L10P_4	IO_L10P_4	W17	I/O
4	IO_L15N_4	IO_L15N_4	Y17	I/O
4	IO_L15P_4	IO_L15P_4	AA17	I/O
4	IO_L16N_4	IO_L16N_4	V16	I/O
4	IO_L16P_4	IO_L16P_4	W16	I/O
4	N.C. (◆)	IO_L19N_4	AA16	I/O
4	N.C. (◆)	IO_L19P_4	AB16	I/O
4	N.C. (◆)	IO_L22N_4/ VREF_4	V15	VREF
4	N.C. (◆)	IO_L22P_4	W15	I/O
4	IO_L24N_4	IO_L24N_4	AA15	I/O
4	IO_L24P_4	IO_L24P_4	AB15	I/O
4	IO_L25N_4	IO_L25N_4	U14	I/O
4	IO_L25P_4	IO_L25P_4	V14	I/O
4	IO_L27N_4/DIN/D0	IO_L27N_4/DIN/D0	AA14	DUAL
4	IO_L27P_4/D1	IO_L27P_4/D1	AB14	DUAL
4	IO_L28N_4	IO_L28N_4	U13	I/O
4	IO_L28P_4	IO_L28P_4	V13	I/O
4	IO_L29N_4	IO_L29N_4	Y13	I/O
4	IO_L29P_4	IO_L29P_4	AA13	I/O

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
5	IO_L01P_5/CS_B	IO_L01P_5/CS_B	IO_L01P_5/CS_B	IO_L01P_5/CS_B	IO_L01P_5/CS_B	AB5	DUAL
5	IO_L04N_5	IO_L04N_5	IO_L04N_5	IO_L04N_5	IO_L04N_5	AE4	I/O
5	IO_L04P_5	IO_L04P_5	IO_L04P_5	IO_L04P_5	IO_L04P_5	AD4	I/O
5	IO_L05N_5	IO_L05N_5	IO_L05N_5	IO_L05N_5	IO_L05N_5	AB6	I/O
5	IO_L05P_5	IO_L05P_5	IO_L05P_5	IO_L05P_5	IO_L05P_5	AA6	I/O
5	IO_L06N_5	IO_L06N_5	IO_L06N_5	IO_L06N_5	IO_L06N_5	AE5	I/O
5	IO_L06P_5	IO_L06P_5	IO_L06P_5	IO_L06P_5	IO_L06P_5	AD5	I/O
5	IO_L07N_5	IO_L07N_5	IO_L07N_5	IO_L07N_5	IO_L07N_5	AD6	I/O
5	IO_L07P_5	IO_L07P_5	IO_L07P_5	IO_L07P_5	IO_L07P_5	AC6	I/O
5	IO_L08N_5	IO_L08N_5	IO_L08N_5	IO_L08N_5	IO_L08N_5	AF6	I/O
5	IO_L08P_5	IO_L08P_5	IO_L08P_5	IO_L08P_5	IO_L08P_5	AE6	I/O
5	IO_L09N_5	IO_L09N_5	IO_L09N_5	IO_L09N_5	IO_L09N_5	AC7	I/O
5	IO_L09P_5	IO_L09P_5	IO_L09P_5	IO_L09P_5	IO_L09P_5	AB7	I/O
5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	AF7	DCI
5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	AE7	DCI
5	N.C. (◆)	IO_L11N_5/VREF_5	IO_L11N_5/VREF_5	IO_L11N_5/VREF_5	IO_L11N_5/VREF_5	AB8	VREF
5	N.C. (◆)	IO_L11P_5	IO_L11P_5	IO_L11P_5	IO_L11P_5	AA8	I/O
5	N.C. (◆)	IO_L12N_5	IO_L12N_5	IO_L12N_5	IO_L12N_5	AD8	I/O
5	N.C. (◆)	IO_L12P_5	IO_L12P_5	IO_L12P_5	IO_L12P_5	AC8	I/O
5	IO_L15N_5	IO_L15N_5	IO_L15N_5	IO_L15N_5	IO_L15N_5	AF8	I/O
5	IO_L15P_5	IO_L15P_5	IO_L15P_5	IO_L15P_5	IO_L15P_5	AE8	I/O
5	IO_L16N_5	IO_L16N_5	IO_L16N_5	IO_L16N_5	IO_L16N_5	AA9	I/O
5	IO_L16P_5	IO_L16P_5	IO_L16P_5	IO_L16P_5	IO_L16P_5	Y9	I/O
5	N.C. (◆)	IO_L18N_5	IO_L18N_5	IO_L18N_5	IO_L18N_5	AE9	I/O
5	N.C. (◆)	IO_L18P_5	IO_L18P_5	IO_L18P_5	IO_L18P_5	AD9	I/O
5	IO_L19N_5	IO_L19N_5	IO_L19N_5	IO_L19N_5	IO_L19N_5	AA10	I/O
5	IO_L19P_5/VREF_5	IO_L19P_5/VREF_5	IO_L19P_5/VREF_5	IO_L19P_5/VREF_5	IO_L19P_5/VREF_5	Y10	VREF
5	IO_L22N_5	IO_L22N_5	IO_L22N_5	IO_L22N_5	IO_L22N_5	AC10	I/O
5	IO_L22P_5	IO_L22P_5	IO_L22P_5	IO_L22P_5	IO_L22P_5	AB10	I/O
5	N.C. (◆)	IO_L23N_5	IO_L23N_5	IO_L23N_5	IO_L23N_5	AF10	I/O
5	N.C. (◆)	IO_L23P_5	IO_L23P_5	IO_L23P_5	IO_L23P_5	AE10	I/O
5	IO_L24N_5	IO_L24N_5	IO_L24N_5	IO_L24N_5	IO_L24N_5	Y11	I/O
5	IO_L24P_5	IO_L24P_5	IO_L24P_5	IO_L24P_5	IO_L24P_5	W11	I/O
5	IO_L25N_5	IO_L25N_5	IO_L25N_5	IO_L25N_5	IO_L25N_5	AB11	I/O
5	IO_L25P_5	IO_L25P_5	IO_L25P_5	IO_L25P_5	IO_L25P_5	AA11	I/O
5	N.C. (◆)	IO_L26N_5	IO_L26N_5	IO_L26N_5	IO_L26N_5	AF11	I/O
5	N.C. (◆)	IO_L26P_5	IO_L26P_5	IO_L26P_5	IO_L26P_5	AE11	I/O
5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	Y12	VREF
5	IO_L27P_5	IO_L27P_5	IO_L27P_5	IO_L27P_5	IO_L27P_5	W12	I/O
5	IO_L28N_5/D6	IO_L28N_5/D6	IO_L28N_5/D6	IO_L28N_5/D6	IO_L28N_5/D6	AB12	DUAL
5	IO_L28P_5/D7	IO_L28P_5/D7	IO_L28P_5/D7	IO_L28P_5/D7	IO_L28P_5/D7	AA12	DUAL
5	IO_L29N_5	IO_L29N_5	IO_L29N_5	IO_L29N_5	IO_L29N_5	AF12	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
3	IO_L21P_3	IO_L21P_3	Y23	I/O
3	IO_L22N_3	IO_L22N_3	Y26	I/O
3	IO_L22P_3	IO_L22P_3	Y25	I/O
3	IO_L23N_3	IO_L23N_3	Y28	I/O
3	IO_L23P_3/VREF_3	IO_L23P_3/VREF_3	Y27	VREF
3	IO_L24N_3	IO_L24N_3	Y30	I/O
3	IO_L24P_3	IO_L24P_3	Y29	I/O
3	IO_L26N_3	IO_L26N_3	W30	I/O
3	IO_L26P_3	IO_L26P_3	W29	I/O
3	IO_L27N_3	IO_L27N_3	V21	I/O
3	IO_L27P_3	IO_L27P_3	W21	I/O
3	IO_L28N_3	IO_L28N_3	V23	I/O
3	IO_L28P_3	IO_L28P_3	V22	I/O
3	IO_L29N_3	IO_L29N_3	V25	I/O
3	IO_L29P_3	IO_L29P_3	W26	I/O
3	IO_L31N_3	IO_L31N_3	V30	I/O
3	IO_L31P_3	IO_L31P_3	V29	I/O
3	IO_L32N_3	IO_L32N_3	U22	I/O
3	IO_L32P_3	IO_L32P_3	U21	I/O
3	IO_L33N_3	IO_L33N_3	U25	I/O
3	IO_L33P_3	IO_L33P_3	U24	I/O
3	IO_L34N_3	IO_L34N_3	U29	I/O
3	IO_L34P_3/VREF_3	IO_L34P_3/VREF_3	U28	VREF
3	IO_L35N_3	IO_L35N_3	T22	I/O
3	IO_L35P_3	IO_L35P_3	T21	I/O
3	IO_L37N_3	IO_L37N_3	T24	I/O
3	IO_L37P_3	IO_L37P_3	T23	I/O
3	IO_L38N_3	IO_L38N_3	T26	I/O
3	IO_L38P_3	IO_L38P_3	T25	I/O
3	IO_L39N_3	IO_L39N_3	T28	I/O
3	IO_L39P_3	IO_L39P_3	T27	I/O
3	IO_L40N_3/VREF_3	IO_L40N_3/VREF_3	T30	VREF
3	IO_L40P_3	IO_L40P_3	T29	I/O
3	N.C. (◆)	IO_L46N_3	W23	I/O
3	N.C. (◆)	IO_L46P_3	W22	I/O
3	N.C. (◆)	IO_L47N_3	W25	I/O
3	N.C. (◆)	IO_L47P_3	W24	I/O
3	N.C. (◆)	IO_L48N_3	W28	I/O
3	N.C. (◆)	IO_L48P_3	W27	I/O
3	N.C. (◆)	IO_L50N_3	V27	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
N/A	GND	GND	K30	GND
N/A	GND	GND	P30	GND
N/A	GND	GND	U30	GND
N/A	GND	GND	AA30	GND
N/A	GND	GND	AE30	GND
N/A	GND	GND	AJ30	GND
N/A	GND	GND	AK30	GND
N/A	GND	GND	AK2	GND
N/A	VCCAUX	VCCAUX	F4	VCCAUX
N/A	VCCAUX	VCCAUX	K4	VCCAUX
N/A	VCCAUX	VCCAUX	P4	VCCAUX
N/A	VCCAUX	VCCAUX	U4	VCCAUX
N/A	VCCAUX	VCCAUX	AA4	VCCAUX
N/A	VCCAUX	VCCAUX	AE4	VCCAUX
N/A	VCCAUX	VCCAUX	D6	VCCAUX
N/A	VCCAUX	VCCAUX	AG6	VCCAUX
N/A	VCCAUX	VCCAUX	D10	VCCAUX
N/A	VCCAUX	VCCAUX	AG10	VCCAUX
N/A	VCCAUX	VCCAUX	D14	VCCAUX
N/A	VCCAUX	VCCAUX	AG14	VCCAUX
N/A	VCCAUX	VCCAUX	D17	VCCAUX
N/A	VCCAUX	VCCAUX	AG17	VCCAUX
N/A	VCCAUX	VCCAUX	D21	VCCAUX
N/A	VCCAUX	VCCAUX	AG21	VCCAUX
N/A	VCCAUX	VCCAUX	D25	VCCAUX
N/A	VCCAUX	VCCAUX	AG25	VCCAUX
N/A	VCCAUX	VCCAUX	F27	VCCAUX
N/A	VCCAUX	VCCAUX	K27	VCCAUX
N/A	VCCAUX	VCCAUX	P27	VCCAUX
N/A	VCCAUX	VCCAUX	U27	VCCAUX
N/A	VCCAUX	VCCAUX	AA27	VCCAUX
N/A	VCCAUX	VCCAUX	AE27	VCCAUX
N/A	VCCINT	VCCINT	L11	VCCINT
N/A	VCCINT	VCCINT	R11	VCCINT
N/A	VCCINT	VCCINT	T11	VCCINT
N/A	VCCINT	VCCINT	Y11	VCCINT
N/A	VCCINT	VCCINT	M12	VCCINT
N/A	VCCINT	VCCINT	N12	VCCINT
N/A	VCCINT	VCCINT	P12	VCCINT
N/A	VCCINT	VCCINT	U12	VCCINT

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
7	IO_L01P_7/VRN_7	IO_L01P_7/VRN_7	C2	DCI
7	IO_L02N_7	IO_L02N_7	D1	I/O
7	IO_L02P_7	IO_L02P_7	D2	I/O
7	IO_L03N_7/VREF_7	IO_L03N_7/VREF_7	E2	VREF
7	IO_L03P_7	IO_L03P_7	E3	I/O
7	IO_L04N_7	IO_L04N_7	F3	I/O
7	IO_L04P_7	IO_L04P_7	F4	I/O
7	IO_L05N_7	IO_L05N_7	F1	I/O
7	IO_L05P_7	IO_L05P_7	F2	I/O
7	IO_L06N_7	IO_L06N_7	G5	I/O
7	IO_L06P_7	IO_L06P_7	G6	I/O
7	IO_L07N_7	IO_L07N_7	H5	I/O
7	IO_L07P_7	IO_L07P_7	H6	I/O
7	IO_L08N_7	IO_L08N_7	H1	I/O
7	IO_L08P_7	IO_L08P_7	H2	I/O
7	IO_L09N_7	IO_L09N_7	J6	I/O
7	IO_L09P_7	IO_L09P_7	J7	I/O
7	IO_L10N_7	IO_L10N_7	J4	I/O
7	IO_L10P_7/VREF_7	IO_L10P_7/VREF_7	H4	VREF
7	IO_L11N_7	IO_L11N_7	J2	I/O
7	IO_L11P_7	IO_L11P_7	J3	I/O
7	IO_L12N_7	IO_L12N_7	K9	I/O
7	IO_L12P_7	IO_L12P_7	J8	I/O
7	IO_L13N_7	IO_L13N_7	K7	I/O
7	IO_L13P_7	IO_L13P_7	K8	I/O
7	IO_L14N_7	IO_L14N_7	K5	I/O
7	IO_L14P_7	IO_L14P_7	K6	I/O
7	IO_L15N_7	IO_L15N_7	K3	I/O
7	IO_L15P_7	IO_L15P_7	K4	I/O
7	IO_L16N_7	IO_L16N_7	K1	I/O
7	IO_L16P_7/VREF_7	IO_L16P_7/VREF_7	K2	VREF
7	IO_L17N_7	IO_L17N_7	L9	I/O
7	IO_L17P_7	IO_L17P_7	L10	I/O
7	IO_L19N_7/VREF_7	IO_L19N_7/VREF_7	L1	VREF
7	IO_L19P_7	IO_L19P_7	L2	I/O
7	IO_L20N_7	IO_L20N_7	M10	I/O
7	IO_L20P_7	IO_L20P_7	M11	I/O
7	IO_L21N_7	IO_L21N_7	M7	I/O
7	IO_L21P_7	IO_L21P_7	M8	I/O
7	IO_L22N_7	IO_L22N_7	M5	I/O