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Understanding Embedded - FPGAs (Field Programmable Gate Array)

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	192
Number of Logic Elements/Cells	1728
Total RAM Bits	73728
Number of I/O	124
Number of Gates	50000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s50-4pqg208c

Supply Voltages for the IOBs

Three different supplies power the IOBs:

- The V_{CCO} supplies, one for each of the FPGA's I/O banks, power the output drivers, except when using the GTL and GTLP signal standards. The voltage on the V_{CCO} pins determines the voltage swing of the output signal.
- V_{CCINT} is the main power supply for the FPGA's internal logic.
- The V_{CCAUX} is an auxiliary source of power, primarily to optimize the performance of various FPGA functions such as I/O switching.

The I/Os During Power-On, Configuration, and User Mode

With no power applied to the FPGA, all I/Os are in a high-impedance state. The V_{CCINT} (1.2V), V_{CCAUX} (2.5V), and V_{CCO} supplies may be applied in any order. Before power-on can finish, V_{CCINT}, V_{CCO} Bank 4, and V_{CCAUX} must have reached their respective minimum recommended operating levels (see Table 29, page 59). At this time, all I/O drivers also will be in a high-impedance state. V_{CCO} Bank 4, V_{CCINT}, and V_{CCAUX} serve as inputs to the internal Power-On Reset circuit (POR).

A Low level applied to the HSWAP_EN input enables pull-up resistors on User I/Os from power-on throughout configuration. A High level on HSWAP_EN disables the pull-up resistors, allowing the I/Os to float. If the HSWAP_EN pin is floating, then an internal pull-up resistor pulls HSWAP_EN High. As soon as power is applied, the FPGA begins initializing its configuration memory. At the same time, the FPGA internally asserts the Global Set-Reset (GSR), which asynchronously resets all IOB storage elements to a Low state.

Upon the completion of initialization, INIT_B goes High, sampling the M0, M1, and M2 inputs to determine the configuration mode. At this point, the configuration data is loaded into the FPGA. The I/O drivers remain in a high-impedance state (with or without pull-up resistors, as determined by the HSWAP_EN input) throughout configuration.

The Global Three State (GTS) net is released during Start-Up, marking the end of configuration and the beginning of design operation in the User mode. At this point, those I/Os to which signals have been assigned go active while all unused I/Os remain in a high-impedance state. The release of the GSR net, also part of Start-up, leaves the IOB registers in a Low state by default, unless the loaded design reverses the polarity of their respective RS inputs.

In User mode, all internal pull-up resistors on the I/Os are disabled and HSWAP_EN becomes a "don't care" input. If it is desirable to have pull-up or pull-down resistors on I/Os carrying signals, the appropriate symbol—e.g., PULLUP, PULLDOWN—must be placed at the appropriate pads in the design. The Bitstream Generator (Bitgen) option UnusedPin available in the Xilinx development software determines whether unused I/Os collectively have pull-up resistors, pull-down resistors, or no resistors in User mode.

CLB Overview

For more details on the CLBs, refer to the chapter entitled "Using Configurable Logic Blocks" in UG331.

The Configurable Logic Blocks (CLBs) constitute the main logic resource for implementing synchronous as well as combinatorial circuits. Each CLB comprises four interconnected slices, as shown in Figure 11. These slices are grouped in pairs. Each pair is organized as a column with an independent carry chain.

The nomenclature that the FPGA Editor—part of the Xilinx development software—uses to designate slices is as follows: The letter 'X' followed by a number identifies columns of slices. The 'X' number counts up in sequence from the left side of the die to the right. The letter 'Y' followed by a number identifies the position of each slice in a pair as well as indicating the CLB row. The 'Y' number counts slices starting from the bottom of the die according to the sequence: 0, 1, 0, 1 (the first CLB row); 2, 3, 2, 3 (the second CLB row); etc. Figure 11 shows the CLB located in the lower left-hand corner of the die. Slices X0Y0 and X0Y1 make up the column-pair on the left where as slices X1Y0 and X1Y1 make up the column-pair on the right. For each CLB, the term "left-hand" (or SLICEM) indicates the pair of slices labeled with an even 'X' number, such as X0, and the term "right-hand" (or SLICEL) designates the pair of slices with an odd 'X' number, e.g., X1.

Arrangement of RAM Blocks on Die

The XC3S50 has one column of block RAM. The Spartan-3 devices ranging from the XC3S200 to XC3S2000 have two columns of block RAM. The XC3S4000 and XC3S5000 have four columns. The position of the columns on the die is shown in Figure 1, page 3. For a given device, the total available RAM blocks are distributed equally among the columns. Table 12 shows the number of RAM blocks, the data storage capacity, and the number of columns for each device.

Table 12: **Number of RAM Blocks by Device**

Device	Total Number of RAM Blocks	Total Addressable Locations (Bits)	Number of Columns
XC3S50	4	73,728	1
XC3S200	12	221,184	2
XC3S400	16	294,912	2
XC3S1000	24	442,368	2
XC3S1500	32	589,824	2
XC3S2000	40	737,280	2
XC3S4000	96	1,769,472	4
XC3S5000	104	1,916,928	4

Block RAM and multipliers have interconnects between them that permit simultaneous operation; however, since the multiplier shares inputs with the upper data bits of block RAM, the maximum data path width of the block RAM is 18 bits in this case.

The Internal Structure of the Block RAM

The block RAM has a dual port structure. The two identical data ports called A and B permit independent access to the common RAM block, which has a maximum capacity of 18,432 bits—or 16,384 bits when no parity lines are used. Each port has its own dedicated set of data, control and clock lines for synchronous read and write operations. There are four basic data paths, as shown in Figure 13: (1) write to and read from Port A, (2) write to and read from Port B, (3) data transfer from Port A to Port B, and (4) data transfer from Port B to Port A.

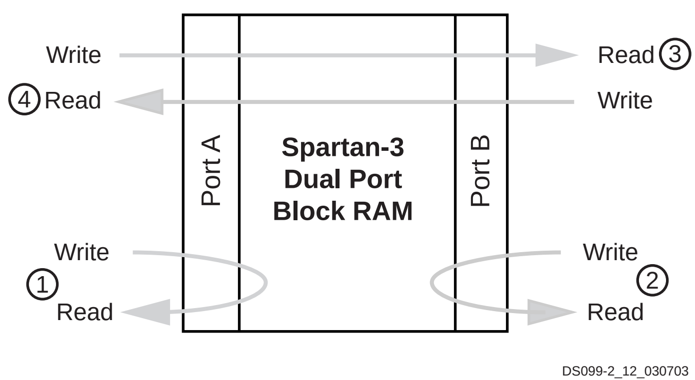

Figure 13: **Block RAM Data Paths**

Block RAM Port Signal Definitions

Representations of the dual-port primitive RAMB16_S[w_A]_S[w_B] and the single-port primitive RAMB16_S[w] with their associated signals are shown in Figure 14. These signals are defined in Table 13.

Table 13: **Block RAM Port Signals *(Cont'd)***

Signal Description	Port A Signal Name	Port B Signal Name	Direction	Function
Data Output Bus	DOA	DOB	Output	Basic data access occurs whenever WE is inactive. The DO outputs mirror the data stored in the addressed memory location. Data access with WE asserted is also possible if one of the following two attributes is chosen: WRITE_FIRST and READ_FIRST. WRITE_FIRST simultaneously presents the new input data on the DO output port and writes the data to the address RAM location. READ_FIRST presents the previously stored RAM data on the DO output port while writing new data to RAM. A third attribute, NO_CHANGE, latches the DO outputs upon the assertion of WE. It is possible to configure a port's total data path width (w) to be 1, 2, 4, 9, 18, or 36 bits. This selection applies to both the DI and DO paths. See the DI signal description.
Parity Data Output(s)	DOPA	DOPB	Output	Parity inputs represent additional bits included in the data input path to support error detection. The number of parity bits "p" included in the DI (same as for the DO bus) depends on a port's total data path width (w). See Table 14.
Write Enable	WEA	WEB	Input	When asserted together with EN, this input enables the writing of data to the RAM. In this case, the data access attributes WRITE_FIRST, READ_FIRST or NO_CHANGE determines if and how data is updated on the DO outputs. See the DO signal description. When WE is inactive with EN asserted, read operations are still possible. In this case, a transparent latch passes data from the addressed memory location to the DO outputs.
Clock Enable	ENA	ENB	Input	When asserted, this input enables the CLK signal to synchronize Block RAM functions as follows: the writing of data to the DI inputs (when WE is also asserted), the updating of data at the DO outputs as well as the setting/resetting of the DO output latches. When de-asserted, the above functions are disabled.
Set/Reset	SSRA	SSRB	Input	When asserted, this pin forces the DO output latch to the value that the SRVAL attribute is set to. A Set/Reset operation on one port has no effect on the other ports functioning, nor does it disturb the memory's data contents. It is synchronized to the CLK signal.
Clock	CLKA	CLKB	Input	This input accepts the clock signal to which read and write operations are synchronized. All associated port inputs are required to meet setup times with respect to the clock signal's active edge. The data output bus responds after a clock-to-out delay referenced to the clock signal's active edge.

Port Aspect Ratios

On a given port, it is possible to select a number of different possible widths ($w - p$) for the DI/DO buses as shown in Table 14. These two buses always have the same width. This data bus width selection is independent for each port. If the data bus width of Port A differs from that of Port B, the Block RAM automatically performs a bus-matching function. When data are written to a port with a narrow bus, then read from a port with a wide bus, the latter port will effectively combine "narrow" words to form "wide" words. Similarly, when data are written into a port with a wide bus, then read from a port with a narrow bus, the latter port will divide "wide" words to form "narrow" words. When the data bus width is eight bits or greater, extra parity bits become available. The width of the total data path (w) is the sum of the DI/DO bus width and any parity bits (p).

The width selection made for the DI/DO bus determines the number of address lines according to the relationship expressed below:

$$r = 14 - [\log(w-p)/\log(2)] \quad \textit{Equation 1}$$

In turn, the number of address lines delimits the total number (n) of addressable locations or depth according to the following equation:

$$n = 2^r \quad \textit{Equation 2}$$

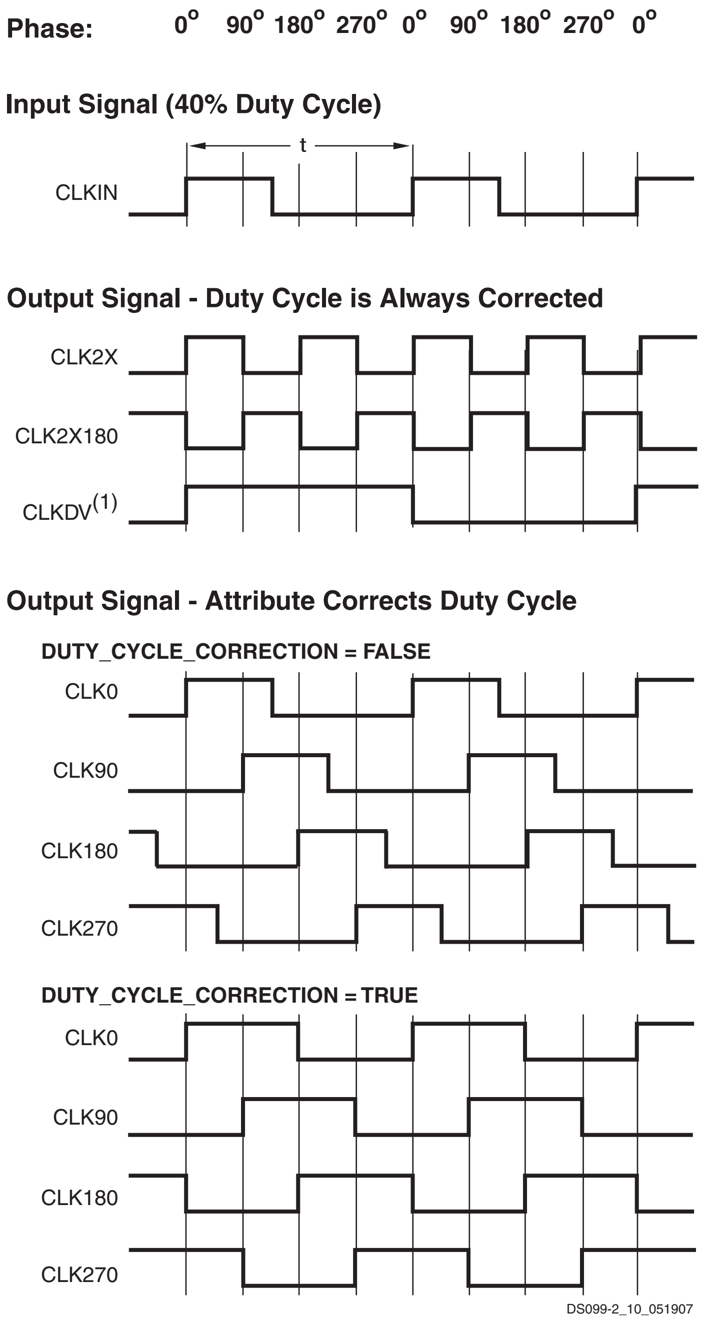

Figure 22: **Characteristics of the DLL Clock Outputs**

Digital Frequency Synthesizer (DFS)

The DFS component generates clock signals the frequency of which is a product of the clock frequency at the CLKIN input and a ratio of two user-determined integers. Because of the wide range of possible output frequencies such a ratio permits, the DFS feature provides still further flexibility than the DLL's basic synthesis options as described in the preceding section. The DFS component's two dedicated outputs, CLKFX and CLKFX180, are defined in Table 19.

The signal at the CLKFX180 output is essentially an inversion of the CLKFX signal. These two outputs always exhibit a 50% duty cycle. This is true even when the CLKIN signal does not. These DFS clock outputs are driven at the same time as the DLL's seven clock outputs.

The numerator of the ratio is the integer value assigned to the attribute CLKFX_MULTIPLY and the denominator is the integer value assigned to the attribute CLKFX_DIVIDE. These attributes are described in Table 18.

DFS Clock Output Connections

There are two basic cases that determine how to connect the DFS clock outputs: on-chip and off-chip, which are illustrated in sections [a] and [c], respectively, of Figure 21. This is similar to what has already been described for the DLL component. See DLL Clock Output and Feedback Connections, page 34.

In the on-chip case, it is possible to connect either of the DFS's two output clock signals through general routing resources to the FPGA's internal registers. Either a Global Clock Buffer (BUFG) or a BUFGMUX affords access to the global clock network. The optional feedback loop is formed in this way, routing CLK0 to a global clock net, which in turn drives the CLKFB input.

In the off-chip case, the DFS's two output clock signals, plus CLK0 for an optional feedback loop, can exit the FPGA using output buffers (OBUF) to drive a clock network plus registers on the board. The feedback loop is formed by feeding the CLK0 signal back into the FPGA using an IBUFG, which directly accesses the global clock network, or an IBUF. Then, the global clock net is connected directly to the CLKFB input.

Phase Shifter (PS)

The DCM provides two approaches to controlling the phase of a DCM clock output signal relative to the CLKIN signal: First, there are nine clock outputs that employ the DLL to achieve a desired phase relationship: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, CLKDV CLKFX, and CLKFX180. These outputs afford "coarse" phase control.

The second approach uses the PS component described in this section to provide a still finer degree of control. The PS component is only available when the DLL is operating in its low-frequency mode. The PS component phase shifts the DCM output clocks by introducing a "fine phase shift" (T_{PS}) between the CLKFB and CLKIN signals inside the DLL component. The user can control this fine phase shift down to a resolution of 1/256 of a CLKIN cycle or one tap delay (DCM_TAP), whichever is greater. When in use, the PS component shifts the phase of all nine DCM clock output signals together. If the PS component is used together with a DCM clock output such as the CLK90, CLK180, CLK270, CLK2X180 and CLKFX180, then the fine phase shift of the former gets added to the coarse phase shift of the latter.

PS Component Enabling and Mode Selection

The CLKOUT_PHASE_SHIFT attribute enables the PS component for use in addition to selecting between two operating modes. As described in Table 20, this attribute has three possible values: NONE, FIXED and VARIABLE. When CLKOUT_PHASE_SHIFT is set to NONE, the PS component is disabled and its inputs, PSEN, PSCLK, and PSINCDEC, must be tied to GND. The set of waveforms in section [a] of Figure 22 shows the disabled case, where the DLL maintains a zero-phase alignment of signals CLKFB and CLKIN upon which the PS component has no effect. The PS component is enabled by setting the attribute to either the FIXED or VARIABLE values, which select the Fixed Phase mode and the Variable Phase mode, respectively. These two modes are described in the sections that follow

Determining the Fine Phase Shift

The user controls the phase shift of CLKFB relative to CLKIN by setting and/or adjusting the value of the PHASE_SHIFT attribute. This value must be an integer ranging from –255 to +255. The PS component uses this value to calculate the desired fine phase shift (T_{PS}) as a fraction of the CLKIN period (T_{CLKIN}). Given values for PHASE-SHIFT and T_{CLKIN}, it is possible to calculate T_{PS} as follows:

$$T_{PS} = T_{CLKIN}(\text{PHASE\_SHIFT}/256) \qquad \textit{Equation 4}$$

Both the Fixed Phase and Variable Phase operating modes employ this calculation. If the PHASE_SHIFT value is zero, then CLKFB and CLKIN will be in phase, the same as when the PS component is disabled. When the PHASE_SHIFT value is positive, the CLKFB signal will be shifted later in time with respect to CLKIN. If the attribute value is negative, the CLKFB signal will be shifted earlier in time with respect to CLKIN.

The Fixed Phase Mode

This mode fixes the desired fine phase shift to a fraction of the T_{CLKIN}, as determined by Equation 4 and its user-selected PHASE_SHIFT value P. The set of waveforms insection [b] of Figure 22 illustrates the relationship between CLKFB and CLKIN in the Fixed Phase mode. In the Fixed Phase mode, the PSEN, PSCLK and PSINCDEC inputs are not used and must be tied to GND. Fixed phase shift requires ISE software version 10.1.03 or later.

Table 22: **Status Logic Signals**

Signal	Direction	Description
RST	Input	A High resets the entire DCM to its initial power-on state. Initializes the DLL taps for a delay of zero. Sets the LOCKED output Low. This input is asynchronous.
STATUS[7:0]	Output	The bit values on the STATUS bus provide information regarding the state of DLL and PS operation
LOCKED	Output	Indicates that the CLKIN and CLKFB signals are in phase by going High. The two signals are out-of-phase when Low.

Table 23: **DCM STATUS Bus**

Bit	Name	Description
0	Phase Shift Overflow	A value of 1 indicates a phase shift overflow when one of two conditions occurs: Incrementing (or decrementing) TPS beyond 255/256 of a CLKIN cycle. The DLL is producing its maximum possible phase shift (i.e., all delay taps are active).[1]
1	CLKIN Input Stopped Toggling	A value of 1 indicates that the CLKIN input signal is not toggling. A value of 0 indicates toggling. This bit functions only when the CLKFB input is connected.[2]
2	CLKFX/CLKFX180 Output Stopped Toggling	A value of 1 indicates that the CLKFX or CLKFX180 output signals are not toggling. A value of 0 indicates toggling. This bit functions only when using the Digital Frequency Synthesizer (DFS).
3:7	Reserved	–

Notes:

1. The DLL phase shift with all delay taps active is specified as the parameter FINE_SHIFT_RANGE.
2. If only the DFS clock outputs are used, but none of the DLL clock outputs, this bit will not go High when the CLKIN signal stops.

Table 24: **Status Attributes**

Attribute	Description	Values
STARTUP_WAIT	Delays transition from configuration to user mode until lock condition is achieved.	TRUE, FALSE

Stabilizing DCM Clocks Before User Mode

It is possible to delay the completion of device configuration until after the DLL has achieved a lock condition using the STARTUP_WAIT attribute described in Table 24. This option ensures that the FPGA does not enter user mode—i.e., begin functional operation—until all system clocks generated by the DCM are stable. In order to achieve the delay, it is necessary to set the attribute to TRUE as well as set the BitGen option LCK_cycle to one of the six cycles making up the Startup phase of configuration. The selected cycle defines the point at which configuration will halt until the LOCKED output goes High.

Global Clock Network

Spartan-3 devices have eight Global Clock inputs called GCLK0 - GCLK7. These inputs provide access to a low-capacitance, low-skew network that is well-suited to carrying high-frequency signals. The Spartan-3 FPGAs clock network is shown in Figure 23. GCLK0 through GCLK3 are located in the center of the bottom edge. GCLK4 through GCLK7 are located in the center of the top edge.

Eight Global Clock Multiplexers (also called BUFGMUX elements) are provided that accept signals from Global Clock inputs and route them to the internal clock network as well as DCMs. Four BUFGMUX elements are located in the center of the bottom edge, just above the GCLK0 - GCLK3 inputs. The remaining four BUFGMUX elements are located in the center of the top edge, just below the GCLK4 - GCLK7 inputs.

Pairs of BUFGMUX elements share global inputs, as shown in Figure 24. For example, the GCLK4 and GCLK5 inputs both potentially connect to BUFGMUX4 and BUFGMUX5 located in the upper right center. A differential clock input uses a pair of GCLK inputs to connect to a single BUFGMUX element.

Table 45: **Timing for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade -5 Max(3)	Speed Grade -4 Max(3)	Units
Clock-to-Output Times						
T_{IOCKP}	When reading from the Output Flip-Flop (OFF), the time from the active transition at the OTCLK input to data appearing at the Output pin	LVCMOS25(2), 12 mA output drive, Fast slew rate	XC3S200 XC3S400	1.28	1.47	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	1.95	2.24	ns
Propagation Times						
T_{IOOP}	The time it takes for data to travel from the IOB's O input to the Output pin	LVCMOS25(2), 12 mA output drive, Fast slew rate	XC3S200 XC3S400	1.28	1.46	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	1.94	2.23	ns
T_{IOOLP}	The time it takes for data to travel from the O input through the OFF latch to the Output pin		XC3S200 XC3S400	1.28	1.47	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	1.95	2.24	ns
Set/Reset Times						
T_{IOSRP}	Time from asserting the OFF's SR input to setting/resetting data at the Output pin	LVCMOS25(2), 12 mA output drive, Fast slew rate	XC3S200 XC3S400	2.10	2.41	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	2.77	3.18	ns
T_{IOGSRQ}	Time from asserting the Global Set Reset (GSR) net to setting/resetting data at the Output pin		All	8.07	9.28	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32 and Table 35.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 47.
3. For minimums, use the values reported by the Xilinx timing analyzer.

Table 59: **Switching Characteristics for the DLL *(Cont'd)***

Symbol	Description	Frequency Mode / FCLKIN Range	Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Lock Time								
LOCK_DLL	When using the DLL alone: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase	18 MHz $\le F_{CLKIN} \le$ 30 MHz	All	–	2.88	–	2.88	ms
		30 MHz $< F_{CLKIN} \le$ 40 MHz		–	2.16	–	2.16	ms
		40 MHz $< F_{CLKIN} \le$ 50 MHz		–	1.20	–	1.20	ms
		50 MHz $< F_{CLKIN} \le$ 60 MHz		–	0.60	–	0.60	ms
		$F_{CLKIN} >$ 60 MHz		–	0.48	–	0.48	ms
Delay Lines								
DCM_TAP	Delay tap resolution	All	All	30.0	60.0	30.0	60.0	ps

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32 and Table 58.
2. DLL specifications apply when any of the DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV) are in use.
3. Only mask revision 'E' and later devices (see Mask and Fab Revisions, page 58) and all revisions of the XC3S50 and the XC3S1000 support DLL feedback using the CLK2X output. For all other Spartan-3 devices, use feedback from the CLK0 output (instead of the CLK2X output) and set the CLK_FEEDBACK attribute to 1X.
4. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
5. This specification only applies if the attribute DUTY_CYCLE_CORRECTION = TRUE.

Digital Frequency Synthesizer (DFS)

Table 60: **Recommended Operating Conditions for the DFS**

Symbol		Description	Frequency Mode	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Input Frequency Ranges(2)								
F_{CLKIN}	CLKIN_FREQ_FX	Frequency for the CLKIN input	All	1	280	1	280	MHz
Input Clock Jitter Tolerance(3)								
CLKIN_CYC_JITT_FX_LF		Cycle-to-cycle jitter at the CLKIN input	Low	–	±300	–	±300	ps
CLKIN_CYC_JITT_FX_HF			High	–	±150	–	±150	ps
CLKIN_PER_JITT_FX		Period jitter at the CLKIN input	All	–	±1	–	±1	ns

Notes:

1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) are used.
2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 58.
3. CLKIN input jitter beyond these limits may cause the DCM to lose lock.

Date	Version	Description
05/25/07	2.2	Improved absolute maximum voltage specifications in Table 28, providing additional overshoot allowance. Improved XC3S50 HBM ESD to 2000V in Table 28. Based on extensive 90 nm production data, improved (reduced) the maximum quiescent current limits for the I_{CCINTQ} and I_{CCOQ} specifications in Table 34. Widened the recommended voltage range for the PCI standard and clarified the hysteresis footnote in Table 35. Noted restriction on combining differential outputs in Table 38. Updated footnote 1 in Table 64.
11/30/07	2.3	Updated 3.3V VCCO max from 3.45V to 3.465V in Table 32 and elsewhere. Reduced t_{ICCK} minimum from 0.50µs to 0.25µs in Table 65. Updated links to technical documentation.
06/25/08	2.4	Clarified dual marking. Added Mask and Fab Revisions. Added references to XAPP459 in Table 28 and Table 32. Removed absolute minimum and added footnote referring to timing analyzer for minimum delay values. Added HSLVDCI to Table 48 and Table 50. Updated t_{DICK} in Table 51 to match largest possible value in speed file. Updated formatting and links.
12/04/09	2.5	Updated notes 2 and 3 in Table 28. Removed silicon process specific information and revised notes in Table 30. Updated note 3 in Table 32. Updated note 3 in Table 34. Updated note 5 in Table 35. Updated V_{OL} max and V_{OH} min for SSTL2_II in Table 36. Updated note 5 in Table 36. Updated JTAG Waveforms in Figure 39. Updated V_{ICM} max for LVPECL_25 in Table 37. Updated RT and VT for LVDS_25_DCI in Table 48. Updated Simultaneously Switching Output Guidelines. Noted that the CP132 package is being discontinued in Table 49. Removed minimum values for T_{MULTCK} clock-to-output times in Table 54. Updated footnote 3 in Table 58. Removed minimum values for T_{MULT} propagation times in Table 55. Removed silicon process specific information and revised notes in Table 61. Updated Phase Shifter (PS).
10/29/12	3.0	Added Notice of Disclaimer. Per XCN07022, updated the discontinued FG1156 and FGG1156 package discussion throughout document. Per XCN08011, updated the discontinued CP132 and CPG132 package discussion throughout document. Revised description of V_{IN} in Table 32 and added note 7. Added note 4 to Table 33. This product is not recommended for new designs.

Table 79: **Pin Behavior After Power-Up, During Configuration *(Cont'd)***

Pin Name	Configuration Mode Settings <M2:M1:M0>					Bitstream Configuration Option
	Serial Modes		SelectMap Parallel Modes		JTAG Mode <1:0:1>	
	Master <0:0:0>	Slave <1:1:1>	Master <0:1:1>	Slave <1:1:0>		
VCCO: I/O bank output voltage supply pins						
VCCO_4 (for DUAL pins)	Same voltage as external interface	Same voltage as external interface	Same voltage as external interface	Same voltage as external interface	VCCO_4	N/A
VCCO_5 (for DUAL pins)	VCCO_5	VCCO_5	Same voltage as external interface	Same voltage as external interface	VCCO_5	N/A
VCCO_#	VCCO_#	VCCO_#	VCCO_#	VCCO_#	VCCO_#	N/A
VCCAUX: Auxiliary voltage supply pins						
VCCAUX	+2.5V	+2.5V	+2.5V	+2.5V	+2.5V	N/A
VCCINT: Internal core voltage supply pins						
VCCINT	+1.2V	+1.2V	+1.2V	+1.2V	+1.2V	N/A
GND: Ground supply pins						
GND	GND	GND	GND	GND	GND	N/A

Notes:

1. #= I/O bank number, an integer from 0 to 7.
2. (I) = input, (O) = output, (OD) = open-drain output, (I/O) = bidirectional, (I/OD) = bidirectional with open-drain output. Open-drain output requires pull-up to create logic High level.
3. Shaded cell indicates that the pin is high-impedance during configuration. To enable a soft pull-up resistor during configuration, drive or tie HSWAP_EN Low.

Bitstream Options

Table 80 lists the various bitstream options that affect pins on a Spartan-3 FPGA. The table shows the names of the affected pins, describes the function of the bitstream option, the name of the bitstream generator option variable, and the legal values for each variable. The default option setting for each variable is indicated with bold, underlined text.

Table 80: **Bitstream Options Affecting Spartan-3 Device Pins**

Affected Pin Name(s)	Bitstream Generation Function	Option Variable Name	Values (Default)
All unused I/O pins of type I/O, DUAL, GCLK, DCI, VREF	For all I/O pins that are unused in the application after configuration, this option defines whether the I/Os are individually tied to VCCO via a pull-up resistor, tied ground via a pull-down resistor, or left floating. If left floating, the unused pins should be connected to a defined logic level, either from a source internal to the FPGA or external.	UnusedPin	• **Pulldown** • Pullup • Pullnone
IO_Lxxy_#/DIN, IO_Lxxy_#/DOUT, IO_Lxxy_#/INIT_B	Serial configuration mode: If set to Yes, then these pins retain their functionality after configuration completes, allowing for device (re-)configuration. Readback is not supported in with serial mode.	Persist	• **No** • Yes
IO_Lxxy_#/D0, IO_Lxxy_#/D1, IO_Lxxy_#/D2, IO_Lxxy_#/D3, IO_Lxxy_#/D4, IO_Lxxy_#/D5, IO_Lxxy_#/D6, IO_Lxxy_#/D7, IO_Lxxy_#/CS_B, IO_Lxxy_#/RDWR_B, IO_Lxxy_#/BUSY, IO_Lxxy_#/INIT_B	Parallel configuration mode (also called SelectMAP): If set to Yes, then these pins retain their SelectMAP functionality after configuration completes, allowing for device readback and for partial or complete (re-)configuration.	Persist	• **No** • Yes

Table 89: **CP132 Package Pinout *(Cont'd)***

Bank	XC3S50 Pin Name	CP132 Ball	Type
6	IO_L22N_6	K1	I/O
6	IO_L22P_6	J3	I/O
6	IO_L23N_6	J2	I/O
6	IO_L23P_6	J1	I/O
6	IO_L24N_6/VREF_6	H3	VREF
6	IO_L24P_6	H2	I/O
6	IO_L40N_6	H1	I/O
6	IO_L40P_6/VREF_6	G3	VREF
7	IO_L01N_7/VRP_7	B2	DCI
7	IO_L01P_7/VRN_7	B1	DCI
7	IO_L21N_7	C1	I/O
7	IO_L21P_7	D3	I/O
7	IO_L22N_7	D1	I/O
7	IO_L22P_7	D2	I/O
7	IO_L23N_7	E2	I/O
7	IO_L23P_7	E3	I/O
7	IO_L24N_7	F3	I/O
7	IO_L24P_7	E1	I/O
7	IO_L40N_7/VREF_7	G1	VREF
7	IO_L40P_7	F2	I/O
0,1	VCCO_TOP	B12	VCCO
0,1	VCCO_TOP	A4	VCCO
0,1	VCCO_TOP	B8	VCCO
2,3	VCCO_RIGHT	D13	VCCO
2,3	VCCO_RIGHT	H13	VCCO
2,3	VCCO_RIGHT	M12	VCCO
4,5	VCCO_BOTTOM	N7	VCCO
4,5	VCCO_BOTTOM	P11	VCCO
4,5	VCCO_BOTTOM	N3	VCCO
6,7	VCCO_LEFT	G2	VCCO
6,7	VCCO_LEFT	L2	VCCO
6,7	VCCO_LEFT	C3	VCCO
N/A	GND	B4	GND
N/A	GND	B9	GND
N/A	GND	C2	GND
N/A	GND	C12	GND
N/A	GND	D14	GND
N/A	GND	F1	GND
N/A	GND	J14	GND
N/A	GND	L1	GND

CP132 Footprint

VCCO_TOP for Top Edge Outputs — Bank 0 (columns 3–7), Bank 1 (columns 8–13)
VCCO_LEFT for Left Edge Outputs — Bank 7 (rows A–G), Bank 6 (rows H–M)
VCCO_RIGHT for Right Edge Outputs — Bank 2 (rows C–G), Bank 3 (rows H–N)
VCCO_BOTTOM for Bottom Edge Outputs — Bank 5 (columns 2–7), Bank 4 (columns 8–14)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	TDI	PROG_B	I/O L01N_0 VRP_0	VCCO_ TOP	VCCAUX	I/O L30P_0	I/O L32N_0 GCLK7	I/O L32N_1 GCLK5	I/O L32P_1 GCLK4	I/O L31P_1	I/O L28N_1	I/O L27P_1	I/O L01N_1 VRP_1	TMS
B	I/O L01P_7 VRN_7	I/O L01N_7 VRP_7	HSWAP_ EN	GND	I/O L27P_0	I/O L30N_0	I/O L31P_0 VREF_0	VCCO_ TOP	GND	VCCINT	I/O L28P_1	VCCO_ TOP	I/O L01P_1 VRN_1	TCK
C	I/O L21N_7	GND	VCCO_ LEFT	I/O L01P_0 VRN_0	I/O L27N_0	VCCINT	I/O L31N_0	I/O L32P_0 GCLK6	I/O L31N_1 VREF_1	VCCAUX	I/O L27N_1	GND	TDO	I/O L01P_2 VRN_2
D	I/O L22N_7	I/O L22P_7	I/O L21P_7									I/O L01N_2 VRP_2	VCCO_ RIGHT	GND
E	I/O L24P_7	I/O L23N_7	I/O L23P_7									I/O L20N_2	I/O L20P_2	I/O L21N_2
F	GND	I/O L40P_7	I/O L24N_7									I/O L21P_2	I/O L23N_2 VREF_2	I/O L23P_2
G	I/O L40N_7 VREF_7	VCCO_ LEFT	I/O L40P_6 VREF_6									I/O L24N_2	I/O L24P_2	I/O L40N_2
H	I/O L40N_6	I/O L24P_6	I/O L24N_6 VREF_6									I/O L40P_2 VREF_2	VCCO_ RIGHT	I/O L40N_3 VREF_3
J	I/O L23P_6	I/O L23N_6	I/O L22P_6									I/O L24N_3	I/O L40P_3	GND
K	I/O L22N_6	I/O L20P_6	I/O L20N_6									I/O L23P_3 VREF_3	I/O L23N_3	I/O L24P_3
L	GND	VCCO_ LEFT	I/O L01N_6 VRP_6									I/O L20N_3	I/O L22P_3	I/O L22N_3
M	I/O L01P_6 VRN_6	M1	GND	I/O L27N_5 VREF_5	VCCAUX	I/O L31N_5 D4	I/O L32P_4 GCLK0	I/O L31N_4 INIT_B	VCCINT	I/O L27N_4 DIN D0	I/O L01P_4 VRN_4	VCCO_ RIGHT	GND	I/O L20P_3
N	M0	I/O L01P_5 CS_B	VCCO_ BOTTOM	I/O L28P_5 D7	VCCINT	GND	VCCO_ BOTTOM	I/O L31P_4 DOUT BUSY	I/O L30N_4 D2	I/O L27P_4 D1	GND	I/O VREF_4	I/O L01N_3 VRP_3	I/O L01P_3 VRN_3
P	M2	I/O L01N_5 RDWR_B	I/O L27P_5	I/O L28N_5 D6	I/O L31P_5 D5	I/O L32P_5 GCLK2	I/O L32N_5 GCLK3	I/O L32N_4 GCLK1	I/O L30P_4 D3	VCCAUX	VCCO_ BOTTOM	I/O L01N_4 VRP_4	DONE	CCLK

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Figure 45: **CP132 Package Footprint (Top View). Note pin 1 indicator in top-left corner and logo orientation.**

44	**I/O:** Unrestricted, general-purpose user I/O	12	**DUAL:** Configuration pin, then possible user I/O	11	**VREF:** User I/O or input voltage reference for bank
14	**DCI:** User I/O or reference resistor input for bank	8	**GCLK:** User I/O, input, or global buffer input	12	**VCCO:** Output voltage supply for bank
7	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	4	**VCCINT:** Internal core voltage supply (+1.2V)
0	**N.C.:** No unconnected pins in this package	12	**GND:** Ground	4	**VCCAUX:** Auxiliary voltage supply (+2.5V)

FT256: 256-lead Fine-pitch Thin Ball Grid Array

The 256-lead fine-pitch thin ball grid array package, FT256, supports three different Spartan-3 devices, including the XC3S200, the XC3S400, and the XC3S1000. The footprints for all three devices are identical, as shown in Table 96 and Figure 49.

All the package pins appear in Table 96 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

Pinout Table

Table 96: **FT256 Package Pinout**

Bank	XC3S200, XC3S400, XC3S1000 Pin Name	FT256 Pin Number	Type
0	IO	A5	I/O
0	IO	A7	I/O
0	IO/VREF_0	A3	VREF
0	IO/VREF_0	D5	VREF
0	IO_L01N_0/VRP_0	B4	DCI
0	IO_L01P_0/VRN_0	A4	DCI
0	IO_L25N_0	C5	I/O
0	IO_L25P_0	B5	I/O
0	IO_L27N_0	E6	I/O
0	IO_L27P_0	D6	I/O
0	IO_L28N_0	C6	I/O
0	IO_L28P_0	B6	I/O
0	IO_L29N_0	E7	I/O
0	IO_L29P_0	D7	I/O
0	IO_L30N_0	C7	I/O
0	IO_L30P_0	B7	I/O
0	IO_L31N_0	D8	I/O
0	IO_L31P_0/VREF_0	C8	VREF
0	IO_L32N_0/GCLK7	B8	GCLK
0	IO_L32P_0/GCLK6	A8	GCLK
0	VCCO_0	E8	VCCO
0	VCCO_0	F7	VCCO
0	VCCO_0	F8	VCCO
1	IO	A9	I/O
1	IO	A12	I/O
1	IO	C10	I/O
1	IO/VREF_1	D12	VREF
1	IO_L01N_1/VRP_1	A14	DCI
1	IO_L01P_1/VRN_1	B14	DCI

Table 96: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S200, XC3S400, XC3S1000 Pin Name	FT256 Pin Number	Type
6	IO_L16P_6	N3	I/O
6	IO_L17N_6	N2	I/O
6	IO_L17P_6/VREF_6	N1	VREF
6	IO_L19N_6	M4	I/O
6	IO_L19P_6	M3	I/O
6	IO_L20N_6	M2	I/O
6	IO_L20P_6	M1	I/O
6	IO_L21N_6	L5	I/O
6	IO_L21P_6	L4	I/O
6	IO_L22N_6	L3	I/O
6	IO_L22P_6	L2	I/O
6	IO_L23N_6	K5	I/O
6	IO_L23P_6	K4	I/O
6	IO_L24N_6/VREF_6	K3	VREF
6	IO_L24P_6	K2	I/O
6	IO_L39N_6	J4	I/O
6	IO_L39P_6	J3	I/O
6	IO_L40N_6	J2	I/O
6	IO_L40P_6/VREF_6	J1	VREF
6	VCCO_6	J5	VCCO
6	VCCO_6	J6	VCCO
6	VCCO_6	K6	VCCO
7	IO	G2	I/O
7	IO_L01N_7/VRP_7	C1	DCI
7	IO_L01P_7/VRN_7	B1	DCI
7	IO_L16N_7	C2	I/O
7	IO_L16P_7/VREF_7	C3	VREF
7	IO_L17N_7	D1	I/O
7	IO_L17P_7	D2	I/O
7	IO_L19N_7/VREF_7	E3	VREF
7	IO_L19P_7	D3	I/O
7	IO_L20N_7	E1	I/O
7	IO_L20P_7	E2	I/O
7	IO_L21N_7	F4	I/O
7	IO_L21P_7	E4	I/O
7	IO_L22N_7	F2	I/O
7	IO_L22P_7	F3	I/O
7	IO_L23N_7	G5	I/O
7	IO_L23P_7	F5	I/O
7	IO_L24N_7	G3	I/O

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
6	N.C. (◆)	IO_L28N_6	R5	I/O
6	N.C. (◆)	IO_L28P_6	P6	I/O
6	N.C. (◆)	IO_L29N_6	R2	I/O
6	N.C. (◆)	IO_L29P_6	R1	I/O
6	N.C. (◆)	IO_L31N_6	P5	I/O
6	N.C. (◆)	IO_L31P_6	P4	I/O
6	N.C. (◆)	IO_L32N_6	P2	I/O
6	N.C. (◆)	IO_L32P_6	P1	I/O
6	N.C. (◆)	IO_L33N_6	N6	I/O
6	N.C. (◆)	IO_L33P_6	N5	I/O
6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	N4	VREF
6	IO_L34P_6	IO_L34P_6	N3	I/O
6	IO_L35N_6	IO_L35N_6	N2	I/O
6	IO_L35P_6	IO_L35P_6	N1	I/O
6	IO_L38N_6	IO_L38N_6	M6	I/O
6	IO_L38P_6	IO_L38P_6	M5	I/O
6	IO_L39N_6	IO_L39N_6	M4	I/O
6	IO_L39P_6	IO_L39P_6	M3	I/O
6	IO_L40N_6	IO_L40N_6	M2	I/O
6	IO_L40P_6/VREF_6	IO_L40P_6/VREF_6	M1	VREF
6	VCCO_6	VCCO_6	M7	VCCO
6	VCCO_6	VCCO_6	N7	VCCO
6	VCCO_6	VCCO_6	P7	VCCO
6	VCCO_6	VCCO_6	R3	VCCO
6	VCCO_6	VCCO_6	R6	VCCO
7	IO	IO	C2	I/O
7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	C3	DCI
7	IO_L01P_7/VRN_7	IO_L01P_7/VRN_7	C4	DCI
7	IO_L16N_7	IO_L16N_7	D1	I/O
7	IO_L16P_7/VREF_7	IO_L16P_7/VREF_7	C1	VREF
7	IO_L17N_7	IO_L17N_7	E4	I/O
7	IO_L17P_7	IO_L17P_7	D4	I/O
7	IO_L19N_7/VREF_7	IO_L19N_7/VREF_7	D3	VREF
7	IO_L19P_7	IO_L19P_7	D2	I/O
7	IO_L20N_7	IO_L20N_7	F4	I/O
7	IO_L20P_7	IO_L20P_7	E3	I/O
7	IO_L21N_7	IO_L21N_7	E1	I/O
7	IO_L21P_7	IO_L21P_7	E2	I/O
7	IO_L22N_7	IO_L22N_7	G6	I/O
7	IO_L22P_7	IO_L22P_7	F5	I/O

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
1	N.C. (◆)	IO_L18P_1	IO_L18P_1	IO_L18P_1	IO[3]	C18	I/O
1	IO_L19N_1	IO_L19N_1	IO_L19N_1	IO_L19N_1	IO_L19N_1	F17	I/O
1	IO_L19P_1	IO_L19P_1	IO_L19P_1	IO_L19P_1	IO_L19P_1	G17	I/O
1	IO_L22N_1	IO_L22N_1	IO_L22N_1	IO_L22N_1	IO_L22N_1	D17	I/O
1	IO_L22P_1	IO_L22P_1	IO_L22P_1	IO_L22P_1	IO_L22P_1	E17	I/O
1	N.C. (◆)	IO_L23N_1	IO_L23N_1	IO_L23N_1	IO_L23N_1	A17	I/O
1	N.C. (◆)	IO_L23P_1	IO_L23P_1	IO_L23P_1	IO_L23P_1	B17	I/O
1	IO_L24N_1	IO_L24N_1	IO_L24N_1	IO_L24N_1	IO_L24N_1	G16	I/O
1	IO_L24P_1	IO_L24P_1	IO_L24P_1	IO_L24P_1	IO_L24P_1	H16	I/O
1	IO_L25N_1	IO_L25N_1	IO_L25N_1	IO_L25N_1	IO_L25N_1	E16	I/O
1	IO_L25P_1	IO_L25P_1	IO_L25P_1	IO_L25P_1	IO_L25P_1	F16	I/O
1	N.C. (◆)	IO_L26N_1	IO_L26N_1	IO_L26N_1	IO_L26N_1	A16	I/O
1	N.C. (◆)	IO_L26P_1	IO_L26P_1	IO_L26P_1	IO_L26P_1	B16	I/O
1	IO_L27N_1	IO_L27N_1	IO_L27N_1	IO_L27N_1	IO_L27N_1	G15	I/O
1	IO_L27P_1	IO_L27P_1	IO_L27P_1	IO_L27P_1	IO_L27P_1	H15	I/O
1	IO_L28N_1	IO_L28N_1	IO_L28N_1	IO_L28N_1	IO_L28N_1	E15	I/O
1	IO_L28P_1	IO_L28P_1	IO_L28P_1	IO_L28P_1	IO_L28P_1	F15	I/O
1	IO_L29N_1	IO_L29N_1	IO_L29N_1	IO_L29N_1	IO_L29N_1	A15	I/O
1	IO_L29P_1	IO_L29P_1	IO_L29P_1	IO_L29P_1	IO_L29P_1	B15	I/O
1	IO_L30N_1	IO_L30N_1	IO_L30N_1	IO_L30N_1	IO_L30N_1	G14	I/O
1	IO_L30P_1	IO_L30P_1	IO_L30P_1	IO_L30P_1	IO_L30P_1	H14	I/O
1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	D14	VREF
1	IO_L31P_1	IO_L31P_1	IO_L31P_1	IO_L31P_1	IO_L31P_1	E14	I/O
1	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	B14	GCLK
1	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	C14	GCLK
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	C16	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	C20	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	H17	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	H18	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	J14	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	J15	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	J16	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	K14	VCCO
2	N.C. (◆)	N.C. (■)	IO	IO	IO	F22	I/O
2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	C25	DCI
2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	C26	DCI
2	IO_L02N_2	IO_L02N_2	IO_L02N_2	IO_L02N_2	IO_L02N_2	E23	I/O
2	IO_L02P_2	IO_L02P_2	IO_L02P_2	IO_L02P_2	IO_L02P_2	E24	I/O
2	IO_L03N_2/VREF_2	IO_L03N_2/VREF_2[1]	IO_L03N_2/VREF_2	IO_L03N_2/VREF_2	IO_L03N_2/VREF_2	D25	VREF[1]
2	IO_L03P_2	IO_L03P_2	IO_L03P_2	IO_L03P_2	IO_L03P_2	D26	I/O
2	N.C. (◆)	IO_L05N_2	IO_L05N_2	IO_L05N_2	IO_L05N_2	E25	I/O
2	N.C. (◆)	IO_L05P_2	IO_L05P_2	IO_L05P_2	IO_L05P_2	E26	I/O

FG676 Footprint

Left Half of Package (Top View)

XC3S1000 (391 max. user I/O)

- 315 **I/O:** Unrestricted, general-purpose user I/O
- 40 **VREF:** User I/O or input voltage reference for bank
- 98 **N.C.:** Unconnected pins for XC3S1000 (◆)

XC3S1500 (487 max user I/O)

- 403 **I/O:** Unrestricted, general-purpose user I/O
- 48 **VREF:** User I/O or input voltage reference for bank
- 2 **N.C.:** Unconnected pins for XC3S1500 (■)

XC3S2000, XC3S4000, XC3S5000 (489 max user I/O)

- 405 **I/O:** Unrestricted, general-purpose user I/O
- 48 **VREF:** User I/O or input voltage reference for bank
- 0 **N.C.:** No unconnected pins

All devices

- 12 **DUAL:** Configuration pin, then possible user I/O
- 8 **GCLK:** User I/O or global clock buffer input
- 16 **DCI:** User I/O or reference resistor input for bank
- 7 **CONFIG:** Dedicated configuration pins
- 4 **JTAG:** Dedicated JTAG port pins
- 20 **VCCINT:** Internal core voltage supply (+1.2V)
- 64 **VCCO:** Output voltage supply for bank
- 16 **VCCAUX:** Auxiliary voltage supply (+2.5V)
- 76 **GND:** Ground

Bank 0

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	GND	VCCAUX	I/O	I/O L05P_0 VREF_0	I/O	I/O	I/O L10P_0	I/O L15P_0	VCCAUX	I/O L23P_0 ◆	I/O L26P_0 VREF_0 ◆	I/O L29P_0	I/O L32P_0 GCLK6
B	VCCAUX	GND	I/O VREF_0	I/O L05N_0	I/O L06P_0	I/O L08P_0	I/O L10N_0	I/O L15N_0	I/O L18P_0 ◆	I/O L23N_0 ◆	I/O L26N_0 ◆	I/O L29N_0	I/O L32N_0 GCLK7
C	TDI	HSWAP_EN	GND	I/O	I/O L06N_0	I/O L08N_0	VCCO_0	I/O ◆	I/O L18N_0 ◆	I/O L22P_0	VCCO_0	I/O	I/O L31P_0 VREF_0
D	I/O L03N_7 VREF_7	I/O L03P_7	PROG_B	GND	I/O L01P_0 VRN_0	I/O L07P_0	I/O L09P_0	I/O L12P_0 ◆	I/O L17P_0 ◆	I/O L22N_0	I/O L25P_0	GND	I/O L31N_0
E	I/O L06N_7 ◆	I/O L06P_7 ◆	I/O L02N_7	I/O L02P_7	I/O L01N_0 VRP_0	I/O L07N_0	I/O L09N_0	I/O L12N_0 ◆	I/O L17N_0 ◆	I/O L19P_0	I/O L25N_0	I/O L28P_0	I/O
F	I/O L09N_7 ◆	I/O L09P_7 ◆	I/O L07N_7 ◆	I/O L07P_7 ◆	I/O L01N_7 VRP_7	I/O L01P_7 VRN_7	I/O VREF_0	I/O L11P_0 ◆	I/O L16P_0	I/O L19N_0	I/O L24P_0	I/O L28N_0	I/O L30P_0
G	I/O L14N_7	I/O L14P_7	VCCO_7	I/O L08N_7 ◆	I/O L08P_7 ◆	I/O L05N_7 ◆	I/O L05P_7 ◆	I/O L11N_0 ◆	I/O L16N_0	I/O VREF_0	I/O L24N_0	I/O L27N_0	I/O L30N_0
H	I/O L19N_7 VREF_7	I/O L19P_7	I/O L17N_7	I/O L17P_7	I/O L16P_7 VREF_7	I/O L10N_7 ◆	I/O L10P_7 VREF_7 ◆	VCCINT	VCCO_0	VCCO_0	I/O	I/O	I/O L27P_0
J	VCCAUX	I/O L22N_7	I/O L22P_7	I/O L21N_7	I/O L21P_7	I/O L16N_7	I/O L20P_7	VCCO_7	VCCINT	VCCINT	VCCO_0	VCCO_0	VCCO_0
K	I/O L26N_7	I/O L26P_7	I/O L24N_7	I/O L24P_7	I/O L23N_7	I/O L23P_7	I/O L20N_7	VCCO_7	VCCINT	VCCINT	GND	GND	VCCO_0
L	I/O L29N_7	I/O L29P_7	VCCO_7	I/O L33P_7	I/O L28N_7	I/O L28P_7	I/O L27N_7	I/O L27P_7 VREF_7	VCCO_7	GND	GND	GND	GND
M	I/O L34N_7	I/O L34P_7	I/O L33N_7	GND	I/O L32P_7	I/O L32N_7	I/O L31N_7	I/O L31P_7	VCCO_7	GND	GND	GND	GND
N	I/O L40N_7 VREF_7	I/O L40P_7	I/O L39N_7	I/O L39P_7	I/O L38N_7	I/O L38P_7	I/O L35N_7	I/O L35P_7	VCCO_7	VCCO_7	GND	GND	GND
P	I/O L40P_6 VREF_6	I/O L40N_6	I/O L39P_6	I/O L39N_6	I/O L38P_6	I/O L38N_6	I/O L35P_6	I/O L35N_6	VCCO_6	VCCO_6	GND	GND	GND
R	I/O L34P_6	I/O L34N_6 VREF_6	I/O L33P_6	GND	I/O L32P_6	I/O L32N_6	I/O L31P_6	I/O L31N_6	VCCO_6	GND	GND	GND	GND
T	I/O L29P_6	I/O L29N_6	VCCO_6	I/O L33N_6	I/O L28P_6	I/O L28N_6	I/O L27P_6	I/O L27N_6	VCCO_6	GND	GND	GND	GND
U	I/O L26P_6	I/O L26N_6	I/O L24P_6	I/O L24N_6 VREF_6	I/O L23P_6	I/O L23N_6	I/O L20P_6	VCCO_6	VCCINT	VCCINT	GND	GND	VCCO_5
V	VCCAUX	I/O L22P_6	I/O L22N_6	I/O L21P_6	I/O L21N_6	I/O L16N_6	I/O L20N_6	VCCO_6	VCCINT	VCCINT	VCCO_5	VCCO_5	VCCO_5
W	I/O L19P_6	I/O L19N_6	I/O L17P_6 VREF_6	I/O L17N_6	I/O L16P_6	I/O L14P_6	I/O L14N_6	VCCINT	VCCO_5	VCCO_5	I/O L24P_5	I/O L27P_5	I/O L30P_5
Y	I/O L10P_6 ◆	I/O L10N_6 ◆	VCCO_6	I/O L08P_6 ◆	I/O L08N_6 ◆	I/O L06P_6 ◆	I/O L06N_6 ◆	I/O	I/O L16P_5	I/O L19P_5 VREF_5	I/O L24N_5	I/O L27N_5 VREF_5	I/O L30N_5
AA	I/O L09P_6 ◆	I/O L09N_6 VREF_6 ◆	I/O L07P_6 ◆	I/O L07N_6 ◆	I/O ◆■	I/O L05P_5	I/O	I/O L11P_5 ◆	I/O L16N_5	I/O L19N_5	I/O L25P_5	I/O L28P_5 D7	I/O
AB	I/O L05P_6 ◆	I/O L05N_6 ◆	I/O L02P_6	I/O L02N_6	I/O L01P_5 CS_B	I/O L05N_5	I/O L09P_5	I/O L11N_5 VREF_5 ◆	I/O	I/O L22P_5	I/O L25N_5	I/O L28N_5 D6	I/O L31P_5 D5
AC	I/O L03P_6	I/O L03N_6 VREF_6	M1	GND	I/O L01N_5 RDWR_B	I/O L07P_5	I/O L09N_5	I/O L12P_5 ◆	I/O ◆	I/O L22N_5	I/O	GND	I/O L31N_5 D4
AD	I/O L01P_6 VRN_6	I/O L01N_6 VRP_6	GND	I/O L04P_5	I/O L06P_5	I/O L07N_5	VCCO_5	I/O L12N_5 ◆	I/O L18P_5 ◆	I/O	VCCO_5	I/O	I/O L32P_5 GCLK2
AE	VCCAUX	GND	M0	I/O L04N_5	I/O L06N_5	I/O L08P_5	I/O L10P_5 VRN_5	I/O L15P_5	I/O L18N_5 ◆	I/O L23P_5 ◆	I/O L26P_5 ◆	I/O L29P_5 VREF_5	I/O L32N_5 GCLK3
AF	GND	VCCAUX	M2	I/O	I/O VREF_5	I/O L08N_5	I/O L10N_5 VRP_5	I/O L15N_5	VCCAUX	I/O L23N_5 ◆	I/O L26N_5 ◆	I/O L29N_5	I/O VREF_5

Bank 7

Bank 6

Bank 5

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Figure 53: **FG676 Package Footprint (Top View)**

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
3	IO_L21P_3	IO_L21P_3	Y23	I/O
3	IO_L22N_3	IO_L22N_3	Y26	I/O
3	IO_L22P_3	IO_L22P_3	Y25	I/O
3	IO_L23N_3	IO_L23N_3	Y28	I/O
3	IO_L23P_3/VREF_3	IO_L23P_3/VREF_3	Y27	VREF
3	IO_L24N_3	IO_L24N_3	Y30	I/O
3	IO_L24P_3	IO_L24P_3	Y29	I/O
3	IO_L26N_3	IO_L26N_3	W30	I/O
3	IO_L26P_3	IO_L26P_3	W29	I/O
3	IO_L27N_3	IO_L27N_3	V21	I/O
3	IO_L27P_3	IO_L27P_3	W21	I/O
3	IO_L28N_3	IO_L28N_3	V23	I/O
3	IO_L28P_3	IO_L28P_3	V22	I/O
3	IO_L29N_3	IO_L29N_3	V25	I/O
3	IO_L29P_3	IO_L29P_3	W26	I/O
3	IO_L31N_3	IO_L31N_3	V30	I/O
3	IO_L31P_3	IO_L31P_3	V29	I/O
3	IO_L32N_3	IO_L32N_3	U22	I/O
3	IO_L32P_3	IO_L32P_3	U21	I/O
3	IO_L33N_3	IO_L33N_3	U25	I/O
3	IO_L33P_3	IO_L33P_3	U24	I/O
3	IO_L34N_3	IO_L34N_3	U29	I/O
3	IO_L34P_3/VREF_3	IO_L34P_3/VREF_3	U28	VREF
3	IO_L35N_3	IO_L35N_3	T22	I/O
3	IO_L35P_3	IO_L35P_3	T21	I/O
3	IO_L37N_3	IO_L37N_3	T24	I/O
3	IO_L37P_3	IO_L37P_3	T23	I/O
3	IO_L38N_3	IO_L38N_3	T26	I/O
3	IO_L38P_3	IO_L38P_3	T25	I/O
3	IO_L39N_3	IO_L39N_3	T28	I/O
3	IO_L39P_3	IO_L39P_3	T27	I/O
3	IO_L40N_3/VREF_3	IO_L40N_3/VREF_3	T30	VREF
3	IO_L40P_3	IO_L40P_3	T29	I/O
3	N.C. (◆)	IO_L46N_3	W23	I/O
3	N.C. (◆)	IO_L46P_3	W22	I/O
3	N.C. (◆)	IO_L47N_3	W25	I/O
3	N.C. (◆)	IO_L47P_3	W24	I/O
3	N.C. (◆)	IO_L48N_3	W28	I/O
3	N.C. (◆)	IO_L48P_3	W27	I/O
3	N.C. (◆)	IO_L50N_3	V27	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
2	IO_L19N_2	IO_L19N_2	M29	I/O
2	IO_L19P_2	IO_L19P_2	M30	I/O
2	IO_L20N_2	IO_L20N_2	M31	I/O
2	IO_L20P_2	IO_L20P_2	M32	I/O
2	IO_L21N_2	IO_L21N_2	M26	I/O
2	IO_L21P_2	IO_L21P_2	N25	I/O
2	IO_L22N_2	IO_L22N_2	N27	I/O
2	IO_L22P_2	IO_L22P_2	N28	I/O
2	IO_L23N_2/VREF_2	IO_L23N_2VREF_2	N31	VREF
2	IO_L23P_2	IO_L23P_2	N32	I/O
2	IO_L24N_2	IO_L24N_2	N24	I/O
2	IO_L24P_2	IO_L24P_2	P24	I/O
2	IO_L26N_2	IO_L26N_2	P29	I/O
2	IO_L26P_2	IO_L26P_2	P30	I/O
2	IO_L27N_2	IO_L27N_2	P31	I/O
2	IO_L27P_2	IO_L27P_2	P32	I/O
2	IO_L28N_2	IO_L28N_2	P33	I/O
2	IO_L28P_2	IO_L28P_2	P34	I/O
2	IO_L29N_2	IO_L29N_2	R24	I/O
2	IO_L29P_2	IO_L29P_2	R25	I/O
2	IO_L30N_2	IO_L30N_2	R28	I/O
2	IO_L30P_2	IO_L30P_2	R29	I/O
2	IO_L31N_2	IO_L31N_2	R31	I/O
2	IO_L31P_2	IO_L31P_2	R32	I/O
2	IO_L32N_2	IO_L32N_2	R33	I/O
2	IO_L32P_2	IO_L32P_2	R34	I/O
2	IO_L33N_2	IO_L33N_2	R26	I/O
2	IO_L33P_2	IO_L33P_2	T25	I/O
2	IO_L34N_2/VREF_2	IO_L34N_2/VREF_2	T28	VREF
2	IO_L34P_2	IO_L34P_2	T29	I/O
2	IO_L35N_2	IO_L35N_2	T32	I/O
2	IO_L35P_2	IO_L35P_2	T33	I/O
2	IO_L37N_2	IO_L37N_2	U27	I/O
2	IO_L37P_2	IO_L37P_2	U28	I/O
2	IO_L38N_2	IO_L38N_2	U29	I/O
2	IO_L38P_2	IO_L38P_2	U30	I/O
2	IO_L39N_2	IO_L39N_2	U31	I/O
2	IO_L39P_2	IO_L39P_2	U32	I/O
2	IO_L40N_2	IO_L40N_2	U33	I/O
2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	U34	VREF

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
N/A	VCCAUX	VCCAUX	Y5	VCCAUX
N/A	VCCINT	VCCINT	AA13	VCCINT
N/A	VCCINT	VCCINT	AA22	VCCINT
N/A	VCCINT	VCCINT	AB13	VCCINT
N/A	VCCINT	VCCINT	AB14	VCCINT
N/A	VCCINT	VCCINT	AB15	VCCINT
N/A	VCCINT	VCCINT	AB16	VCCINT
N/A	VCCINT	VCCINT	AB19	VCCINT
N/A	VCCINT	VCCINT	AB20	VCCINT
N/A	VCCINT	VCCINT	AB21	VCCINT
N/A	VCCINT	VCCINT	AB22	VCCINT
N/A	VCCINT	VCCINT	AC12	VCCINT
N/A	VCCINT	VCCINT	AC17	VCCINT
N/A	VCCINT	VCCINT	AC18	VCCINT
N/A	VCCINT	VCCINT	AC23	VCCINT
N/A	VCCINT	VCCINT	M12	VCCINT
N/A	VCCINT	VCCINT	M17	VCCINT
N/A	VCCINT	VCCINT	M18	VCCINT
N/A	VCCINT	VCCINT	M23	VCCINT
N/A	VCCINT	VCCINT	N13	VCCINT
N/A	VCCINT	VCCINT	N14	VCCINT
N/A	VCCINT	VCCINT	N15	VCCINT
N/A	VCCINT	VCCINT	N16	VCCINT
N/A	VCCINT	VCCINT	N19	VCCINT
N/A	VCCINT	VCCINT	N20	VCCINT
N/A	VCCINT	VCCINT	N21	VCCINT
N/A	VCCINT	VCCINT	N22	VCCINT
N/A	VCCINT	VCCINT	P13	VCCINT
N/A	VCCINT	VCCINT	P22	VCCINT
N/A	VCCINT	VCCINT	R13	VCCINT
N/A	VCCINT	VCCINT	R22	VCCINT
N/A	VCCINT	VCCINT	T13	VCCINT
N/A	VCCINT	VCCINT	T22	VCCINT
N/A	VCCINT	VCCINT	U12	VCCINT
N/A	VCCINT	VCCINT	U23	VCCINT
N/A	VCCINT	VCCINT	V12	VCCINT
N/A	VCCINT	VCCINT	V23	VCCINT
N/A	VCCINT	VCCINT	W13	VCCINT
N/A	VCCINT	VCCINT	W22	VCCINT
N/A	VCCINT	VCCINT	Y13	VCCINT