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Understanding Embedded - FPGAs (Field Programmable Gate Array)

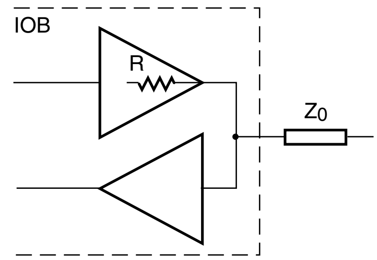
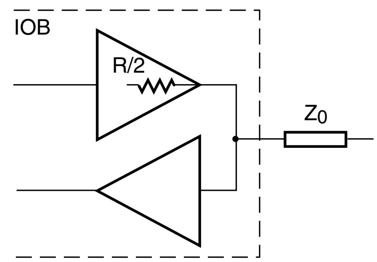
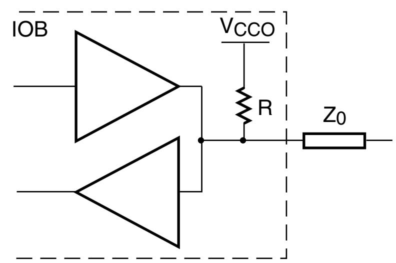
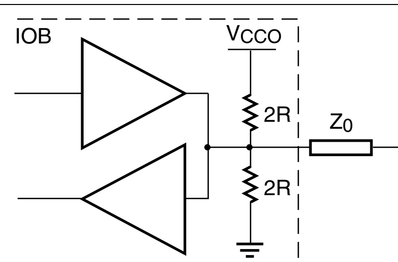
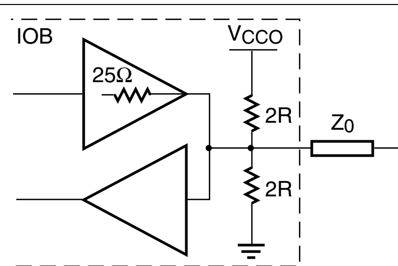
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	192
Number of Logic Elements/Cells	1728
Total RAM Bits	73728
Number of I/O	97
Number of Gates	50000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s50-4tq144c

Table 11: **DCI Terminations**

Termination	Schematic[(1)]	Signal Standards (IOSTANDARD)
Controlled impedance output driver	 ds099_06a_070903	LVDCI_15 LVDCI_18 LVDCI_25 LVDCI_33 HSLVDCI_15 HSLVDCI_18 HSLVDCI_25 HSLVDCI_33
Controlled output driver with half impedance	 ds099_06b_070903	LVDCI_DV2_15 LVDCI_DV2_18 LVDCI_DV2_25 LVDCI_DV2_33
Single resistor	 ds099_06c_070903	GTL_DCI GTLP_DCI HSTL_III_DCI[(2)] HSTL_III_DCI_18[(2)]
Split resistors	 ds099_06d_070903	HSTL_I_DCI[(2)] HSTL_I_DCI_18[(2)] HSTL_II_DCI_18 DIFF_HSTL_II_18_DCI DIFF_SSTL2_II_DCI LVDS_25_DCI LVDSEXT_25_DCI
Split resistors with output driver impedance fixed to 25Ω	 ds099_06e_070903	SSTL18_I_DCI[(3)] SSTL2_I_DCI[(3)] SSTL2_II_DCI

Notes:
1. The value of R is equivalent to the characteristic impedance of the line connected to the I/O. It is also equal to half the value of RREF for the DV2 standards and RREF for all other DCI standards.
2. For DCI using HSTL Classes I and III, terminations only go into effect at inputs (not at outputs).
3. For DCI using SSTL Class I, the split termination only goes into effect at inputs (not at outputs).

In contrast, the 144-pin Thin Quad Flat Pack (TQ144) package and the 132-pin Chip-Scale Package (CP132) tie V_{CCO} together internally for the pair of banks on each side of the device. For example, the V_{CCO} Bank 0 and the V_{CCO} Bank 1 lines are tied together. The interconnected bank-pairs are 0/1, 2/3, 4/5, and 6/7. As a result, Spartan-3 devices in the CP132 and TQ144 packages support four independent V_{CCO} supplies.

Note: The CP132 package is discontinued. See http://www.xilinx.com/support/documentation /spartan-3_customer_notices.htm.

Spartan-3 FPGA Compatibility

Within the Spartan-3 family, all devices are pin-compatible by package. When the need for future logic resources outgrows the capacity of the Spartan-3 device in current use, a larger device in the same package can serve as a direct replacement. Larger devices may add extra V_{REF} and V_{CCO} lines to support a greater number of I/Os. In the larger device, more pins can convert from user I/Os to V_{REF} lines. Also, additional V_{CCO} lines are bonded out to pins that were "not connected" in the smaller device. Thus, it is important to plan for future upgrades at the time of the board's initial design by laying out connections to the extra pins.

The Spartan-3 family is not pin-compatible with any previous Xilinx FPGA family or with other platforms among the Spartan-3 Generation FPGAs.

Rules Concerning Banks

When assigning I/Os to banks, it is important to follow the following V_{CCO} rules:

- Leave no V_{CCO} pins unconnected on the FPGA.
- Set all V_{CCO} lines associated with the (interconnected) bank to the same voltage level.
- The V_{CCO} levels used by all standards assigned to the I/Os of the (interconnected) bank(s) must agree. The Xilinx development software checks for this. Tables 8, 9, and 10 describe how different standards use the V_{CCO} supply.
- Only one of the following standards is allowed on outputs per bank: LVDS, LDT, LVDS_EXT, or RSDS. This restriction is for the eight banks in each device, even if the V_{CCO} levels are shared across banks, as in the CP132 and TQ144 packages.
- If none of the standards assigned to the I/Os of the (interconnected) bank(s) uses V_{CCO}, tie all associated V_{CCO} lines to 2.5V.
- In general, apply 2.5V to V_{CCO} Bank 4 from power-on to the end of configuration. Apply the same voltage to V_{CCO} Bank 5 during parallel configuration or a Readback operation. For information on how to program the FPGA using 3.3V signals and power, see the 3.3V-Tolerant Configuration Interface section.

If any of the standards assigned to the Inputs of the bank use V_{REF}, then observe the following additional rules:

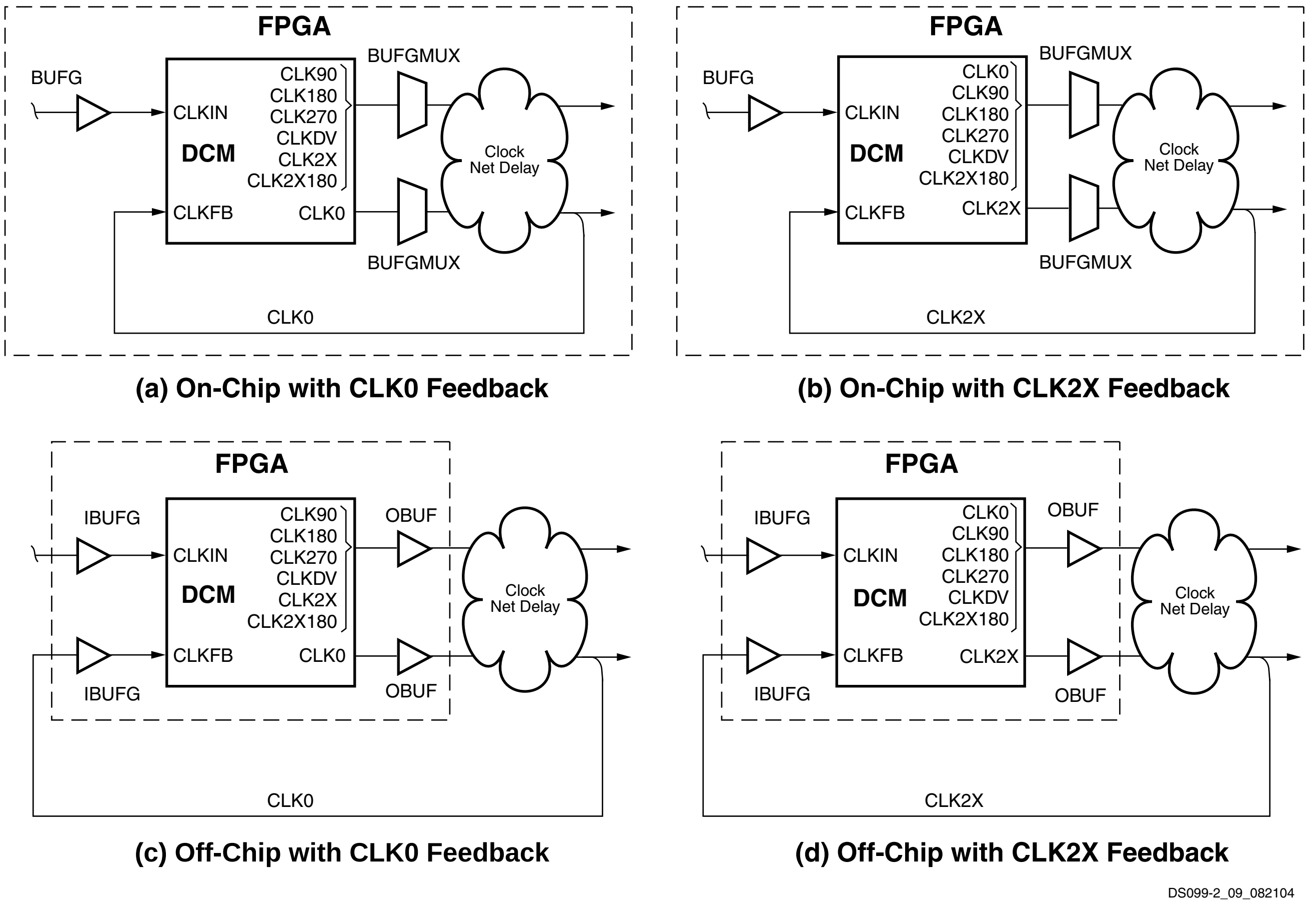
- Connect *all* V_{REF} pins within the bank to the same voltage level.
- The V_{REF} levels used by all standards assigned to the Inputs of the bank must agree. The Xilinx development software checks for this. Tables 8 and 10 describe how different standards use the V_{REF} supply.

If none of the standards assigned to the Inputs of a bank use V_{REF} for biasing input switching thresholds, all associated V_{REF} pins function as User I/Os.

Exceptions to Banks Supporting I/O Standards

Bank 5 of any Spartan-3 device in a VQ100, CP132, or TQ144 package does not support DCI signal standards. In this case, bank 5 has neither VRN nor VRP pins.

Furthermore, banks 4 and 5 of any Spartan-3 device in a VQ100 package do not support signal standards using V_{REF} (see Table 8). In this case, the two banks do not have any V_{REF} pins.



Notes:

1. In the Low Frequency mode, all seven DLL outputs are available. In the High Frequency mode, only the CLK0, CLK180, and CLKDV outputs are available.

Figure 21: **Input Clock, Output Clock, and Feedback Connections for the DLL**

In the on-chip synchronization case (the [a] and [b] sections of Figure 21), it is possible to connect any of the DLL's seven output clock signals through general routing resources to the FPGA's internal registers. Either a Global Clock Buffer (BUFG) or a BUFGMUX affords access to the global clock network. As shown in the [a] section of Figure 21, the feedback loop is created by routing CLK0 (or CLK2X, in the [b] section) to a global clock net, which in turn drives the CLKFB input.

In the off-chip synchronization case (the [c] and [d] sections of Figure 21), CLK0 (or CLK2X) plus any of the DLL's other output clock signals exit the FPGA using output buffers (OBUF) to drive an external clock network plus registers on the board. As shown in the [c] section of Figure 21, the feedback loop is formed by feeding CLK0 (or CLK2X, in the [d] section) back into the FPGA using an IBUFG, which directly accesses the global clock network, or an IBUF. Then, the global clock net is connected directly to the CLKFB input.

DLL Frequency Modes

The DLL supports two distinct operating modes, High Frequency and Low Frequency, with each specified over a different clock frequency range. The DLL_FREQUENCY_MODE attribute chooses between the two modes. When the attribute is set to LOW, the Low Frequency mode permits all seven DLL clock outputs to operate over a low-to-moderate frequency range. When the attribute is set to HIGH, the High Frequency mode allows the CLK0, CLK180 and CLKDV outputs to operate at the highest possible frequencies. The remaining DLL clock outputs are not available for use in High Frequency mode.

Accommodating High Input Frequencies

If the frequency of the CLKIN signal is high such that it exceeds the maximum permitted, divide it down to an acceptable value using the CLKIN_DIVIDE_BY_2 attribute. When this attribute is set to TRUE, the CLKIN frequency is divided by a factor of two just as it enters the DCM.

Table 47: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
PCI33_3	0.74	0.85	ns
SSTL18_I	0.07	0.07	ns
SSTL18_I_DCI	0.22	0.25	ns
SSTL18_II	0.30	0.34	ns
SSTL2_I	0.23	0.26	ns
SSTL2_I_DCI	0.19	0.22	ns
SSTL2_II	0.13	0.15	ns
SSTL2_II_DCI	0.10	0.11	ns
Differential Standards			
LDT_25 (ULVDS_25)	–0.06	–0.05	ns
LVDS_25	–0.09	–0.07	ns
BLVDS_25	0.02	0.04	ns
LVDSEXT_25	–0.15	–0.13	ns
LVPECL_25	0.16	0.18	ns
RSDS_25	0.05	0.06	ns
DIFF_HSTL_II_18	–0.02	–0.01	ns
DIFF_HSTL_II_18_DCI	0.75	0.86	ns
DIFF_SSTL2_II	0.13	0.15	ns
DIFF_SSTL2_II_DCI	0.10	0.11	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32, Table 35, and Table 37.
2. These adjustments are used to convert output- and three-state-path times originally specified for the LVCMOS25 standard with 12 mA drive and Fast slew rate to times that correspond to other signal standards. Do not adjust times that measure when outputs go into a high-impedance state.
3. For minimums, use the values reported by the Xilinx timing analyzer.

Table 50: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}/GND Pair *(Cont'd)***

Signal Standard (IOSTANDARD)			Package				
			VQ100	TQ144	PQ208	CP132	FT256, FG320, FG456, FG676, FG900, FG1156
LVDCI_15			6	6	6	6	14
LVDCI_DV2_15			6	6	6	6	14
HSLVDCI_15			6	6	6	6	14
LVCMOS18	Slow	2	19	13	13	29	64
		4	13	8	8	19	34
		6	8	8	8	9	22
		8	7	7	7	9	18
		12	5	5	5	5	13
		16	5	5	5	5	10
	Fast	2	13	13	13	19	36
		4	8	8	8	13	21
		6	8	8	8	8	13
		8	7	7	7	7	10
		12	5	5	5	5	9
		16	5	5	5	5	6
LVDCI_18			7	7	7	7	10
LVDCI_DV2_18			7	7	7	7	10
HSLVDCI_18			7	7	7	7	10
LVCMOS25	Slow	2	28	16	12	42	76
		4	13	10	10	19	46
		6	13	8	8	19	33
		8	7	7	7	9	24
		12	6	6	6	9	18
		16	6	6	6	6	11
		24	5	5	5	5	7
	Fast	2	17	12	12	26	42
		4	10	10	10	13	20
		6	8	8	8	13	15
		8	7	7	7	7	13
		12	6	6	6	6	11
		16	6	6	6	6	8
		24	5	5	5	5	5
LVDCI_25			7	7	7	7	11
LVDCI_DV2_25			7	7	7	7	11
HSLVDCI_25			7	7	7	7	11

Table 54: **Synchronous 18 x 18 Multiplier Timing**

Symbol	Description	P Outputs	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Clock-to-Output Times							
T_{MULTCK}	When reading from the Multiplier, the time from the active transition at the C clock input to data appearing at the P outputs	P[0]	–	1.00	–	1.15	ns
		P[15]	–	1.15	–	1.32	ns
		P[17]	–	1.30	–	1.50	ns
		P[19]	–	1.45	–	1.67	ns
		P[23]	–	1.76	–	2.02	ns
		P[31]	–	2.37	–	2.72	ns
		P[35]	–	2.67	–	3.07	ns
Setup Times							
$T_{MULIDCK}$	Time from the setup of data at the A and B inputs to the active transition at the C input of the Multiplier	-	1.84	–	2.11	–	ns
Hold Times							
$T_{MULCKID}$	Time from the active transition at the Multiplier's C input to the point where data is last held at the A and B inputs	-	0	–	0	–	ns

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 32.

Table 55: **Asynchronous 18 x 18 Multiplier Timing**

Symbol	Description	P Outputs	Speed Grade		Units
			-5	-4	
			Max	Max	
Propagation Times					
T_{MULT}	The time it takes for data to travel from the A and B inputs to the P outputs	P[0]	1.55	1.78	ns
		P[15]	3.15	3.62	ns
		P[17]	3.36	3.86	ns
		P[19]	3.49	4.01	ns
		P[23]	3.73	4.29	ns
		P[31]	4.23	4.86	ns
		P[35]	4.47	5.14	ns

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 32.

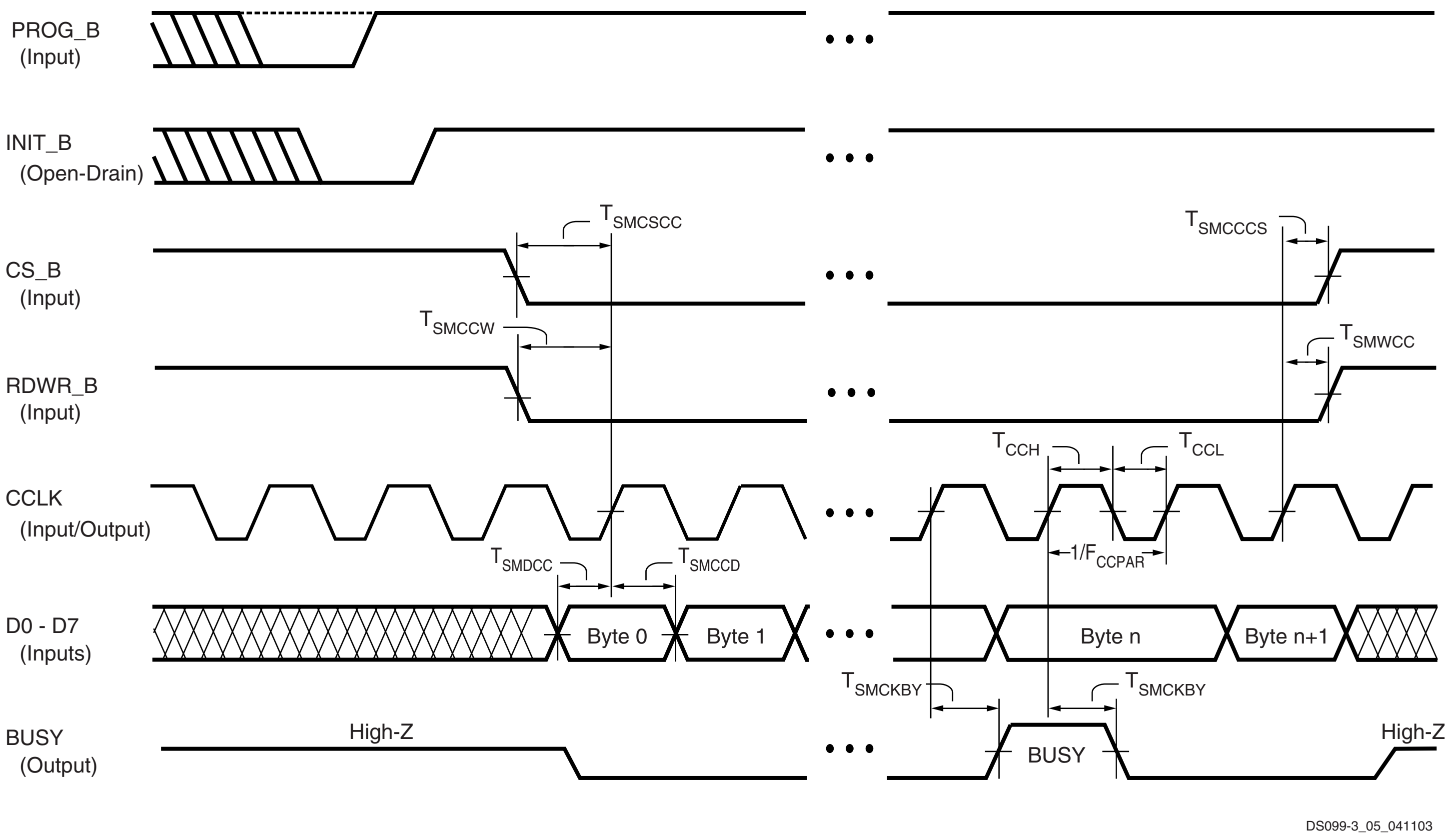


Figure 38: **Waveforms for Master and Slave Parallel Configuration**

Table 67: **Timing for the Master and Slave Parallel Configuration Modes**

Symbol	Description	Slave/ Master	All Speed Grades		Units
			Min	Max	
Clock-to-Output Times					
T_{SMCKBY}	The time from the rising transition on the CCLK pin to a signal transition at the BUSY pin	Slave	–	12.0	ns
Setup Times					
T_{SMDCC}	The time from the setup of data at the D0-D7 pins to the rising transition at the CCLK pin	Both	10.0	–	ns
T_{SMCSCC}	The time from the setup of a logic level at the CS_B pin to the rising transition at the CCLK pin		10.0	–	ns
T_{SMCCW}(3)	The time from the setup of a logic level at the RDWR_B pin to the rising transition at the CCLK pin		10.0	–	ns
Hold Times					
T_{SMCCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the D0-D7 pins	Both	0	–	ns
T_{SMCCCS}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the CS_B pin		0	–	ns
T_{SMWCC}(3)	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the RDWR_B pin		0	–	ns

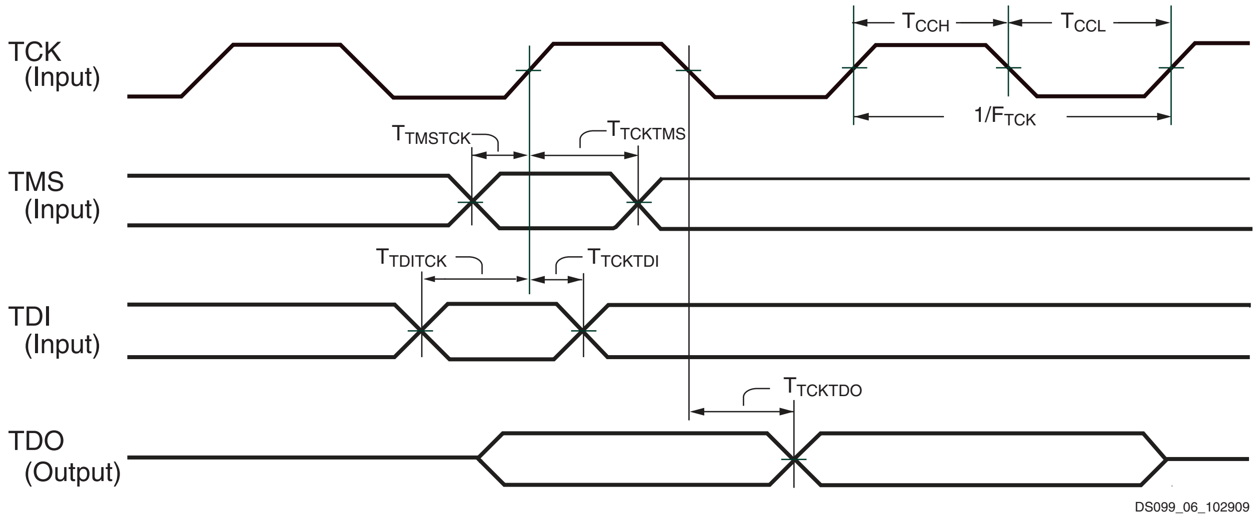


Figure 39: **JTAG Waveforms**

Table 68: **Timing for the JTAG Test Access Port**

Symbol	Description		All Speed Grades		Units
			Min	Max	
Clock-to-Output Times					
T_{TCKTDO}	The time from the falling transition on the TCK pin to data appearing at the TDO pin		1.0	11.0	ns
Setup Times					
T_{TDITCK}	The time from the setup of data at the TDI pin to the rising transition at the TCK pin		7.0	–	ns
T_{TMSTCK}	The time from the setup of a logic level at the TMS pin to the rising transition at the TCK pin		7.0	–	ns
Hold Times					
T_{TCKTDI}	The time from the rising transition at the TCK pin to the point when data is last held at the TDI pin		0	–	ns
T_{TCKTMS}	The time from the rising transition at the TCK pin to the point when a logic level is last held at the TMS pin		0	–	ns
Clock Timing					
T_{TCKH}	TCK pin High pulse width		5	∞	ns
T_{TCKL}	TCK pin Low pulse width		5	∞	ns
F_{TCK}	Frequency of the TCK signal	JTAG Configuration	0	33	MHz
		Boundary-Scan	0	25	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32.

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CP132: 132-Ball Chip-Scale Package

Note: The CP132 and CPG132 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.

The pinout and footprint for the XC3S50 in the 132-ball chip-scale package, CP132, appear in Table 89 and Figure 45.

All the package pins appear in Table 89 and are sorted by bank number, then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The CP132 footprint has eight I/O banks. However, the voltage supplies for the two I/O banks along an edge are connected together internally. Consequently, there are four output voltage supplies, labeled VCCO_TOP, VCCO_RIGHT, VCCO_BOTTOM, and VCCO_LEFT.

Pinout Table

Table 89: **CP132 Package Pinout**

Bank	XC3S50 Pin Name	CP132 Ball	Type
0	IO_L01N_0/VRP_0	A3	DCI
0	IO_L01P_0/VRN_0	C4	DCI
0	IO_L27N_0	C5	I/O
0	IO_L27P_0	B5	I/O
0	IO_L30N_0	B6	I/O
0	IO_L30P_0	A6	I/O
0	IO_L31N_0	C7	I/O
0	IO_L31P_0/VREF_0	B7	VREF
0	IO_L32N_0/GCLK7	A7	GCLK
0	IO_L32P_0/GCLK6	C8	GCLK
1	IO_L01N_1/VRP_1	A13	DCI
1	IO_L01P_1/VRN_1	B13	DCI
1	IO_L27N_1	C11	I/O
1	IO_L27P_1	A12	I/O
1	IO_L28N_1	A11	I/O
1	IO_L28P_1	B11	I/O
1	IO_L31N_1/VREF_1	C9	VREF
1	IO_L31P_1	A10	I/O
1	IO_L32N_1/GCLK5	A8	GCLK
1	IO_L32P_1/GCLK4	A9	GCLK
2	IO_L01N_2/VRP_2	D12	DCI
2	IO_L01P_2/VRN_2	C14	DCI
2	IO_L20N_2	E12	I/O
2	IO_L20P_2	E13	I/O
2	IO_L21N_2	E14	I/O
2	IO_L21P_2	F12	I/O
2	IO_L23N_2/VREF_2	F13	VREF
2	IO_L23P_2	F14	I/O
2	IO_L24N_2	G12	I/O

Table 93: **PQ208 Package Pinout *(Cont'd)***

Bank	XC3S50 Pin Name	XC3S200, XC3S400 Pin Names	PQ208 Pin Number	Type
5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	P61	DCI
5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	P65	VREF
5	IO_L27P_5	IO_L27P_5	P64	I/O
5	IO_L28N_5/D6	IO_L28N_5/D6	P68	DUAL
5	IO_L28P_5/D7	IO_L28P_5/D7	P67	DUAL
5	IO_L31N_5/D4	IO_L31N_5/D4	P74	DUAL
5	IO_L31P_5/D5	IO_L31P_5/D5	P72	DUAL
5	IO_L32N_5/GCLK3	IO_L32N_5/GCLK3	P77	GCLK
5	IO_L32P_5/GCLK2	IO_L32P_5/GCLK2	P76	GCLK
5	VCCO_5	VCCO_5	P60	VCCO
5	VCCO_5	VCCO_5	P73	VCCO
6	N.C. (◆)	IO/VREF_6	P50	VREF
6	IO_L01N_6/VRP_6	IO_L01N_6/VRP_6	P52	DCI
6	IO_L01P_6/VRN_6	IO_L01P_6/VRN_6	P51	DCI
6	IO_L19N_6	IO_L19N_6	P48	I/O
6	IO_L19P_6	IO_L19P_6	P46	I/O
6	IO_L20N_6	IO_L20N_6	P45	I/O
6	IO_L20P_6	IO_L20P_6	P44	I/O
6	IO_L21N_6	IO_L21N_6	P43	I/O
6	IO_L21P_6	IO_L21P_6	P42	I/O
6	IO_L22N_6	IO_L22N_6	P40	I/O
6	IO_L22P_6	IO_L22P_6	P39	I/O
6	IO_L23N_6	IO_L23N_6	P37	I/O
6	IO_L23P_6	IO_L23P_6	P36	I/O
6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	P35	VREF
6	IO_L24P_6	IO_L24P_6	P34	I/O
6	N.C. (◆)	IO_L39N_6	P33	I/O
6	N.C. (◆)	IO_L39P_6	P31	I/O
6	IO_L40N_6	IO_L40N_6	P29	I/O
6	IO_L40P_6/VREF_6	IO_L40P_6/VREF_6	P28	VREF
6	VCCO_6	VCCO_6	P32	VCCO
6	VCCO_6	VCCO_6	P49	VCCO
7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	P3	DCI
7	IO_L01P_7/VRN_7	IO_L01P_7/VRN_7	P2	DCI
7	N.C. (◆)	IO_L16N_7	P5	I/O
7	N.C. (◆)	IO_L16P_7/VREF_7	P4	VREF
7	IO_L19N_7/VREF_7	IO_L19N_7/VREF_7	P9	VREF
7	IO_L19P_7	IO_L19P_7	P7	I/O
7	IO_L20N_7	IO_L20N_7	P11	I/O
7	IO_L20P_7	IO_L20P_7	P10	I/O

FT256: 256-lead Fine-pitch Thin Ball Grid Array

The 256-lead fine-pitch thin ball grid array package, FT256, supports three different Spartan-3 devices, including the XC3S200, the XC3S400, and the XC3S1000. The footprints for all three devices are identical, as shown in Table 96 and Figure 49.

All the package pins appear in Table 96 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

Pinout Table

Table 96: **FT256 Package Pinout**

Bank	XC3S200, XC3S400, XC3S1000 Pin Name	FT256 Pin Number	Type
0	IO	A5	I/O
0	IO	A7	I/O
0	IO/VREF_0	A3	VREF
0	IO/VREF_0	D5	VREF
0	IO_L01N_0/VRP_0	B4	DCI
0	IO_L01P_0/VRN_0	A4	DCI
0	IO_L25N_0	C5	I/O
0	IO_L25P_0	B5	I/O
0	IO_L27N_0	E6	I/O
0	IO_L27P_0	D6	I/O
0	IO_L28N_0	C6	I/O
0	IO_L28P_0	B6	I/O
0	IO_L29N_0	E7	I/O
0	IO_L29P_0	D7	I/O
0	IO_L30N_0	C7	I/O
0	IO_L30P_0	B7	I/O
0	IO_L31N_0	D8	I/O
0	IO_L31P_0/VREF_0	C8	VREF
0	IO_L32N_0/GCLK7	B8	GCLK
0	IO_L32P_0/GCLK6	A8	GCLK
0	VCCO_0	E8	VCCO
0	VCCO_0	F7	VCCO
0	VCCO_0	F8	VCCO
1	IO	A9	I/O
1	IO	A12	I/O
1	IO	C10	I/O
1	IO/VREF_1	D12	VREF
1	IO_L01N_1/VRP_1	A14	DCI
1	IO_L01P_1/VRN_1	B14	DCI

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
4	IO_L31P_4/ DOUT/BUSY	V10	DUAL
4	IO_L32N_4/GCLK1	N10	GCLK
4	IO_L32P_4/GCLK0	P10	GCLK
4	VCCO_4	M10	VCCO
4	VCCO_4	M11	VCCO
4	VCCO_4	T13	VCCO
4	VCCO_4	U11	VCCO
5	IO	N8	I/O
5	IO	P8	I/O
5	IO	U6	I/O
5	IO/VREF_5	R9	VREF
5	IO_L01N_5/RDWR_B	V3	DUAL
5	IO_L01P_5/CS_B	V2	DUAL
5	IO_L06N_5	T5	I/O
5	IO_L06P_5	T4	I/O
5	IO_L10N_5/VRP_5	V4	DCI
5	IO_L10P_5/VRN_5	U4	DCI
5	IO_L15N_5	R6	I/O
5	IO_L15P_5	R5	I/O
5	IO_L16N_5	V5	I/O
5	IO_L16P_5	U5	I/O
5	IO_L27N_5/VREF_5	P6	VREF
5	IO_L27P_5	P7	I/O
5	IO_L28N_5/D6	R7	DUAL
5	IO_L28P_5/D7	T7	DUAL
5	IO_L29N_5	V8	I/O
5	IO_L29P_5/VREF_5	V7	VREF
5	IO_L30N_5	R8	I/O
5	IO_L30P_5	T8	I/O
5	IO_L31N_5/D4	U9	DUAL
5	IO_L31P_5/D5	V9	DUAL
5	IO_L32N_5/GCLK3	N9	GCLK
5	IO_L32P_5/GCLK2	P9	GCLK
5	VCCO_5	M8	VCCO
5	VCCO_5	M9	VCCO
5	VCCO_5	T6	VCCO
5	VCCO_5	U8	VCCO
6	IO	K6	I/O
6	IO_L01N_6/VRP_6	T3	DCI

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
7	IO_L20P_7	E1	I/O
7	IO_L21N_7	E4	I/O
7	IO_L21P_7	F4	I/O
7	IO_L22N_7	G5	I/O
7	IO_L22P_7	F5	I/O
7	IO_L23N_7	G1	I/O
7	IO_L23P_7	F2	I/O
7	IO_L24N_7	G4	I/O
7	IO_L24P_7	G3	I/O
7	IO_L27N_7	H5	I/O
7	IO_L27P_7/VREF_7	H6	VREF
7	IO_L34N_7	H4	I/O
7	IO_L34P_7	H3	I/O
7	IO_L35N_7	H1	I/O
7	IO_L35P_7	H2	I/O
7	IO_L39N_7	J1	I/O
7	IO_L39P_7	J2	I/O
7	IO_L40N_7/VREF_7	J5	VREF
7	IO_L40P_7	J4	I/O
7	VCCO_7	F3	VCCO
7	VCCO_7	H7	VCCO
7	VCCO_7	J7	VCCO
N/A	GND	A1	GND
N/A	GND	A13	GND
N/A	GND	A18	GND
N/A	GND	A6	GND
N/A	GND	B17	GND
N/A	GND	B2	GND
N/A	GND	C10	GND
N/A	GND	C9	GND
N/A	GND	F1	GND
N/A	GND	F18	GND
N/A	GND	G12	GND
N/A	GND	G7	GND
N/A	GND	H10	GND
N/A	GND	H11	GND
N/A	GND	H8	GND
N/A	GND	H9	GND
N/A	GND	J11	GND
N/A	GND	J16	GND

FG456: 456-lead Fine-pitch Ball Grid Array

The 456-lead fine-pitch ball grid array package, FG456, supports four different Spartan-3 devices, including the XC3S400, the XC3S1000, the XC3S1500, and the XC3S2000. The footprints for the XC3S1000, the XC3S1500, and the XC3S2000 are identical, as shown in Table 100 and Figure 51. The XC3S400, however, has fewer I/O pins which consequently results in 69 unconnected pins on the FG456 package, labeled as "N.C." In Table 100 and Figure 51, these unconnected pins are indicated with a black diamond symbol (◆).

All the package pins appear in Table 100 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

If there is a difference between the XC3S400 pinout and the pinout for the XC3S1000, the XC3S1500, or the XC3S2000, then that difference is highlighted in Table 100. If the table entry is shaded grey, then there is an unconnected pin on the XC3S400 that maps to a user-I/O pin on the XC3S1000, XC3S1500, and XC3S2000. If the table entry is shaded tan, then the unconnected pin on the XC3S400 maps to a VREF-type pin on the XC3S1000, the XC3S1500, or the XC3S2000. If the other VREF pins in the bank all connect to a voltage reference to support a special I/O standard, then also connect the N.C. pin on the XC3S400 to the same VREF voltage. This provides maximum flexibility as you could potentially migrate a design from the XC3S400 device to an XC3S1000, an XC3S1500, or an XC3S2000 FPGA without changing the printed circuit board.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

Pinout Table

Table 100: **FG456 Package Pinout**

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
0	IO	IO	A10	I/O
0	IO	IO	D9	I/O
0	IO	IO	D10	I/O
0	IO	IO	F6	I/O
0	IO/VREF_0	IO/VREF_0	A3	VREF
0	IO/VREF_0	IO/VREF_0	C7	VREF
0	N.C. (◆)	IO/VREF_0	E5	VREF
0	IO/VREF_0	IO/VREF_0	F7	VREF
0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	B4	DCI
0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	A4	DCI
0	IO_L06N_0	IO_L06N_0	D5	I/O
0	IO_L06P_0	IO_L06P_0	C5	I/O
0	IO_L09N_0	IO_L09N_0	B5	I/O
0	IO_L09P_0	IO_L09P_0	A5	I/O
0	IO_L10N_0	IO_L10N_0	E6	I/O
0	IO_L10P_0	IO_L10P_0	D6	I/O
0	IO_L15N_0	IO_L15N_0	C6	I/O
0	IO_L15P_0	IO_L15P_0	B6	I/O
0	IO_L16N_0	IO_L16N_0	E7	I/O
0	IO_L16P_0	IO_L16P_0	D7	I/O
0	N.C. (◆)	IO_L19N_0	B7	I/O
0	N.C. (◆)	IO_L19P_0	A7	I/O

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
6	N.C. (◆)	IO_L28N_6	R5	I/O
6	N.C. (◆)	IO_L28P_6	P6	I/O
6	N.C. (◆)	IO_L29N_6	R2	I/O
6	N.C. (◆)	IO_L29P_6	R1	I/O
6	N.C. (◆)	IO_L31N_6	P5	I/O
6	N.C. (◆)	IO_L31P_6	P4	I/O
6	N.C. (◆)	IO_L32N_6	P2	I/O
6	N.C. (◆)	IO_L32P_6	P1	I/O
6	N.C. (◆)	IO_L33N_6	N6	I/O
6	N.C. (◆)	IO_L33P_6	N5	I/O
6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	N4	VREF
6	IO_L34P_6	IO_L34P_6	N3	I/O
6	IO_L35N_6	IO_L35N_6	N2	I/O
6	IO_L35P_6	IO_L35P_6	N1	I/O
6	IO_L38N_6	IO_L38N_6	M6	I/O
6	IO_L38P_6	IO_L38P_6	M5	I/O
6	IO_L39N_6	IO_L39N_6	M4	I/O
6	IO_L39P_6	IO_L39P_6	M3	I/O
6	IO_L40N_6	IO_L40N_6	M2	I/O
6	IO_L40P_6/VREF_6	IO_L40P_6/VREF_6	M1	VREF
6	VCCO_6	VCCO_6	M7	VCCO
6	VCCO_6	VCCO_6	N7	VCCO
6	VCCO_6	VCCO_6	P7	VCCO
6	VCCO_6	VCCO_6	R3	VCCO
6	VCCO_6	VCCO_6	R6	VCCO
7	IO	IO	C2	I/O
7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	C3	DCI
7	IO_L01P_7/VRN_7	IO_L01P_7/VRN_7	C4	DCI
7	IO_L16N_7	IO_L16N_7	D1	I/O
7	IO_L16P_7/VREF_7	IO_L16P_7/VREF_7	C1	VREF
7	IO_L17N_7	IO_L17N_7	E4	I/O
7	IO_L17P_7	IO_L17P_7	D4	I/O
7	IO_L19N_7/VREF_7	IO_L19N_7/VREF_7	D3	VREF
7	IO_L19P_7	IO_L19P_7	D2	I/O
7	IO_L20N_7	IO_L20N_7	F4	I/O
7	IO_L20P_7	IO_L20P_7	E3	I/O
7	IO_L21N_7	IO_L21N_7	E1	I/O
7	IO_L21P_7	IO_L21P_7	E2	I/O
7	IO_L22N_7	IO_L22N_7	G6	I/O
7	IO_L22P_7	IO_L22P_7	F5	I/O

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
7	IO_L29P_7	IO_L29P_7	IO_L29P_7	IO_L29P_7	IO_L29P_7	L2	I/O
7	IO_L31N_7	IO_L31N_7	IO_L31N_7	IO_L31N_7	IO_L31N_7	M7	I/O
7	IO_L31P_7	IO_L31P_7	IO_L31P_7	IO_L31P_7	IO_L31P_7	M8	I/O
7	IO_L32N_7	IO_L32N_7	IO_L32N_7	IO_L32N_7	IO_L32N_7	M6	I/O
7	IO_L32P_7	IO_L32P_7	IO_L32P_7	IO_L32P_7	IO_L32P_7	M5	I/O
7	IO_L33N_7	IO_L33N_7	IO_L33N_7	IO_L33N_7	IO_L33N_7	M3	I/O
7	IO_L33P_7	IO_L33P_7	IO_L33P_7	IO_L33P_7	IO_L33P_7	L4	I/O
7	IO_L34N_7	IO_L34N_7	IO_L34N_7	IO_L34N_7	IO_L34N_7	M1	I/O
7	IO_L34P_7	IO_L34P_7	IO_L34P_7	IO_L34P_7	IO_L34P_7	M2	I/O
7	IO_L35N_7	IO_L35N_7	IO_L35N_7	IO_L35N_7	IO_L35N_7	N7	I/O
7	IO_L35P_7	IO_L35P_7	IO_L35P_7	IO_L35P_7	IO_L35P_7	N8	I/O
7	IO_L38N_7	IO_L38N_7	IO_L38N_7	IO_L38N_7	IO_L38N_7	N5	I/O
7	IO_L38P_7	IO_L38P_7	IO_L38P_7	IO_L38P_7	IO_L38P_7	N6	I/O
7	IO_L39N_7	IO_L39N_7	IO_L39N_7	IO_L39N_7	IO_L39N_7	N3	I/O
7	IO_L39P_7	IO_L39P_7	IO_L39P_7	IO_L39P_7	IO_L39P_7	N4	I/O
7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	N1	VREF
7	IO_L40P_7	IO_L40P_7	IO_L40P_7	IO_L40P_7	IO_L40P_7	N2	I/O
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	G3	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	J8	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	K8	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	L3	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	L9	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	M9	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	N9	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	N10	VCCO
N/A	GND	GND	GND	GND	GND	A1	GND
N/A	GND	GND	GND	GND	GND	A26	GND
N/A	GND	GND	GND	GND	GND	AC4	GND
N/A	GND	GND	GND	GND	GND	AC12	GND
N/A	GND	GND	GND	GND	GND	AC15	GND
N/A	GND	GND	GND	GND	GND	AC23	GND
N/A	GND	GND	GND	GND	GND	AD3	GND
N/A	GND	GND	GND	GND	GND	AD24	GND
N/A	GND	GND	GND	GND	GND	AE2	GND
N/A	GND	GND	GND	GND	GND	AE25	GND
N/A	GND	GND	GND	GND	GND	AF1	GND
N/A	GND	GND	GND	GND	GND	AF26	GND
N/A	GND	GND	GND	GND	GND	B2	GND
N/A	GND	GND	GND	GND	GND	B25	GND
N/A	GND	GND	GND	GND	GND	C3	GND
N/A	GND	GND	GND	GND	GND	C24	GND
N/A	GND	GND	GND	GND	GND	D4	GND
N/A	GND	GND	GND	GND	GND	D12	GND

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
N/A	GND	GND	GND	GND	GND	D15	GND
N/A	GND	GND	GND	GND	GND	D23	GND
N/A	GND	GND	GND	GND	GND	K11	GND
N/A	GND	GND	GND	GND	GND	K12	GND
N/A	GND	GND	GND	GND	GND	K15	GND
N/A	GND	GND	GND	GND	GND	K16	GND
N/A	GND	GND	GND	GND	GND	L10	GND
N/A	GND	GND	GND	GND	GND	L11	GND
N/A	GND	GND	GND	GND	GND	L12	GND
N/A	GND	GND	GND	GND	GND	L13	GND
N/A	GND	GND	GND	GND	GND	L14	GND
N/A	GND	GND	GND	GND	GND	L15	GND
N/A	GND	GND	GND	GND	GND	L16	GND
N/A	GND	GND	GND	GND	GND	L17	GND
N/A	GND	GND	GND	GND	GND	M4	GND
N/A	GND	GND	GND	GND	GND	M10	GND
N/A	GND	GND	GND	GND	GND	M11	GND
N/A	GND	GND	GND	GND	GND	M12	GND
N/A	GND	GND	GND	GND	GND	M13	GND
N/A	GND	GND	GND	GND	GND	M14	GND
N/A	GND	GND	GND	GND	GND	M15	GND
N/A	GND	GND	GND	GND	GND	M16	GND
N/A	GND	GND	GND	GND	GND	M17	GND
N/A	GND	GND	GND	GND	GND	M23	GND
N/A	GND	GND	GND	GND	GND	N11	GND
N/A	GND	GND	GND	GND	GND	N12	GND
N/A	GND	GND	GND	GND	GND	N13	GND
N/A	GND	GND	GND	GND	GND	N14	GND
N/A	GND	GND	GND	GND	GND	N15	GND
N/A	GND	GND	GND	GND	GND	N16	GND
N/A	GND	GND	GND	GND	GND	P11	GND
N/A	GND	GND	GND	GND	GND	P12	GND
N/A	GND	GND	GND	GND	GND	P13	GND
N/A	GND	GND	GND	GND	GND	P14	GND
N/A	GND	GND	GND	GND	GND	P15	GND
N/A	GND	GND	GND	GND	GND	P16	GND
N/A	GND	GND	GND	GND	GND	R4	GND
N/A	GND	GND	GND	GND	GND	R10	GND
N/A	GND	GND	GND	GND	GND	R11	GND
N/A	GND	GND	GND	GND	GND	R12	GND
N/A	GND	GND	GND	GND	GND	R13	GND
N/A	GND	GND	GND	GND	GND	R14	GND
N/A	GND	GND	GND	GND	GND	R15	GND

Right Half of Package (Top View)

Bank 1 (columns 14–23, top); Bank 2 (rows C–N, right); Bank 3 (rows P–AC, right); Bank 4 (bottom)

	14	15	16	17	18	19	20	21	22	23	24	25	26
A	I/O	I/O L29N_1	I/O L26N_1 ◆	I/O L23N_1 ◆	VCCAUX	I/O L15N_1	I/O L10N_1 VREF_1	I/O L08N_1	I/O	I/O	TMS	VCCAUX	GND
B	I/O L32N_1 GCLK5	I/O L29P_1	I/O L26P_1 ◆	I/O L23P_1 ◆	I/O L18N_1 ◆	I/O L15P_1	I/O L10P_1	I/O L08P_1	I/O L06N_1 VREF_1	I/O L04N_1	TCK	GND	VCCAUX
C	I/O L32P_1 GCLK4	I/O VREF_1	VCCO_1	I/O VREF_1	I/O L18P_1 ◆	I/O L12N_1 ◆	VCCO_1	I/O L07N_1	I/O L06P_1	I/O L04P_1	GND	I/O L01N_2 VRP_2	I/O L01P_2 VRN_2
D	I/O L31N_1 VREF_1	GND	I/O	I/O L22N_1	I/O VREF_1 ◆	I/O L12P_1 ◆	I/O L09N_1	I/O L07P_1	I/O L01N_1 VRP_1	GND	TDO	I/O L03N_2 VREF_2	I/O L03P_2
E	I/O L31P_1	I/O L28N_1	I/O L25N_1	I/O L22P_1	I/O	I/O L11N_1 ◆	I/O L09P_1	I/O L05N_1	I/O L01P_1 VRN_1	I/O L02N_2	I/O L02P_2	I/O L05N_2 ◆	I/O L05P_2 ◆
F	I/O	I/O L28P_1	I/O L25P_1	I/O L19N_1	I/O L16N_1	I/O L11P_1 ◆	I/O	I/O L05P_1	I/O ◆■	I/O L07N_2 ◆	I/O L07P_2 ◆	I/O L09N_2 VREF_2 ◆	I/O L09P_2 ◆
G	I/O L30N_1	I/O L27N_1	I/O L24N_1	I/O L19P_1	I/O L16P_1	I/O	I/O L06N_2 ◆	I/O L06P_2 ◆	I/O L08N_2 ◆	I/O L08P_2 ◆	VCCO_2	I/O L10N_2 ◆	I/O L10P_2 ◆
H	I/O L30P_1	I/O L27P_1	I/O L24P_1	VCCO_1	VCCO_1	VCCINT	I/O L14N_2 (L11N_2)	I/O L14P_2 (L11P_2)	I/O L16N_2 (L12N_2)	I/O L17N_2 (L13N_2)	I/O L17P_2 (L13P_2) VREF_2	I/O L19N_2	I/O L19P_2
J	VCCO_1	VCCO_1	VCCO_1	VCCINT	VCCINT	VCCO_2	I/O L20N_2	I/O L16P_2 (L12P_2)	I/O L21N_2	I/O L21P_2	I/O L22N_2	I/O L22P_2	VCCAUX
K	VCCO_1	GND	GND	VCCINT	VCCINT	VCCO_2	I/O L20P_2	I/O L23N_2 VREF_2	I/O L23P_2	I/O L24N_2	I/O L24P_2	I/O L26N_2	I/O L26P_2
L	GND	GND	GND	GND	VCCO_2	I/O L27N_2	I/O L27P_2	I/O L28N_2	I/O L28P_2	I/O L33N_2	VCCO_2	I/O L29N_2	I/O L29P_2
M	GND	GND	GND	GND	VCCO_2	I/O L31N_2	I/O L31P_2	I/O L32N_2	I/O L32P_2	GND	I/O L33P_2	I/O L34N_2 VREF_2	I/O L34P_2
N	GND	GND	GND	VCCO_2	VCCO_2	I/O L35N_2	I/O L35P_2	I/O L38N_2	I/O L38P_2	I/O L39N_2	I/O L39P_2	I/O L40N_2	I/O L40P_2 VREF_2
P	GND	GND	GND	VCCO_3	VCCO_3	I/O L35P_3	I/O L35N_3	I/O L38P_3	I/O L38N_3	I/O L39P_3	I/O L39N_3	I/O L40P_3	I/O L40N_3 VREF_3
R	GND	GND	GND	GND	VCCO_3	I/O L31P_3	I/O L31N_3	I/O L32P_3	I/O L32N_3	GND	I/O L33N_3	I/O L34P_3 VREF_3	I/O L34N_3
T	GND	GND	GND	GND	VCCO_3	I/O L27P_3	I/O L27N_3	I/O L28P_3	I/O L28N_3	I/O L33P_3	VCCO_3	I/O L29P_3	I/O L29N_3
U	VCCO_4	GND	GND	VCCINT	VCCINT	VCCO_3	I/O L20N_3	I/O L23P_3 VREF_3	I/O L23N_3	I/O L24P_3	I/O L24N_3	I/O L26P_3	I/O L26N_3
V	VCCO_4	VCCO_4	VCCO_4	VCCINT	VCCINT	VCCO_3	I/O L20P_3	I/O L16N_3	I/O L21P_3	I/O L21N_3	I/O L22P_3	I/O L22N_3	VCCAUX
W	I/O L27P_4 D1	I/O	I/O	VCCO_4	VCCO_4	VCCINT	I/O L10P_3 ◆	I/O L10N_3 ◆	I/O L16P_3	I/O L17P_3 VREF_3	I/O L17N_3	I/O L19P_3	I/O L19N_3
Y	I/O L30N_4 D2	I/O L27N_4 DIN D0	I/O L24N_4	I/O VREF_4	I/O L16N_4	I/O L11N_4 ◆	I/O L05P_3 ◆	I/O L05N_3 ◆	I/O L08P_3 ◆	I/O L08N_3 ◆	VCCO_3	I/O L14P_3	I/O L14N_3
AA	I/O L30P_4 D3	I/O L28N_4	I/O L24P_4	I/O L19P_4	I/O L16P_4	I/O L11P_4 ◆	I/O	I/O L01P_3 VRN_3	I/O L01N_3 VRP_3	I/O L07P_3 ◆	I/O L07N_3 ◆	I/O L09P_3 VREF_3 ◆	I/O L09N_3 ◆
AB	IO VREF_4	I/O L28P_4	I/O L25N_4	I/O L22P_4	I/O L17N_4 ◆	I/O L12N_4 ◆	I/O L09N_4	I/O L07N_4	I/O L01N_4 VRP_4	I/O L02P_3	I/O L02N_3 VREF_3	I/O L06P_3 ◆	I/O L06N_3 ◆
AC	I/O L31N_4 INIT_B	GND	I/O L25P_4	I/O L19N_4	I/O L17P_4 ◆	I/O L12P_4 ◆	I/O L09P_4	I/O L07P_4	I/O L01P_4 VRN_4	GND	DONE	I/O L03P_3	I/O L03N_3
AD	I/O L31P_4 DOUT BUSY	I/O	VCCO_4	I/O L22N_4 VREF_4	I/O L18N_4 ◆	I/O ◆	VCCO_4	I/O L08N_4	I/O L06N_4 VREF_4	I/O	GND	I/O VREF_4	CCLK
AE	I/O L32N_4 GCLK1	I/O L29N_4	I/O L26N_4 ◆	I/O L23N_4 ◆	I/O L18P_4 ◆	I/O L15N_4	I/O L10N_4	I/O L08P_4	I/O L06P_4	I/O L05N_4	I/O L04N_4	GND	VCCAUX
AF	I/O L32P_4 GCLK0	I/O L29P_4	I/O L26P_4 VREF_4 ◆	I/O L23P_4 ◆	VCCAUX	I/O L15P_4	I/O L10P_4	I/O	I/O	I/O L05P_4	I/O L04P_4	VCCAUX	GND

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Notes:

1. Differential pair assignments shown in parentheses on balls H20, H21, H22, H23, H24, and J21 are for XC3S4000 only.
2. Differential pair assignments for the XC3S5000 are different on 15 balls (see Table 103 for details.)

Figure 54: FG676 Package Footprint (Top View) Continued

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
1	IO_L05P_1	IO_L05P_1	F25	I/O
1	IO_L06N_1/VREF_1	IO_L06N_1/VREF_1	C24	VREF
1	IO_L06P_1	IO_L06P_1	D24	I/O
1	IO_L07N_1	IO_L07N_1	A24	I/O
1	IO_L07P_1	IO_L07P_1	B24	I/O
1	IO_L08N_1	IO_L08N_1	H23	I/O
1	IO_L08P_1	IO_L08P_1	G24	I/O
1	IO_L09N_1	IO_L09N_1	F23	I/O
1	IO_L09P_1	IO_L09P_1	G23	I/O
1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	C23	VREF
1	IO_L10P_1	IO_L10P_1	D23	I/O
1	IO_L11N_1	IO_L11N_1	A23	I/O
1	IO_L11P_1	IO_L11P_1	B23	I/O
1	IO_L12N_1	IO_L12N_1	H22	I/O
1	IO_L12P_1	IO_L12P_1	J22	I/O
1	IO_L13N_1	IO_L13N_1	F22	I/O
1	IO_L13P_1	IO_L13P_1	E23	I/O
1	IO_L14N_1	IO_L14N_1	D22	I/O
1	IO_L14P_1	IO_L14P_1	E22	I/O
1	IO_L15N_1	IO_L15N_1	A22	I/O
1	IO_L15P_1	IO_L15P_1	B22	I/O
1	IO_L16N_1	IO_L16N_1	F21	I/O
1	IO_L16P_1	IO_L16P_1	G21	I/O
1	IO_L17N_1/VREF_1	IO_L17N_1/VREF_1	B21	VREF
1	IO_L17P_1	IO_L17P_1	C21	I/O
1	IO_L18N_1	IO_L18N_1	G20	I/O
1	IO_L18P_1	IO_L18P_1	H20	I/O
1	IO_L19N_1	IO_L19N_1	E20	I/O
1	IO_L19P_1	IO_L19P_1	F20	I/O
1	IO_L20N_1	IO_L20N_1	C20	I/O
1	IO_L20P_1	IO_L20P_1	D20	I/O
1	IO_L21N_1	IO_L21N_1	A20	I/O
1	IO_L21P_1	IO_L21P_1	B20	I/O
1	IO_L22N_1	IO_L22N_1	J19	I/O
1	IO_L22P_1	IO_L22P_1	K19	I/O
1	IO_L23N_1	IO_L23N_1	G19	I/O
1	IO_L23P_1	IO_L23P_1	H19	I/O
1	IO_L24N_1	IO_L24N_1	E19	I/O
1	IO_L24P_1	IO_L24P_1	F19	I/O
1	IO_L25N_1	IO_L25N_1	C19	I/O