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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	192
Number of Logic Elements/Cells	1728
Total RAM Bits	73728
Number of I/O	63
Number of Gates	50000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s50-4vq100i

According to Figure 7, the clock line OTCLK1 connects the CK inputs of the upper registers on the output and three-state paths. Similarly, OTCLK2 connects the CK inputs for the lower registers on the output and three-state paths. The upper and lower registers on the input path have independent clock lines: ICLK1 and ICLK2. The enable line OCE connects the CE inputs of the upper and lower registers on the output path. Similarly, TCE connects the CE inputs for the register pair on the three-state path and ICE does the same for the register pair on the input path. The Set/Reset (SR) line entering the IOB is common to all six registers, as is the Reverse (REV) line.

Each storage element supports numerous options in addition to the control over signal polarity described in the IOB Overview section. These are described in Table 6.

Table 6: **Storage Element Options**

Option Switch	Function	Specificity
FF/Latch	Chooses between an edge-sensitive flip-flop or a level-sensitive latch	Independent for each storage element.
SYNC/ASYNC	Determines whether SR is synchronous or asynchronous	Independent for each storage element.
SRHIGH/SRLOW	Determines whether SR acts as a Set, which forces the storage element to a logic "1" (SRHIGH) or a Reset, which forces a logic "0" (SRLOW).	Independent for each storage element, except when using FDDR. In the latter case, the selection for the upper element (OFF1 or TFF2) applies to both elements.
INIT1/INIT0	In the event of a Global Set/Reset, after configuration or upon activation of the GSR net, this switch decides whether to set or reset a storage element. By default, choosing SRLOW also selects INIT0; choosing SRHIGH also selects INIT1.	Independent for each storage element, except when using FDDR. In the latter case, selecting INIT0 for one element applies to both elements (even though INIT1 is selected for the other).

Double-Data-Rate Transmission

Double-Data-Rate (DDR) transmission describes the technique of synchronizing signals to both the rising and falling edges of the clock signal. Spartan-3 devices use register-pairs in all three IOB paths to perform DDR operations.

The pair of storage elements on the IOB's Output path (OFF1 and OFF2), used as registers, combine with a special multiplexer to form a DDR D-type flip-flop (FDDR). This primitive permits DDR transmission where output data bits are synchronized to both the rising and falling edges of a clock. It is possible to access this function by placing either an FDDRRSE or an FDDRCPE component or symbol into the design. DDR operation requires two clock signals (50% duty cycle), one the inverted form of the other. These signals trigger the two registers in alternating fashion, as shown in Figure 8. Commonly, the Digital Clock Manager (DCM) generates the two clock signals by mirroring an incoming signal, then shifting it 180 degrees. This approach ensures minimal skew between the two signals.

The storage-element-pair on the Three-State path (TFF1 and TFF2) can also be combined with a local multiplexer to form an FDDR primitive. This permits synchronizing the output enable to both the rising and falling edges of a clock. This DDR operation is realized in the same way as for the output path.

The storage-element-pair on the input path (IFF1 and IFF2) allows an I/O to receive a DDR signal. An incoming DDR clock signal triggers one register and the inverted clock signal triggers the other register. In this way, the registers take turns capturing bits of the incoming DDR data signal.

Arrangement of RAM Blocks on Die

The XC3S50 has one column of block RAM. The Spartan-3 devices ranging from the XC3S200 to XC3S2000 have two columns of block RAM. The XC3S4000 and XC3S5000 have four columns. The position of the columns on the die is shown in Figure 1, page 3. For a given device, the total available RAM blocks are distributed equally among the columns. Table 12 shows the number of RAM blocks, the data storage capacity, and the number of columns for each device.

Table 12: **Number of RAM Blocks by Device**

Device	Total Number of RAM Blocks	Total Addressable Locations (Bits)	Number of Columns
XC3S50	4	73,728	1
XC3S200	12	221,184	2
XC3S400	16	294,912	2
XC3S1000	24	442,368	2
XC3S1500	32	589,824	2
XC3S2000	40	737,280	2
XC3S4000	96	1,769,472	4
XC3S5000	104	1,916,928	4

Block RAM and multipliers have interconnects between them that permit simultaneous operation; however, since the multiplier shares inputs with the upper data bits of block RAM, the maximum data path width of the block RAM is 18 bits in this case.

The Internal Structure of the Block RAM

The block RAM has a dual port structure. The two identical data ports called A and B permit independent access to the common RAM block, which has a maximum capacity of 18,432 bits—or 16,384 bits when no parity lines are used. Each port has its own dedicated set of data, control and clock lines for synchronous read and write operations. There are four basic data paths, as shown in Figure 13: (1) write to and read from Port A, (2) write to and read from Port B, (3) data transfer from Port A to Port B, and (4) data transfer from Port B to Port A.

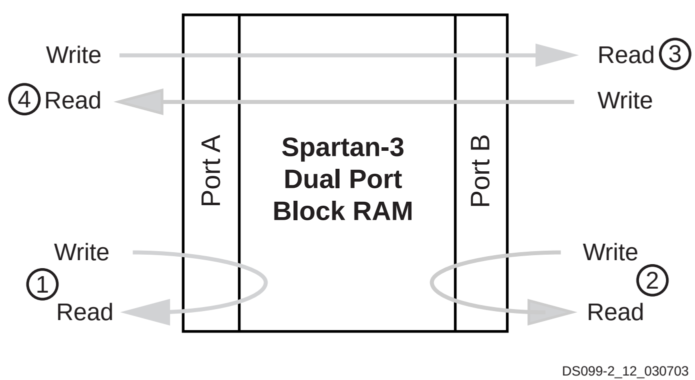


Figure 13: **Block RAM Data Paths**

Block RAM Port Signal Definitions

Representations of the dual-port primitive RAMB16_S[w_A]_S[w_B] and the single-port primitive RAMB16_S[w] with their associated signals are shown in Figure 14. These signals are defined in Table 13.

Each BUFGMUX element, shown in Figure 24, is a 2-to-1 multiplexer that can receive signals from any of the four following sources:

- One of the four Global Clock inputs on the same side of the die—top or bottom—as the BUFGMUX element in use.
- Any of four nearby horizontal Double lines.
- Any of four outputs from the DCM in the right-hand quadrant that is on the same side of the die as the BUFGMUX element in use.
- Any of four outputs from the DCM in the left-hand quadrant that is on the same side of the die as the BUFGMUX element in use.

The multiplexer select line, S, chooses which of the two inputs, I0 or I1, drives the BUFGMUX's output signal, O, as described in Table 25. The switching from one clock to the other is glitchless, and done in such a way that the output High and Low times are never shorter than the shortest High or Low time of either input clock.

Table 25: **BUFGMUX Select Mechanism**

S Input	O Output
0	I0 Input
1	I1 Input

The two clock inputs can be asynchronous with regard to each other, and the S input can change at any time, except for a short setup time prior to the rising edge of the presently selected clock (I0 or I1). Violating this setup time requirement can result in an undefined runt pulse output.

The BUFG clock buffer primitive drives a single clock signal onto the clock network and is essentially the same element as a BUFGMUX, just without the clock select mechanism. Similarly, the BUFGCE primitive creates an enabled clock buffer using the BUFGMUX select mechanism.

Each BUFGMUX buffers incoming clock signals to two possible destinations:

- The vertical spine belonging to the same side of the die—top or bottom—as the BUFGMUX element in use. The two spines—top and bottom—each comprise four vertical clock lines, each running from one of the BUFGMUX elements on the same side towards the center of the die. At the center of the die, clock signals reach the eight-line horizontal spine, which spans the width of the die. In turn, the horizontal spine branches out into a subsidiary clock interconnect that accesses the CLBs.
- The clock input of either DCM on the same side of the die—top or bottom—as the BUFGMUX element in use.

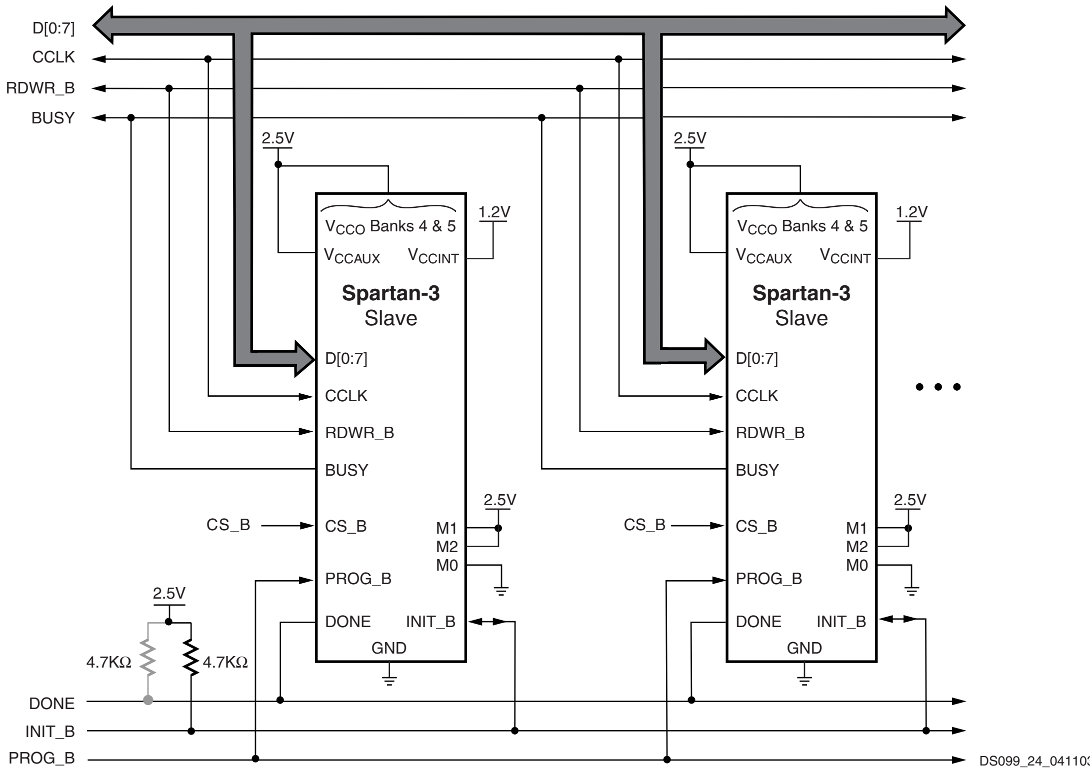
Use either a BUFGMUX element or a BUFG (Global Clock Buffer) element to place a Global input in the design. For the purpose of minimizing the dynamic power dissipation of the clock network, the Xilinx development software automatically disables all clock line segments that a design does not use.

A global clock line ideally drives clock inputs on the various clocked elements within the FPGA, such as CLB or IOB flip-flops or block RAMs. A global clock line also optionally drives combinatorial inputs. However, doing so provides additional loading on the clock line that might also affect clock jitter. Ideally, drive combinatorial inputs using the signal that also drives the input to the BUFGMUX or BUFG element.

For more details, refer to the chapter entitled "Using Global Clock Resources" in UG331.

(e.g. all configuration pins taken together) when operating in the User mode. This is accomplished by setting the *Persist* option to *Yes*.

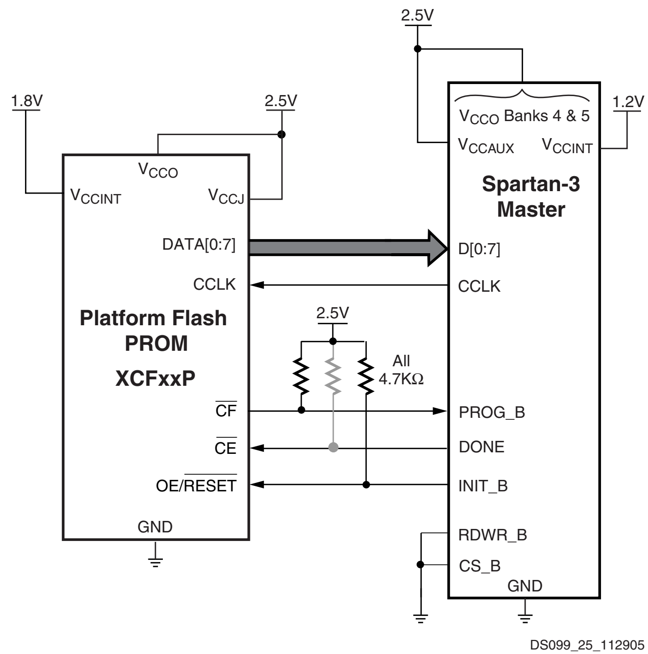
Multiple FPGAs can be configured using the Slave Parallel mode and can be made to start-up simultaneously. Figure 27 shows the device connections. To configure multiple devices in this way, wire the individual CCLK, Data, RDWR_B, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by deasserting the CS_B pin of each device in turn and writing the appropriate data.



Notes:

1. There are two ways to use the DONE line. First, one may set the BitGen option DriveDone to "Yes" only for the last FPGA to be configured in the chain shown above (or for the single FPGA as may be the case). This enables the DONE pin to drive High; thus, no pull-up resistor is necessary. DriveDone is set to "No" for the remaining FPGAs in the chain. Second, DriveDone can be set to "No" for all FPGAs. Then all DONE lines are open-drain and require the pull-up resistor shown in grey. In most cases, a value between 3.3KΩ to 4.7KΩ is sufficient. However, when using DONE synchronously with a long chain of FPGAs, cumulative capacitance may necessitate lower resistor values (e.g. down to 330Ω) in order to ensure a rise time within one clock cycle.
2. If the FPGAs use different configuration data files, configure them in sequence by first asserting the CS_B of one FPGA then asserting the CS_B of the other FPGA.
3. For information on how to program the FPGA using 3.3V signals and power, see 3.3V-Tolerant Configuration Interface.

Figure 27: **Connection Diagram for Slave Parallel Configuration**



Notes:

1. There are two ways to use the DONE line. First, one may set the BitGen option DriveDone to "Yes" only for the last FPGA to be configured in the chain shown above (or for the single FPGA as may be the case). This enables the DONE pin to drive High; thus, no pull-up resistor is necessary. DriveDone is set to "No" for the remaining FPGAs in the chain. Second, DriveDone can be set to "No" for all FPGAs. Then all DONE lines are open-drain and require the pull-up resistor shown in grey. In most cases, a value between 3.3KΩ to 4.7KΩ is sufficient. However, when using DONE synchronously with a long chain of FPGAs, cumulative capacitance may necessitate lower resistor values (e.g. down to 330Ω) in order to ensure a rise time within one clock cycle.

Figure 28: **Connection Diagram for Master Parallel Configuration**

Master Parallel Mode

In this mode, the FPGA configures from byte-wide data, and the FPGA supplies the CCLK configuration clock. In Master configuration modes, CCLK behaves as a bidirectional I/O pin. Timing is similar to the Slave Parallel mode except that CCLK is supplied by the FPGA. The device connections are shown in Figure 28.

Boundary-Scan (JTAG) Mode

In Boundary-Scan mode, dedicated pins are used for configuring the FPGA. The configuration is done entirely through the IEEE 1149.1 Test Access Port (TAP). FPGA configuration using the Boundary-Scan mode is compatible with the IEEE Std 1149.1-1993 standard and IEEE Std 1532 for In-System Configurable (ISC) devices.

Configuration through the boundary-scan port is always available, regardless of the selected configuration mode. In some cases, however, the mode pin setting may affect proper programming of the device due to various interactions. For example, if the mode pins are set to Master Serial or Master Parallel mode, and the associated PROM is already programmed with a valid configuration image, then there is potential for configuration interference between the JTAG and PROM data. Selecting the Boundary-Scan mode disables the other modes and is the most reliable mode when programming via JTAG.

Configuration Sequence

The configuration of Spartan-3 devices is a three-stage process that occurs after Power-On Reset or the assertion of PROG_B. POR occurs after the V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 4 supplies have reached their respective maximum input threshold levels (see Table 29, page 59). After POR, the three-stage process begins.

First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process. A flow diagram for the configuration sequence of the Serial and Parallel modes is shown in Figure 29. The flow diagram for the Boundary-Scan configuration sequence appears in Figure 30.

Table 34: **Quiescent Supply Current Characteristics**

Symbol	Description	Device	Typical[1]	Commercial Maximum[1]	Industrial Maximum[1]	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC3S50	5	24	31	mA
		XC3S200	10	54	80	mA
		XC3S400	15	110	157	mA
		XC3S1000	35	160	262	mA
		XC3S1500	45	260	332	mA
		XC3S2000	60	360	470	mA
		XC3S4000	100	450	810	mA
		XC3S5000	120	600	870	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC3S50	1.5	2.0	2.5	mA
		XC3S200	1.5	3.0	3.5	mA
		XC3S400	1.5	3.0	3.5	mA
		XC3S1000	2.0	4.0	5.0	mA
		XC3S1500	2.5	4.0	5.0	mA
		XC3S2000	3.0	5.0	6.0	mA
		XC3S4000	3.5	5.0	6.0	mA
		XC3S5000	3.5	5.0	6.0	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC3S50	7	20	22	mA
		XC3S200	10	30	33	mA
		XC3S400	15	40	44	mA
		XC3S1000	20	50	55	mA
		XC3S1500	35	75	85	mA
		XC3S2000	45	90	100	mA
		XC3S4000	55	110	125	mA
		XC3S5000	70	130	145	mA

Notes:

1. The numbers in this table are based on the conditions set forth in Table 32. Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. Typical values are characterized using devices with typical processing at room temperature (T_J of 25°C at V_{CCINT} = 1.2V, V_{CCO} = 3.3V, and V_{CCAUX} = 2.5V). Maximum values are the production test limits measured for each device at the maximum specified junction temperature and at maximum voltage limits with V_{CCINT} = 1.26V, V_{CCO} = 3.465V, and V_{CCAUX} = 2.625V. The FPGA is programmed with a "blank" configuration data file (i.e., a design with no functional elements instantiated). For conditions other than those described above, (e.g., a design including functional elements, the use of DCI standards, etc.), measured quiescent current levels may be different than the values in the table. Use the XPower Estimator or XPower Analyzer for more accurate estimates. See Note 2.
2. There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The Spartan-3 XPower Estimator provides quick, approximate, typical estimates, and does not require a netlist of the design. b) XPower Analyzer, part of the Xilinx ISE development software, uses the FPGA netlist as input to provide more accurate maximum and typical estimates.
3. The maximum numbers in this table also indicate the minimum current each power rail requires in order for the FPGA to power-on successfully, once all three rails are supplied. If V_{CCINT} is applied before V_{CCAUX}, there may be temporary additional I_{CCINT} current until V_{CCAUX} is applied. See Surplus I_{CCINT} if V_{CCINT} Applied before V_{CCAUX}, page 54

Table 42: **Setup and Hold Times for the IOB Input Path *(Cont'd)***

Symbol	Description	Conditions	Device	Speed Grade -5 Min	Speed Grade -4 Min	Units
Hold Times						
T_{IOICKP}	Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. No Input Delay is programmed.	LVCMOS25[(3)], IOBDELAY = NONE	XC3S50	-0.55	-0.55	ns
			XC3S200	-0.29	-0.29	ns
			XC3S400	-0.29	-0.29	ns
			XC3S1000	-0.55	-0.55	ns
			XC3S1500	-0.55	-0.55	ns
			XC3S2000	-0.55	-0.55	ns
			XC3S4000	-0.61	-0.61	ns
			XC3S5000	-0.68	-0.68	ns
$T_{IOICKPD}$	Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. The Input Delay is programmed.	LVCMOS25[(3)], IOBDELAY = IFD	XC3S50	-2.74	-2.74	ns
			XC3S200	-3.00	-3.00	ns
			XC3S400	-2.90	-2.90	ns
			XC3S1000	-3.24	-3.24	ns
			XC3S1500	-3.55	-3.55	ns
			XC3S2000	-4.57	-4.57	ns
			XC3S4000	-4.96	-4.96	ns
			XC3S5000	-5.09	-5.09	ns
Set/Reset Pulse Width						
T_{RPW_IOB}	Minimum pulse width to SR control input on IOB		All	0.66	0.76	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32 and Table 35.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, add the appropriate Input adjustment from Table 44.
3. These hold times require adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, subtract the appropriate Input adjustment from Table 44. When the hold time is negative, it is possible to change the data before the clock's active edge.

Internal Logic Timing

Table 51: **CLB Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{CKO}	When reading from the FFX (FFY) Flip-Flop, the time from the active transition at the CLK input to data appearing at the XQ (YQ) output	–	0.63	–	0.72	ns
Setup Times						
T_{AS}	Time from the setup of data at the F or G input to the active transition at the CLK input of the CLB	0.46	–	0.53	–	ns
T_{DICK}	Time from the setup of data at the BX or BY input to the active transition at the CLK input of the CLB	1.27	–	1.57	–	ns
Hold Times						
T_{AH}	Time from the active transition at the CLK input to the point where data is last held at the F or G input	0	–	0	–	ns
T_{CKDI}	Time from the active transition at the CLK input to the point where data is last held at the BX or BY input	0.25	–	0.29	–	ns
Clock Timing						
T_{CH}	CLB CLK signal High pulse width	0.69	∞	0.79	∞	ns
T_{CL}	CLB CLK signal Low pulse width	0.69	∞	0.79	∞	ns
F_{TOG}	Maximum toggle frequency (for export control)	–	725	–	630	MHz
Propagation Times						
T_{ILO}	The time it takes for data to travel from the CLB's F (G) input to the X (Y) output	–	0.53	–	0.61	ns
Set/Reset Pulse Width						
T_{RPW_CLB}	The minimum allowable pulse width, High or Low, to the CLB's SR input	0.76	–	0.87	–	ns

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 32.
2. The timing shown is for SLICEM.
3. For minimums, use the values reported by the Xilinx timing analyzer.

Miscellaneous DCM Timing

Table 64: **Miscellaneous DCM Timing**

Symbol	Description	DLL Frequency Mode	Temperature Range		Units
			Commercial	Industrial	
DCM_INPUT_CLOCK_STOP	Maximum duration that the CLKIN and CLKFB signals can be stopped[1,2]	Any	100	100	ms
DCM_RST_PW_MIN	Minimum duration of a RST pulse width	Any	3	3	CLKIN cycles
DCM_RST_PW_MAX[3]	Maximum duration of a RST pulse width[1,2]	Low	N/A	N/A	seconds
		High	N/A	10	seconds
DCM_CONFIG_LAG_TIME[4]	Maximum duration from V_{CCINT} applied to FPGA configuration successfully completed (DONE pin goes High) and clocks applied to DCM DLL[1,2]	Low	N/A	N/A	minutes
		High	N/A	10	minutes

Notes:

1. These limits only apply to applications that use the DCM DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV). The DCM DFS outputs (CLKFX, CLKFX180) are unaffected. Required due to effects of device cooling: see “Momentarily Stopping CLKIN” in Chapter 3 of UG331.
2. Industrial-temperature applications that use the DLL in High-Frequency mode must use a continuous or increasing operating frequency. The DLL under these conditions does not support reducing the operating frequency once establishing an initial operating frequency.
3. This specification is equivalent to the Virtex-4 FPGA DCM_RESET specification.
4. This specification is equivalent to the Virtex-4 FPGA TCONFIG specification.

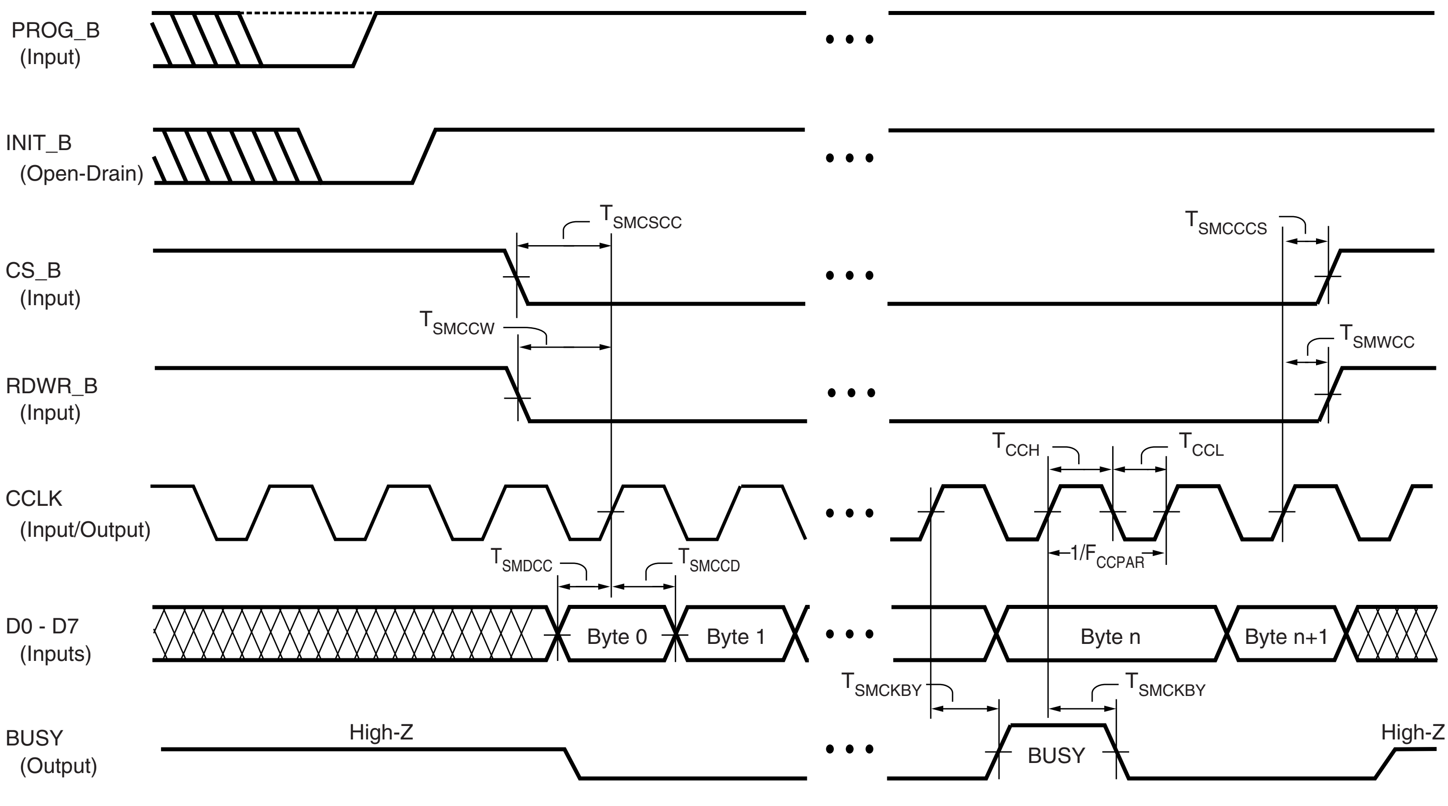


Figure 38: **Waveforms for Master and Slave Parallel Configuration**

Table 67: **Timing for the Master and Slave Parallel Configuration Modes**

Symbol	Description	Slave/ Master	All Speed Grades		Units
			Min	Max	
Clock-to-Output Times					
T_{SMCKBY}	The time from the rising transition on the CCLK pin to a signal transition at the BUSY pin	Slave	–	12.0	ns
Setup Times					
T_{SMDCC}	The time from the setup of data at the D0-D7 pins to the rising transition at the CCLK pin	Both	10.0	–	ns
T_{SMCSCC}	The time from the setup of a logic level at the CS_B pin to the rising transition at the CCLK pin		10.0	–	ns
T_{SMCCW}(3)	The time from the setup of a logic level at the RDWR_B pin to the rising transition at the CCLK pin		10.0	–	ns
Hold Times					
T_{SMCCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the D0-D7 pins	Both	0	–	ns
T_{SMCCCS}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the CS_B pin		0	–	ns
T_{SMWCC}(3)	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the RDWR_B pin		0	–	ns

Spartan-3 FPGA Family: Pinout Descriptions

DS099 (v3.0) October 29, 2012 **Product Specification**

Introduction

This data sheet module describes the various pins on a Spartan®-3 FPGA and how they connect to the supported component packages.

- The Pin Types section categorizes all of the FPGA pins by their function type.
- The Pin Definitions section provides a top-level description for each pin on the device.
- The Detailed, Functional Pin Descriptions section offers significantly more detail about each pin, especially for the dual- or special-function pins used during device configuration.
- Some pins have associated behavior that is controlled by settings in the configuration bitstream. These options are described in the Bitstream Options section.
- The Package Overview section describes the various packaging options available for Spartan-3 FPGAs. Detailed pin list tables and footprint diagrams are provided for each package solution.

Pin Descriptions

Pin Types

A majority of the pins on a Spartan-3 FPGA are general-purpose, user-defined I/O pins. There are, however, up to 12 different functional types of pins on Spartan-3 device packages, as outlined in Table 69. In the package footprint drawings that follow, the individual pins are color-coded according to pin type as in the table.

Table 69: **Types of Pins on Spartan-3 FPGAs**

Pin Type/ Color Code	Description	Pin Name
I/O	Unrestricted, general-purpose user-I/O pin. Most pins can be paired together to form differential I/Os.	IO, IO_Lxxy_#
DUAL	Dual-purpose pin used in some configuration modes during the configuration process and then usually available as a user I/O after configuration. If the pin is not used during configuration, this pin behaves as an I/O-type pin. There are 12 dual-purpose configuration pins on every package. The INIT_B pin has an internal pull-up resistor to VCCO_4 or VCCO_BOTTOM during configuration.	IO_Lxxy_#/DIN/D0, IO_Lxxy_#/D1, IO_Lxxy_#/D2, IO_Lxxy_#/D3, IO_Lxxy_#/D4, IO_Lxxy_#/D5, IO_Lxxy_#/D6, IO_Lxxy_#/D7, IO_Lxxy_#/CS_B, IO_Lxxy_#/RDWR_B, IO_Lxxy_#/BUSY/DOUT, IO_Lxxy_#/INIT_B
CONFIG	Dedicated configuration pin. Not available as a user-I/O pin. Every package has seven dedicated configuration pins. These pins are powered by VCCAUX and have a dedicated internal pull-up resistor to VCCAUX during configuration.	CCLK, DONE, M2, M1, M0, PROG_B, HSWAP_EN
JTAG	Dedicated JTAG pin. Not available as a user-I/O pin. Every package has four dedicated JTAG pins. These pins are powered by VCCAUX and have a dedicated internal pull-up resistor to VCCAUX during configuration.	TDI, TMS, TCK, TDO
DCI	Dual-purpose pin that is either a user-I/O pin or used to calibrate output buffer impedance for a specific bank using Digital Controlled Impedance (DCI). There are two DCI pins per I/O bank.	IO/VRN_# IO_Lxxy_#/VRN_# IO/VRP_# IO_Lxxy_#/VRP_#

Table 91: **TQ144 Package Pinout *(Cont'd)***

Bank	XC3S50, XC3S200, XC3S400 Pin Name	TQ144 Pin Number	Type
2	IO_L23N_2/VREF_2	P98	VREF
2	IO_L23P_2	P97	I/O
2	IO_L24N_2	P96	I/O
2	IO_L24P_2	P95	I/O
2	IO_L40N_2	P93	I/O
2	IO_L40P_2/VREF_2	P92	VREF
3	IO	P76	I/O
3	IO_L01N_3/VRP_3	P74	DCI
3	IO_L01P_3/VRN_3	P73	DCI
3	IO_L20N_3	P78	I/O
3	IO_L20P_3	P77	I/O
3	IO_L21N_3	P80	I/O
3	IO_L21P_3	P79	I/O
3	IO_L22N_3	P83	I/O
3	IO_L22P_3	P82	I/O
3	IO_L23N_3	P85	I/O
3	IO_L23P_3/VREF_3	P84	VREF
3	IO_L24N_3	P87	I/O
3	IO_L24P_3	P86	I/O
3	IO_L40N_3/VREF_3	P90	VREF
3	IO_L40P_3	P89	I/O
4	IO/VREF_4	P70	VREF
4	IO_L01N_4/VRP_4	P69	DCI
4	IO_L01P_4/VRN_4	P68	DCI
4	IO_L27N_4/DIN/D0	P65	DUAL
4	IO_L27P_4/D1	P63	DUAL
4	IO_L30N_4/D2	P60	DUAL
4	IO_L30P_4/D3	P59	DUAL
4	IO_L31N_4/INIT_B	P58	DUAL
4	IO_L31P_4/DOUT/BUSY	P57	DUAL
4	IO_L32N_4/GCLK1	P56	GCLK
4	IO_L32P_4/GCLK0	P55	GCLK
5	IO/VREF_5	P44	VREF
5	IO_L01N_5/RDWR_B	P41	DUAL
5	IO_L01P_5/CS_B	P40	DUAL
5	IO_L28N_5/D6	P47	DUAL
5	IO_L28P_5/D7	P46	DUAL
5	IO_L31N_5/D4	P51	DUAL
5	IO_L31P_5/D5	P50	DUAL
5	IO_L32N_5/GCLK3	P53	GCLK

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
4	IO_L31P_4/ DOUT/BUSY	V10	DUAL
4	IO_L32N_4/GCLK1	N10	GCLK
4	IO_L32P_4/GCLK0	P10	GCLK
4	VCCO_4	M10	VCCO
4	VCCO_4	M11	VCCO
4	VCCO_4	T13	VCCO
4	VCCO_4	U11	VCCO
5	IO	N8	I/O
5	IO	P8	I/O
5	IO	U6	I/O
5	IO/VREF_5	R9	VREF
5	IO_L01N_5/RDWR_B	V3	DUAL
5	IO_L01P_5/CS_B	V2	DUAL
5	IO_L06N_5	T5	I/O
5	IO_L06P_5	T4	I/O
5	IO_L10N_5/VRP_5	V4	DCI
5	IO_L10P_5/VRN_5	U4	DCI
5	IO_L15N_5	R6	I/O
5	IO_L15P_5	R5	I/O
5	IO_L16N_5	V5	I/O
5	IO_L16P_5	U5	I/O
5	IO_L27N_5/VREF_5	P6	VREF
5	IO_L27P_5	P7	I/O
5	IO_L28N_5/D6	R7	DUAL
5	IO_L28P_5/D7	T7	DUAL
5	IO_L29N_5	V8	I/O
5	IO_L29P_5/VREF_5	V7	VREF
5	IO_L30N_5	R8	I/O
5	IO_L30P_5	T8	I/O
5	IO_L31N_5/D4	U9	DUAL
5	IO_L31P_5/D5	V9	DUAL
5	IO_L32N_5/GCLK3	N9	GCLK
5	IO_L32P_5/GCLK2	P9	GCLK
5	VCCO_5	M8	VCCO
5	VCCO_5	M9	VCCO
5	VCCO_5	T6	VCCO
5	VCCO_5	U8	VCCO
6	IO	K6	I/O
6	IO_L01N_6/VRP_6	T3	DCI

FG676: 676-lead Fine-pitch Ball Grid Array

The 676-lead fine-pitch ball grid array package, FG676, supports five different Spartan-3 devices, including the XC3S1000, XC3S1500, XC3S2000, XC3S4000, and XC3S5000. All five have nearly identical footprints but are slightly different, primarily due to unconnected pins on the XC3S1000 and XC3S1500. For example, because the XC3S1000 has fewer I/O pins, this device has 98 unconnected pins on the FG676 package, labeled as "N.C." In Table 103 and Figure 53, these unconnected pins are indicated with a black diamond symbol (◆). The XC3S1500, however, has only two unconnected pins, also labeled "N.C." in the pinout table but indicated with a black square symbol (■).

All the package pins appear in Table 103 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

If there is a difference between the XC3S1000, XC3S1500, XC3S2000, XC3S4000, and XC3S5000 pinouts, then that difference is highlighted in Table 103. If the table entry is shaded grey, then there is an unconnected pin on either the XC3S1000 or XC3S1500 that maps to a user-I/O pin on the XC3S2000, XC3S4000, and XC3S5000. If the table entry is shaded tan, then the unconnected pin on either the XC3S1000 or XC3S1500 maps to a VREF-type pin on the XC3S2000, XC3S4000, and XC3S5000. If the other VREF pins in the bank all connect to a voltage reference to support a special I/O standard, then also connect the N.C. pin on the XC3S1000 or XC3S1500 to the same VREF voltage. This provides maximum flexibility as you could potentially migrate a design from the XC3S1000 through to the XC3S5000 FPGA without changing the printed circuit board.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

Pinout Table

Table 103: **FG676 Package Pinout**

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
0	IO	IO	IO	IO	IO_L04N_0(3)	A3	I/O
0	IO	IO	IO	IO	IO	A5	I/O
0	IO	IO	IO	IO	IO	A6	I/O
0	IO	IO	IO	IO	IO_L04P_0(3)	C4	I/O
0	N.C. (◆)	IO	IO	IO	IO_L13N_0(3)	C8	I/O
0	IO	IO	IO	IO	IO	C12	I/O
0	IO	IO	IO	IO	IO	E13	I/O
0	IO	IO	IO	IO	IO	H11	I/O
0	IO	IO	IO	IO	IO	H12	I/O
0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	B3	VREF
0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	F7	VREF
0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	G10	VREF
0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	E5	DCI
0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	D5	DCI
0	IO_L05N_0	IO_L05N_0	IO_L05N_0	IO_L05N_0	IO_L05N_0	B4	I/O
0	IO_L05P_0/VREF_0	IO_L05P_0/VREF_0	IO_L05P_0/VREF_0	IO_L05P_0/VREF_0	IO_L05P_0/VREF_0	A4	VREF
0	IO_L06N_0	IO_L06N_0	IO_L06N_0	IO_L06N_0	IO_L06N_0	C5	I/O
0	IO_L06P_0	IO_L06P_0	IO_L06P_0	IO_L06P_0	IO_L06P_0	B5	I/O
0	IO_L07N_0	IO_L07N_0	IO_L07N_0	IO_L07N_0	IO_L07N_0	E6	I/O
0	IO_L07P_0	IO_L07P_0	IO_L07P_0	IO_L07P_0	IO_L07P_0	D6	I/O
0	IO_L08N_0	IO_L08N_0	IO_L08N_0	IO_L08N_0	IO_L08N_0	C6	I/O
0	IO_L08P_0	IO_L08P_0	IO_L08P_0	IO_L08P_0	IO_L08P_0	B6	I/O

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
2	N.C. (◆)	IO_L06N_2	IO_L06N_2	IO_L06N_2	IO_L06N_2	G20	I/O
2	N.C. (◆)	IO_L06P_2	IO_L06P_2	IO_L06P_2	IO_L06P_2	G21	I/O
2	N.C. (◆)	IO_L07N_2	IO_L07N_2	IO_L07N_2	IO_L07N_2	F23	I/O
2	N.C. (◆)	IO_L07P_2	IO_L07P_2	IO_L07P_2	IO_L07P_2	F24	I/O
2	N.C. (◆)	IO_L08N_2	IO_L08N_2	IO_L08N_2	IO_L08N_2	G22	I/O
2	N.C. (◆)	IO_L08P_2	IO_L08P_2	IO_L08P_2	IO_L08P_2	G23	I/O
2	N.C. (◆)	IO_L09N_2/VREF_2[1]	IO_L09N_2/VREF_2	IO_L09N_2/VREF_2	IO_L09N_2/VREF_2	F25	VREF[1]
2	N.C. (◆)	IO_L09P_2	IO_L09P_2	IO_L09P_2	IO_L09P_2	F26	I/O
2	N.C. (◆)	IO_L10N_2	IO_L10N_2	IO_L10N_2	IO_L10N_2	G25	I/O
2	N.C. (◆)	IO_L10P_2	IO_L10P_2	IO_L10P_2	IO_L10P_2	G26	I/O
2	IO_L14N_2	IO_L14N_2	IO_L14N_2[2]	IO_L11N_2[2]	IO_L11N_2	H20	I/O
2	IO_L14P_2	IO_L14P_2	IO_L14P_2[2]	IO_L11P_2[2]	IO_L11P_2	H21	I/O
2	IO_L16N_2	IO_L16N_2	IO_L16N_2[2]	IO_L12N_2[2]	IO_L12N_2	H22	I/O
2	IO_L16P_2	IO_L16P_2	IO_L16P_2[2]	IO_L12P_2[2]	IO_L12P_2	J21	I/O
2	IO_L17N_2	IO_L17N_2	IO_L17N_2[2]	IO_L13N_2[2]	IO[3]	H23	I/O
2	IO_L17P_2/VREF_2	IO_L17P_2/VREF_2	IO_L17P_2[2]/VREF_2	IO_L13P_2[2]/VREF_2	IO/VREF_2[3]	H24	VREF
2	IO_L19N_2	IO_L19N_2	IO_L19N_2	IO_L19N_2	IO_L19N_2	H25	I/O
2	IO_L19P_2	IO_L19P_2	IO_L19P_2	IO_L19P_2	IO_L19P_2	H26	I/O
2	IO_L20N_2	IO_L20N_2	IO_L20N_2	IO_L20N_2	IO_L20N_2	J20	I/O
2	IO_L20P_2	IO_L20P_2	IO_L20P_2	IO_L20P_2	IO_L20P_2	K20	I/O
2	IO_L21N_2	IO_L21N_2	IO_L21N_2	IO_L21N_2	IO_L21N_2	J22	I/O
2	IO_L21P_2	IO_L21P_2	IO_L21P_2	IO_L21P_2	IO_L21P_2	J23	I/O
2	IO_L22N_2	IO_L22N_2	IO_L22N_2	IO_L22N_2	IO_L22N_2	J24	I/O
2	IO_L22P_2	IO_L22P_2	IO_L22P_2	IO_L22P_2	IO_L22P_2	J25	I/O
2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	K21	VREF
2	IO_L23P_2	IO_L23P_2	IO_L23P_2	IO_L23P_2	IO_L23P_2	K22	I/O
2	IO_L24N_2	IO_L24N_2	IO_L24N_2	IO_L24N_2	IO_L24N_2	K23	I/O
2	IO_L24P_2	IO_L24P_2	IO_L24P_2	IO_L24P_2	IO_L24P_2	K24	I/O
2	IO_L26N_2	IO_L26N_2	IO_L26N_2	IO_L26N_2	IO_L26N_2	K25	I/O
2	IO_L26P_2	IO_L26P_2	IO_L26P_2	IO_L26P_2	IO_L26P_2	K26	I/O
2	IO_L27N_2	IO_L27N_2	IO_L27N_2	IO_L27N_2	IO_L27N_2	L19	I/O
2	IO_L27P_2	IO_L27P_2	IO_L27P_2	IO_L27P_2	IO_L27P_2	L20	I/O
2	IO_L28N_2	IO_L28N_2	IO_L28N_2	IO_L28N_2	IO_L28N_2	L21	I/O
2	IO_L28P_2	IO_L28P_2	IO_L28P_2	IO_L28P_2	IO_L28P_2	L22	I/O
2	IO_L29N_2	IO_L29N_2	IO_L29N_2	IO_L29N_2	IO_L29N_2	L25	I/O
2	IO_L29P_2	IO_L29P_2	IO_L29P_2	IO_L29P_2	IO_L29P_2	L26	I/O
2	IO_L31N_2	IO_L31N_2	IO_L31N_2	IO_L31N_2	IO_L31N_2	M19	I/O
2	IO_L31P_2	IO_L31P_2	IO_L31P_2	IO_L31P_2	IO_L31P_2	M20	I/O
2	IO_L32N_2	IO_L32N_2	IO_L32N_2	IO_L32N_2	IO_L32N_2	M21	I/O
2	IO_L32P_2	IO_L32P_2	IO_L32P_2	IO_L32P_2	IO_L32P_2	M22	I/O
2	IO_L33N_2	IO_L33N_2	IO_L33N_2	IO_L33N_2	IO_L33N_2	L23	I/O
2	IO_L33P_2	IO_L33P_2	IO_L33P_2	IO_L33P_2	IO_L33P_2	M24	I/O

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
5	IO_L01P_5/CS_B	IO_L01P_5/CS_B	IO_L01P_5/CS_B	IO_L01P_5/CS_B	IO_L01P_5/CS_B	AB5	DUAL
5	IO_L04N_5	IO_L04N_5	IO_L04N_5	IO_L04N_5	IO_L04N_5	AE4	I/O
5	IO_L04P_5	IO_L04P_5	IO_L04P_5	IO_L04P_5	IO_L04P_5	AD4	I/O
5	IO_L05N_5	IO_L05N_5	IO_L05N_5	IO_L05N_5	IO_L05N_5	AB6	I/O
5	IO_L05P_5	IO_L05P_5	IO_L05P_5	IO_L05P_5	IO_L05P_5	AA6	I/O
5	IO_L06N_5	IO_L06N_5	IO_L06N_5	IO_L06N_5	IO_L06N_5	AE5	I/O
5	IO_L06P_5	IO_L06P_5	IO_L06P_5	IO_L06P_5	IO_L06P_5	AD5	I/O
5	IO_L07N_5	IO_L07N_5	IO_L07N_5	IO_L07N_5	IO_L07N_5	AD6	I/O
5	IO_L07P_5	IO_L07P_5	IO_L07P_5	IO_L07P_5	IO_L07P_5	AC6	I/O
5	IO_L08N_5	IO_L08N_5	IO_L08N_5	IO_L08N_5	IO_L08N_5	AF6	I/O
5	IO_L08P_5	IO_L08P_5	IO_L08P_5	IO_L08P_5	IO_L08P_5	AE6	I/O
5	IO_L09N_5	IO_L09N_5	IO_L09N_5	IO_L09N_5	IO_L09N_5	AC7	I/O
5	IO_L09P_5	IO_L09P_5	IO_L09P_5	IO_L09P_5	IO_L09P_5	AB7	I/O
5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	AF7	DCI
5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	AE7	DCI
5	N.C. (◆)	IO_L11N_5/VREF_5	IO_L11N_5/VREF_5	IO_L11N_5/VREF_5	IO_L11N_5/VREF_5	AB8	VREF
5	N.C. (◆)	IO_L11P_5	IO_L11P_5	IO_L11P_5	IO_L11P_5	AA8	I/O
5	N.C. (◆)	IO_L12N_5	IO_L12N_5	IO_L12N_5	IO_L12N_5	AD8	I/O
5	N.C. (◆)	IO_L12P_5	IO_L12P_5	IO_L12P_5	IO_L12P_5	AC8	I/O
5	IO_L15N_5	IO_L15N_5	IO_L15N_5	IO_L15N_5	IO_L15N_5	AF8	I/O
5	IO_L15P_5	IO_L15P_5	IO_L15P_5	IO_L15P_5	IO_L15P_5	AE8	I/O
5	IO_L16N_5	IO_L16N_5	IO_L16N_5	IO_L16N_5	IO_L16N_5	AA9	I/O
5	IO_L16P_5	IO_L16P_5	IO_L16P_5	IO_L16P_5	IO_L16P_5	Y9	I/O
5	N.C. (◆)	IO_L18N_5	IO_L18N_5	IO_L18N_5	IO_L18N_5	AE9	I/O
5	N.C. (◆)	IO_L18P_5	IO_L18P_5	IO_L18P_5	IO_L18P_5	AD9	I/O
5	IO_L19N_5	IO_L19N_5	IO_L19N_5	IO_L19N_5	IO_L19N_5	AA10	I/O
5	IO_L19P_5/VREF_5	IO_L19P_5/VREF_5	IO_L19P_5/VREF_5	IO_L19P_5/VREF_5	IO_L19P_5/VREF_5	Y10	VREF
5	IO_L22N_5	IO_L22N_5	IO_L22N_5	IO_L22N_5	IO_L22N_5	AC10	I/O
5	IO_L22P_5	IO_L22P_5	IO_L22P_5	IO_L22P_5	IO_L22P_5	AB10	I/O
5	N.C. (◆)	IO_L23N_5	IO_L23N_5	IO_L23N_5	IO_L23N_5	AF10	I/O
5	N.C. (◆)	IO_L23P_5	IO_L23P_5	IO_L23P_5	IO_L23P_5	AE10	I/O
5	IO_L24N_5	IO_L24N_5	IO_L24N_5	IO_L24N_5	IO_L24N_5	Y11	I/O
5	IO_L24P_5	IO_L24P_5	IO_L24P_5	IO_L24P_5	IO_L24P_5	W11	I/O
5	IO_L25N_5	IO_L25N_5	IO_L25N_5	IO_L25N_5	IO_L25N_5	AB11	I/O
5	IO_L25P_5	IO_L25P_5	IO_L25P_5	IO_L25P_5	IO_L25P_5	AA11	I/O
5	N.C. (◆)	IO_L26N_5	IO_L26N_5	IO_L26N_5	IO_L26N_5	AF11	I/O
5	N.C. (◆)	IO_L26P_5	IO_L26P_5	IO_L26P_5	IO_L26P_5	AE11	I/O
5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	Y12	VREF
5	IO_L27P_5	IO_L27P_5	IO_L27P_5	IO_L27P_5	IO_L27P_5	W12	I/O
5	IO_L28N_5/D6	IO_L28N_5/D6	IO_L28N_5/D6	IO_L28N_5/D6	IO_L28N_5/D6	AB12	DUAL
5	IO_L28P_5/D7	IO_L28P_5/D7	IO_L28P_5/D7	IO_L28P_5/D7	IO_L28P_5/D7	AA12	DUAL
5	IO_L29N_5	IO_L29N_5	IO_L29N_5	IO_L29N_5	IO_L29N_5	AF12	I/O

FG900: 900-lead Fine-pitch Ball Grid Array

The 900-lead fine-pitch ball grid array package, FG900, supports three different Spartan-3 devices, including the XC3S2000, the XC3S4000, and the XC3S5000. The footprints for the XC3S4000 and XC3S5000 are identical, as shown in Table 107 and Figure 55. The XC3S2000, however, has fewer I/O pins which consequently results in 68 unconnected pins on the FG900 package, labeled as “N.C.” In Table 107 and Figure 55, these unconnected pins are indicated with a black diamond symbol (◆).

All the package pins appear in Table 107 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

If there is a difference between the XC3S2000 pinout and the pinout for the XC3S4000 and XC3S5000, then that difference is highlighted in Table 107. If the table entry is shaded, then there is an unconnected pin on the XC3S2000 that maps to a user-I/O pin on the XC3S4000 and XC3S5000.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

Pinout Table

Table 107: **FG900 Package Pinout**

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
0	IO	IO	E15	I/O
0	IO	IO	K15	I/O
0	IO	IO	D13	I/O
0	IO	IO	K13	I/O
0	IO	IO	G8	I/O
0	IO/VREF_0	IO/VREF_0	F9	VREF
0	IO/VREF_0	IO/VREF_0	C4	VREF
0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	B4	DCI
0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	A4	DCI
0	IO_L02N_0	IO_L02N_0	B5	I/O
0	IO_L02P_0	IO_L02P_0	A5	I/O
0	IO_L03N_0	IO_L03N_0	D5	I/O
0	IO_L03P_0	IO_L03P_0	E6	I/O
0	IO_L04N_0	IO_L04N_0	C6	I/O
0	IO_L04P_0	IO_L04P_0	B6	I/O
0	IO_L05N_0	IO_L05N_0	F6	I/O
0	IO_L05P_0/VREF_0	IO_L05P_0/VREF_0	F7	VREF
0	IO_L06N_0	IO_L06N_0	D7	I/O
0	IO_L06P_0	IO_L06P_0	C7	I/O
0	IO_L07N_0	IO_L07N_0	F8	I/O
0	IO_L07P_0	IO_L07P_0	E8	I/O
0	IO_L08N_0	IO_L08N_0	D8	I/O
0	IO_L08P_0	IO_L08P_0	C8	I/O
0	IO_L09N_0	IO_L09N_0	B8	I/O
0	IO_L09P_0	IO_L09P_0	A8	I/O

FG900 Footprint

Left Half of FG900 Package (Top View)

XC3S2000
(565 max. user I/O)

- 481 — **I/O:** Unrestricted, general-purpose user I/O
- 48 — **VREF:** User I/O or input voltage reference for bank
- 68 — **N.C.:** Unconnected pins for XC3S2000 (◆)

XC3S4000, XC3S5000
(633 max user I/O)

- 549 — **I/O:** Unrestricted, general-purpose user I/O
- 48 — **VREF:** User I/O or input voltage reference for bank
- 0 — **N.C.:** No unconnected pins in this package

All devices

- 12 — **DUAL:** Configuration pin, then possible user I/O
- 8 — **GCLK:** User I/O or global clock buffer input
- 16 — **DCI:** User I/O or reference resistor input for bank
- 7 — **CONFIG:** Dedicated configuration pins
- 4 — **JTAG:** Dedicated JTAG port pins
- 32 — **VCCINT:** Internal core voltage supply (+1.2V)
- 80 — **VCCO:** Output voltage supply for bank
- 24 — **VCCAUX:** Auxiliary voltage supply (+2.5V)
- 120 — **GND:** Ground

Bank 0 (top, columns 4–15); Bank 7 (left, rows A/C–R); Bank 6 (left, rows T–AH); Bank 5 (bottom, columns 4–15)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	GND	GND	HSWAP_EN	I/O L01P_0 VRN_0	I/O L02P_0	GND	I/O L35P_0 ◆	I/O L09P_0	I/O L38P_0 ◆	GND	I/O L17P_0	I/O L22P_0	I/O L25P_0	GND	I/O L32P_0 GCLK6
B	GND	GND	PROG_B	I/O L01N_0 VRP_0	I/O L02N_0	I/O L04P_0	I/O L35N_0 ◆	I/O L09N_0	I/O L38N_0 ◆	I/O L12P_0	I/O L17N_0	I/O L22N_0	I/O L25N_0	I/O L28P_0	I/O L32N_0 GCLK7
C	I/O L01N_7 VRP_7	I/O L01P_7 VRN_7	TDI	IO VREF_0	VCCO_0	I/O L04N_0	I/O L06P_0	I/O L08P_0	VCCO_0	I/O L12N_0	I/O L16P_0	I/O L21P_0	VCCO_0	I/O L28N_0	I/O L31P_0 VREF_0
D	I/O L03N_7 VREF_7	I/O L03P_7	I/O L02N_7	I/O L02P_7	I/O L03N_0	VCCAUX	I/O L06N_0	I/O L08N_0	I/O L37P_0 ◆	VCCAUX	I/O L16N_0	I/O L21N_0	I/O	VCCAUX	I/O L31N_0
E	I/O L04N_7	I/O L04P_7	VCCO_7	I/O L05P_7	GND	I/O L03P_0	VCCO_0	I/O L07P_0	I/O L37N_0 ◆	GND	I/O L15P_0	I/O L20P_0	I/O L24P_0	GND	I/O
F	GND	I/O L06N_7	I/O L06P_7	VCCAUX	I/O L05N_7	I/O L05N_0	I/O L05P_0 VREF_0	I/O L07N_0	IO VREF_0	I/O L11P_0	I/O L15N_0	I/O L20N_0	I/O L24N_0	I/O L27P_0	I/O L30P_0
G	I/O L08N_7	I/O L08P_7	I/O L07N_7	I/O L07P_7	VCCO_7	I/O L09P_7	I/O L36N_0 ◆	I/O	VCCO_0	I/O L11N_0	I/O L14P_0	I/O L19P_0	VCCO_0	I/O L27N_0	I/O L30N_0
H	I/O L13N_7	I/O L13P_7	I/O L11N_7	I/O L11P_7	I/O L10N_7	I/O L10P_7 VREF_7	I/O L09N_7	I/O L36P_0 ◆	I/O L10P_0	GND	I/O L14N_0	I/O L19N_0	I/O L23P_0	GND	I/O L29P_0
J	I/O L15N_7	I/O L15P_7	VCCO_7	I/O L14N_7	I/O L14P_7	I/O	VCCO_7	I/O L16P_7 VREF_7	I/O L10N_0	I/O L13N_0	VCCO_0	I/O L18P_0	I/O L23N_0	I/O L26P_0 VREF_0	I/O L29N_0
K	GND	I/O L19N_7 VREF_7	I/O L19P_7	VCCAUX	GND	I/O L17N_7	I/O L17P_7	GND	I/O L16N_7	I/O L20P_7	I/O L13P_0	I/O L18N_0	I/O	I/O L26N_0	I/O
L	I/O L24N_7	I/O L24P_7	I/O L23N_7	I/O L23P_7	I/O L22N_7	I/O L22P_7	I/O L21N_7	I/O L21P_7	VCCO_7	I/O L20N_7	VCCINT	VCCO_0	VCCO_0	VCCO_0	VCCINT
M	I/O L27N_7	I/O L27P_7 VREF_7	I/O L26N_7	I/O L26P_7	I/O L49P_7 ◆	I/O L25N_7 ◆	I/O L25P_7 ◆	I/O L46N_7 ◆	I/O L46P_7 ◆	I/O L28P_7	VCCO_7	VCCINT	VCCINT	VCCINT	GND
N	I/O L31N_7	I/O L31P_7	VCCO_7	I/O L50N_7 ◆	I/O L50P_7 ◆	I/O L49N_7 ◆	VCCO_7	I/O L29N_7	I/O L29P_7	I/O L28N_7	VCCO_7	VCCINT	GND	GND	GND
P	GND	I/O L34N_7	I/O L34P_7	VCCAUX	GND	I/O L33N_7	I/O L33P_7	GND	I/O L32N_7	I/O L32P_7	VCCO_7	VCCINT	GND	GND	GND
R	I/O L40N_7 VREF_7	I/O L40P_7	I/O L39N_7	I/O L39P_7	I/O L38N_7	I/O L38P_7	I/O L37N_7	I/O L37P_7 VREF_7	I/O L35N_7	I/O L35P_7	VCCINT	GND	GND	GND	GND
T	I/O L40P_6 VREF_6	I/O L40N_6	I/O L39P_6	I/O L39N_6	I/O L38P_6	I/O L38N_6	I/O L52P_6 ◆	I/O L52N_6 ◆	I/O L37P_6	I/O L37N_6	VCCINT	GND	GND	GND	GND
U	GND	I/O L36P_6 ◆	I/O L36N_6 ◆	VCCAUX	GND	I/O L35P_6	I/O L35N_6	GND	I/O L34P_6	I/O L34N_6 VREF_6	VCCO_6	VCCINT	GND	GND	GND
V	I/O L33P_6	I/O L33N_6	VCCO_6	I/O L32P_6	I/O L32N_6	I/O L31P_6	VCCO_6	I/O L30P_6 ◆	I/O L30N_6 ◆	I/O L29P_6	VCCO_6	VCCINT	GND	GND	GND
W	I/O L28P_6	I/O L28N_6	I/O L27P_6	I/O L27N_6	I/O L31N_6	I/O L26P_6	I/O L26N_6	I/O L25P_6 ◆	I/O L25N_6 ◆	I/O L29N_6	VCCO_6	VCCINT	VCCINT	VCCINT	GND
Y	I/O L24P_6	I/O L24N_6 VREF_6	I/O L45P_6 ◆	I/O L45N_6 ◆	I/O L22P_6	I/O L22N_6	I/O L21P_6	I/O L21N_6	VCCO_6	I/O L20P_6	VCCINT	VCCO_5	VCCO_5	VCCO_5	VCCINT
AA	GND	I/O L19P_6	I/O L19N_6	VCCAUX	GND	I/O L17P_6 VREF_6	I/O L17N_6	GND	I/O L16P_6	I/O L20N_6	I/O	I/O L22P_5	I/O L22N_5	I/O L26P_5	I/O
AB	I/O L15P_6	I/O L15N_6	VCCO_6	I/O L14P_6	I/O L14N_6	I/O	VCCO_6	I/O L16N_6	I/O L08P_5	I/O	VCCO_5	I/O L17N_5	I/O L23P_5	I/O L26N_5	I/O L29P_5 VREF_5
AC	I/O L13P_6 VREF_6	I/O L13N_6	I/O L11P_6	I/O L11N_6	I/O L10P_6	I/O L10N_6	I/O L09P_6	I/O L36P_5 ◆	I/O L08N_5	GND	I/O L17P_5	I/O L18P_5	I/O L23N_5	GND	I/O L29N_5
AD	I/O L08P_6	I/O L08N_6	I/O L07P_6	I/O L07N_6	VCCO_6	I/O L09N_6 VREF_6	I/O L05P_5	I/O L36N_5 ◆	VCCO_5	I/O L13P_5	I/O L13N_5	I/O L18N_5	VCCO_5	I/O L30P_5	I/O L30N_5
AE	GND	I/O L06P_6	I/O L06N_6	VCCAUX	I/O L05P_6	I/O	I/O L05N_5	I/O L37P_5 ◆	I/O L11P_5	I/O L11N_5 VREF_5	I/O L14P_5	I/O L19P_5 VREF_5	I/O L27P_5	I/O L27N_5 VREF_5	I/O
AF	I/O L04P_6	I/O L04N_6	VCCO_6	I/O L05N_6	GND	I/O L03N_5	VCCO_5	I/O L37N_5 ◆	I/O L09P_5	GND	I/O L14N_5	I/O L19N_5	I/O L24P_5	GND	I/O L31P_5 D5
AG	I/O L03P_6	I/O L03N_6 VREF_6	I/O L02P_6	I/O L02N_6	I/O L03P_5	VCCAUX	I/O L06P_5	I/O L38P_5 ◆	I/O L09N_5	VCCAUX	I/O L15P_5	I/O L20P_5	I/O L24N_5	VCCAUX	I/O L31N_5 D4
AH	I/O L01P_6 VRN_6	I/O L01N_6 VRP_6	M1	IO VREF_5	VCCO_5	I/O L04P_5	I/O L06N_5	I/O L38N_5 ◆	VCCO_5	I/O L12P_5	I/O L15N_5	I/O L20N_5	VCCO_5	I/O L28P_5 D7	I/O L32P_5 GCLK2
AJ	GND	GND	M0	I/O L01P_5 CS_B	I/O L02P_5	I/O L04N_5	I/O L35P_5 ◆	I/O L07P_5	I/O L10P_5 VRN_5	I/O L12N_5	I/O L16P_5	I/O L21P_5	I/O L25P_5	I/O L28N_5 D6	I/O L32N_5 GCLK3
AK	GND	GND	M2	I/O L01N_5 RDWR_B	I/O L02N_5	GND	I/O L35N_5 ◆	I/O L07N_5	I/O L10N_5 VRP_5	GND	I/O L16N_5	I/O L21N_5	I/O L25N_5	GND	IO VREF_5

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Figure 55: **FG900 Package Footprint (Top View)**

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
0	VCCO_0	VCCO_0	F13	VCCO
0	VCCO_0	VCCO_0	G8	VCCO
0	VCCO_0	VCCO_0	H11	VCCO
0	VCCO_0	VCCO_0	H15	VCCO
0	VCCO_0	VCCO_0	M13	VCCO
0	VCCO_0	VCCO_0	M14	VCCO
0	VCCO_0	VCCO_0	M15	VCCO
0	VCCO_0	VCCO_0	M16	VCCO
1	IO	IO	B26	I/O
1	IO	IO	A18	I/O
1	IO	IO	C23	I/O
1	IO	IO	E21	I/O
1	IO	IO	E25	I/O
1	IO	IO	F18	I/O
1	IO	IO	F27	I/O
1	IO	IO	F29	I/O
1	IO	IO	H23	I/O
1	IO	IO	H26	I/O
1	N.C. (◆)	IO	J26	I/O
1	IO	IO	K19	I/O
1	IO	IO	L19	I/O
1	IO	IO	L20	I/O
1	IO	IO	L21	I/O
1	N.C. (◆)	IO	L23	I/O
1	IO	IO	L24	I/O
1	IO/VREF_1	IO/VREF_1	D30	VREF
1	IO/VREF_1	IO/VREF_1	K21	VREF
1	IO/VREF_1	IO/VREF_1	L18	VREF
1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	A32	DCI
1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	B32	DCI
1	IO_L02N_1	IO_L02N_1	A31	I/O
1	IO_L02P_1	IO_L02P_1	B31	I/O
1	IO_L03N_1	IO_L03N_1	B30	I/O
1	IO_L03P_1	IO_L03P_1	C30	I/O
1	IO_L04N_1	IO_L04N_1	C29	I/O
1	IO_L04P_1	IO_L04P_1	D29	I/O
1	IO_L05N_1	IO_L05N_1	A29	I/O
1	IO_L05P_1	IO_L05P_1	B29	I/O
1	IO_L06N_1/VREF_1	IO_L06N_1/VREF_1	E28	VREF
1	IO_L06P_1	IO_L06P_1	F28	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
N/A	VCCAUX	VCCAUX	Y5	VCCAUX
N/A	VCCINT	VCCINT	AA13	VCCINT
N/A	VCCINT	VCCINT	AA22	VCCINT
N/A	VCCINT	VCCINT	AB13	VCCINT
N/A	VCCINT	VCCINT	AB14	VCCINT
N/A	VCCINT	VCCINT	AB15	VCCINT
N/A	VCCINT	VCCINT	AB16	VCCINT
N/A	VCCINT	VCCINT	AB19	VCCINT
N/A	VCCINT	VCCINT	AB20	VCCINT
N/A	VCCINT	VCCINT	AB21	VCCINT
N/A	VCCINT	VCCINT	AB22	VCCINT
N/A	VCCINT	VCCINT	AC12	VCCINT
N/A	VCCINT	VCCINT	AC17	VCCINT
N/A	VCCINT	VCCINT	AC18	VCCINT
N/A	VCCINT	VCCINT	AC23	VCCINT
N/A	VCCINT	VCCINT	M12	VCCINT
N/A	VCCINT	VCCINT	M17	VCCINT
N/A	VCCINT	VCCINT	M18	VCCINT
N/A	VCCINT	VCCINT	M23	VCCINT
N/A	VCCINT	VCCINT	N13	VCCINT
N/A	VCCINT	VCCINT	N14	VCCINT
N/A	VCCINT	VCCINT	N15	VCCINT
N/A	VCCINT	VCCINT	N16	VCCINT
N/A	VCCINT	VCCINT	N19	VCCINT
N/A	VCCINT	VCCINT	N20	VCCINT
N/A	VCCINT	VCCINT	N21	VCCINT
N/A	VCCINT	VCCINT	N22	VCCINT
N/A	VCCINT	VCCINT	P13	VCCINT
N/A	VCCINT	VCCINT	P22	VCCINT
N/A	VCCINT	VCCINT	R13	VCCINT
N/A	VCCINT	VCCINT	R22	VCCINT
N/A	VCCINT	VCCINT	T13	VCCINT
N/A	VCCINT	VCCINT	T22	VCCINT
N/A	VCCINT	VCCINT	U12	VCCINT
N/A	VCCINT	VCCINT	U23	VCCINT
N/A	VCCINT	VCCINT	V12	VCCINT
N/A	VCCINT	VCCINT	V23	VCCINT
N/A	VCCINT	VCCINT	W13	VCCINT
N/A	VCCINT	VCCINT	W22	VCCINT
N/A	VCCINT	VCCINT	Y13	VCCINT