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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	192
Number of Logic Elements/Cells	1728
Total RAM Bits	73728
Number of I/O	63
Number of Gates	50000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s50-4vqg100i

According to Figure 7, the clock line OTCLK1 connects the CK inputs of the upper registers on the output and three-state paths. Similarly, OTCLK2 connects the CK inputs for the lower registers on the output and three-state paths. The upper and lower registers on the input path have independent clock lines: ICLK1 and ICLK2. The enable line OCE connects the CE inputs of the upper and lower registers on the output path. Similarly, TCE connects the CE inputs for the register pair on the three-state path and ICE does the same for the register pair on the input path. The Set/Reset (SR) line entering the IOB is common to all six registers, as is the Reverse (REV) line.

Each storage element supports numerous options in addition to the control over signal polarity described in the IOB Overview section. These are described in Table 6.

Table 6: **Storage Element Options**

Option Switch	Function	Specificity
FF/Latch	Chooses between an edge-sensitive flip-flop or a level-sensitive latch	Independent for each storage element.
SYNC/ASYNC	Determines whether SR is synchronous or asynchronous	Independent for each storage element.
SRHIGH/SRLOW	Determines whether SR acts as a Set, which forces the storage element to a logic "1" (SRHIGH) or a Reset, which forces a logic "0" (SRLOW).	Independent for each storage element, except when using FDDR. In the latter case, the selection for the upper element (OFF1 or TFF2) applies to both elements.
INIT1/INIT0	In the event of a Global Set/Reset, after configuration or upon activation of the GSR net, this switch decides whether to set or reset a storage element. By default, choosing SRLOW also selects INIT0; choosing SRHIGH also selects INIT1.	Independent for each storage element, except when using FDDR. In the latter case, selecting INIT0 for one element applies to both elements (even though INIT1 is selected for the other).

Double-Data-Rate Transmission

Double-Data-Rate (DDR) transmission describes the technique of synchronizing signals to both the rising and falling edges of the clock signal. Spartan-3 devices use register-pairs in all three IOB paths to perform DDR operations.

The pair of storage elements on the IOB's Output path (OFF1 and OFF2), used as registers, combine with a special multiplexer to form a DDR D-type flip-flop (FDDR). This primitive permits DDR transmission where output data bits are synchronized to both the rising and falling edges of a clock. It is possible to access this function by placing either an FDDRRSE or an FDDRCPE component or symbol into the design. DDR operation requires two clock signals (50% duty cycle), one the inverted form of the other. These signals trigger the two registers in alternating fashion, as shown in Figure 8. Commonly, the Digital Clock Manager (DCM) generates the two clock signals by mirroring an incoming signal, then shifting it 180 degrees. This approach ensures minimal skew between the two signals.

The storage-element-pair on the Three-State path (TFF1 and TFF2) can also be combined with a local multiplexer to form an FDDR primitive. This permits synchronizing the output enable to both the rising and falling edges of a clock. This DDR operation is realized in the same way as for the output path.

The storage-element-pair on the input path (IFF1 and IFF2) allows an I/O to receive a DDR signal. An incoming DDR clock signal triggers one register and the inverted clock signal triggers the other register. In this way, the registers take turns capturing bits of the incoming DDR data signal.

The DCI feature operates independently for each of the device's eight banks. Each bank has an 'N' reference pin (VRN) and a 'P' reference pin, (VRP), to calibrate driver and termination resistance. Only when using a DCI standard on a given bank do these two pins function as VRN and VRP. When not using a DCI standard, the two pins function as user I/Os. As shown in Figure 9, add an external reference resistor to pull the VRN pin up to V_{CCO} and another reference resistor to pull the VRP pin down to GND. Also see Figure 42, page 116. Both resistors have the same value—commonly 50Ω—with one-percent tolerance, which is either the characteristic impedance of the line or twice that, depending on the DCI standard in use. Standards having a symbol name that contains the letters "DV2" use a reference resistor value that is twice the line impedance. DCI adjusts the output driver impedance to match the reference resistors' value or half that, according to the standard. DCI always adjusts the on-chip termination resistors to directly match the reference resistors' value.

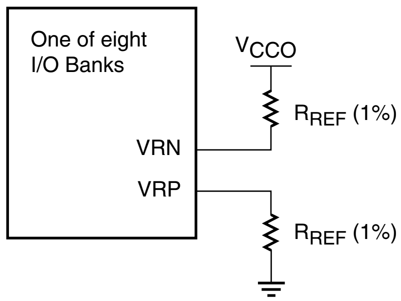

Figure 9: **Connection of Reference Resistors (R_{REF})**

The rules guiding the use of DCI standards on banks are as follows:

- No more than one DCI I/O standard with a Single Termination is allowed per bank.
- No more than one DCI I/O standard with a Split Termination is allowed per bank.
- Single Termination, Split Termination, Controlled- Impedance Driver, and Controlled-Impedance Driver with Half Impedance can co-exist in the same bank.

See also The Organization of IOBs into Banks, immediately below, and DCI: User I/O or Digitally Controlled Impedance Resistor Reference Input, page 115.

The Organization of IOBs into Banks

IOBs are allocated among eight banks, so that each side of the device has two banks, as shown in Figure 10. For all packages, each bank has independent V_{REF} lines. For example, V_{REF} Bank 3 lines are separate from the V_{REF} lines going to all other banks.

For the Very Thin Quad Flat Pack (VQ), Plastic Quad Flat Pack (PQ), Fine Pitch Thin Ball Grid Array (FT), and Fine Pitch Ball Grid Array (FG) packages, each bank has dedicated V_{CCO} lines. For example, the V_{CCO} Bank 7 lines are separate from the V_{CCO} lines going to all other banks. Thus, Spartan-3 devices in these packages support eight independent V_{CCO} supplies.

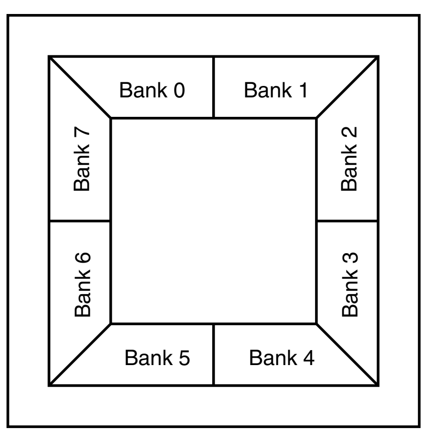

Figure 10: **Spartan-3 FPGA I/O Banks (Top View)**

Each BUFGMUX element, shown in Figure 24, is a 2-to-1 multiplexer that can receive signals from any of the four following sources:

- One of the four Global Clock inputs on the same side of the die—top or bottom—as the BUFGMUX element in use.
- Any of four nearby horizontal Double lines.
- Any of four outputs from the DCM in the right-hand quadrant that is on the same side of the die as the BUFGMUX element in use.
- Any of four outputs from the DCM in the left-hand quadrant that is on the same side of the die as the BUFGMUX element in use.

The multiplexer select line, S, chooses which of the two inputs, I0 or I1, drives the BUFGMUX's output signal, O, as described in Table 25. The switching from one clock to the other is glitchless, and done in such a way that the output High and Low times are never shorter than the shortest High or Low time of either input clock.

Table 25: **BUFGMUX Select Mechanism**

S Input	O Output
0	I0 Input
1	I1 Input

The two clock inputs can be asynchronous with regard to each other, and the S input can change at any time, except for a short setup time prior to the rising edge of the presently selected clock (I0 or I1). Violating this setup time requirement can result in an undefined runt pulse output.

The BUFG clock buffer primitive drives a single clock signal onto the clock network and is essentially the same element as a BUFGMUX, just without the clock select mechanism. Similarly, the BUFGCE primitive creates an enabled clock buffer using the BUFGMUX select mechanism.

Each BUFGMUX buffers incoming clock signals to two possible destinations:

- The vertical spine belonging to the same side of the die—top or bottom—as the BUFGMUX element in use. The two spines—top and bottom—each comprise four vertical clock lines, each running from one of the BUFGMUX elements on the same side towards the center of the die. At the center of the die, clock signals reach the eight-line horizontal spine, which spans the width of the die. In turn, the horizontal spine branches out into a subsidiary clock interconnect that accesses the CLBs.
- The clock input of either DCM on the same side of the die—top or bottom—as the BUFGMUX element in use.

Use either a BUFGMUX element or a BUFG (Global Clock Buffer) element to place a Global input in the design. For the purpose of minimizing the dynamic power dissipation of the clock network, the Xilinx development software automatically disables all clock line segments that a design does not use.

A global clock line ideally drives clock inputs on the various clocked elements within the FPGA, such as CLB or IOB flip-flops or block RAMs. A global clock line also optionally drives combinatorial inputs. However, doing so provides additional loading on the clock line that might also affect clock jitter. Ideally, drive combinatorial inputs using the signal that also drives the input to the BUFGMUX or BUFG element.

For more details, refer to the chapter entitled "Using Global Clock Resources" in UG331.

Table 34: **Quiescent Supply Current Characteristics**

Symbol	Description	Device	Typical[(1)]	Commercial Maximum[(1)]	Industrial Maximum[(1)]	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC3S50	5	24	31	mA
		XC3S200	10	54	80	mA
		XC3S400	15	110	157	mA
		XC3S1000	35	160	262	mA
		XC3S1500	45	260	332	mA
		XC3S2000	60	360	470	mA
		XC3S4000	100	450	810	mA
		XC3S5000	120	600	870	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC3S50	1.5	2.0	2.5	mA
		XC3S200	1.5	3.0	3.5	mA
		XC3S400	1.5	3.0	3.5	mA
		XC3S1000	2.0	4.0	5.0	mA
		XC3S1500	2.5	4.0	5.0	mA
		XC3S2000	3.0	5.0	6.0	mA
		XC3S4000	3.5	5.0	6.0	mA
		XC3S5000	3.5	5.0	6.0	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC3S50	7	20	22	mA
		XC3S200	10	30	33	mA
		XC3S400	15	40	44	mA
		XC3S1000	20	50	55	mA
		XC3S1500	35	75	85	mA
		XC3S2000	45	90	100	mA
		XC3S4000	55	110	125	mA
		XC3S5000	70	130	145	mA

Notes:

1. The numbers in this table are based on the conditions set forth in Table 32. Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. Typical values are characterized using devices with typical processing at room temperature (T_J of 25°C at V_{CCINT} = 1.2V, V_{CCO} = 3.3V, and V_{CCAUX} = 2.5V). Maximum values are the production test limits measured for each device at the maximum specified junction temperature and at maximum voltage limits with V_{CCINT} = 1.26V, V_{CCO} = 3.465V, and V_{CCAUX} = 2.625V. The FPGA is programmed with a "blank" configuration data file (i.e., a design with no functional elements instantiated). For conditions other than those described above, (e.g., a design including functional elements, the use of DCI standards, etc.), measured quiescent current levels may be different than the values in the table. Use the XPower Estimator or XPower Analyzer for more accurate estimates. See Note 2.
2. There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The Spartan-3 XPower Estimator provides quick, approximate, typical estimates, and does not require a netlist of the design. b) XPower Analyzer, part of the Xilinx ISE development software, uses the FPGA netlist as input to provide more accurate maximum and typical estimates.
3. The maximum numbers in this table also indicate the minimum current each power rail requires in order for the FPGA to power-on successfully, once all three rails are supplied. If V_{CCINT} is applied before V_{CCAUX}, there may be temporary additional I_{CCINT} current until V_{CCAUX} is applied. See Surplus I_{CCINT} if V_{CCINT} Applied before V_{CCAUX}, page 54

Table 48: **Test Methods for Timing Measurement at I/Os *(Cont'd)***

Signal Standard (IOSTANDARD)	Inputs			Outputs		Inputs and Outputs
	V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
HSTL_III_18	1.1	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{REF}
HSTL_III_DCI_18						
LVCMOS12	-	0	1.2	1M	0	0.6
LVCMOS15	-	0	1.5	1M	0	0.75
LVDCI_15						
LVDCI_DV2_15						
HSLVDCI_15						
LVCMOS18	-	0	1.8	1M	0	0.9
LVDCI_18						
LVDCI_DV2_18						
HSLVDCI_18						
LVCMOS25	-	0	2.5	1M	0	1.25
LVDCI_25						
LVDCI_DV2_25						
HSLVDCI_25						
LVCMOS33	-	0	3.3	1M	0	1.65
LVDCI_33						
LVDCI_DV2_33						
HSLVDCI_33						
LVTTL	-	0	3.3	1M	0	1.4
PCI33_3 Rising	-	Note 3	Note 3	25	0	0.94
PCI33_3 Falling				25	3.3	2.03
SSTL18_I	0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL18_I_DCI						
SSTL18_II	0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL2_I	1.25	V_{REF} – 0.75	V_{REF} + 0.75	50	1.25	V_{REF}
SSTL2_I_DCI						
SSTL2_II	1.25	V_{REF} – 0.75	V_{REF} + 0.75	25	1.25	V_{REF}
SSTL2_II_DCI				50	1.25	
Differential						
LDT_25 (ULVDS_25)	-	V_{ICM} – 0.125	V_{ICM} + 0.125	60	0.6	V_{ICM}
LVDS_25	-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVDS_25_DCI				N/A	N/A	
BLVDS_25	-	V_{ICM} – 0.125	V_{ICM} + 0.125	1M	0	V_{ICM}
LVDSEXT_25	-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVDSEXT_25_DCI				N/A	N/A	
LVPECL_25	-	V_{ICM} – 0.3	V_{ICM} + 0.3	1M	0	V_{ICM}
RSDS_25	-	V_{ICM} – 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}
DIFF_HSTL_II_18	-	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.8	V_{ICM}
DIFF_HSTL_II_18_DCI						

Table 50: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}/GND Pair**

Signal Standard (IOSTANDARD)			Package				
			VQ100	TQ144	PQ208	CP132	FT256, FG320, FG456, FG676, FG900, FG1156
Single-Ended Standards							
GTL			0	0	0	1	14
GTL_DCI			0	0	0	1	14
GTLP			0	0	0	1	19
GTLP_DCI			0	0	0	1	19
HSLVDCI_15			6	6	6	6	14
HSLVDCI_18			7	7	7	7	10
HSLVDCI_25			7	7	7	7	11
HSLVDCI_33			10	10	10	10	10
HSTL_I			11	11	11	11	17
HSTL_I_DCI			11	11	11	11	17
HSTL_III			7	7	7	7	7
HSTL_III_DCI			7	7	7	7	7
HSTL_I_18			13	13	13	13	17
HSTL_I_DCI_18			13	13	13	13	17
HSTL_II_18			9	9	9	9	9
HSTL_II_DCI_18			9	9	9	9	9
HSTL_III_18			8	8	8	8	8
HSTL_III_DCI_18			8	8	8	8	8
LVCMOS12	Slow	2	17	17	17	17	55
		4	13	13	13	13	32
		6	10	10	10	10	18
	Fast	2	12	12	12	12	31
		4	11	11	11	11	13
		6	9	9	9	9	9
LVCMOS15	Slow	2	16	12	12	19	55
		4	8	7	7	9	31
		6	7	7	7	9	18
		8	6	6	6	6	15
		12	5	5	5	5	10
	Fast	2	10	10	10	13	25
		4	6	7	7	7	16
		6	7	7	7	7	13
		8	6	6	6	6	11
		12	6	6	6	6	7

Table 67: **Timing for the Master and Slave Parallel Configuration Modes *(Cont'd)***

Symbol	Description			Slave/ Master	All Speed Grades		Units
					Min	Max	
Clock Timing							
T_{CCH}	CCLK input pin High pulse width			Slave	5	∞	ns
T_{CCL}	CCLK input pin Low pulse width				5	∞	ns
F_{CCPAR}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	Not using the BUSY pin[(4)]		0	50	MHz
			Using the BUSY pin		0	66	MHz
		With bitstream compression			0	20	MHz
		During STARTUP phase			0	50	MHz
ΔF_{CCPAR}	Variation from the CCLK output frequency set using the BitGen option ConfigRate			Master	–50%	+50%	–

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32.
2. Some Xilinx documents may refer to Parallel modes as "SelectMAP" modes.
3. RDWR_B is synchronized to CCLK for the purpose of performing the Abort operation. The same pin asynchronously controls the driver impedance of the D0 - D7 pins. To avoid contention when writing configuration data to the D0 - D7 bus, do not bring RDWR_B High when CS_B is Low.
4. In the Slave Parallel mode, it is necessary to use the BUSY pin when the CCLK frequency exceeds this maximum specification.

Once the FPGA enters User mode after completing configuration, the DONE pin no longer drives the DONE pin Low. The bitstream generator option DonePin determines whether or not a pull-up resistor is present on the DONE pin to pull the pin to VCCAUX. If the pull-up resistor is eliminated, then the DONE pin must be pulled High using an external pull-up resistor or one of the FPGAs in the design must actively drive the DONE pin High via the DriveDone bitstream generator option.

The bitstream generator option DriveDone causes the FPGA to actively drive the DONE output High after configuration. This option should only be used in single-FPGA designs or on the last FPGA in a multi-FPGA daisy-chain.

By default, the bitstream generator software retains the pull-up resistor and does not actively drive the DONE pin as highlighted in Table 74, which shows the interaction of these bitstream options in single- and multi-FPGA designs.

Table 74: **DonePin and DriveDone Bitstream Option Interaction**

DonePin	DriveDone	Single- or Multi-FPGA Design	Comments
Pullnone	No	Single	External pull-up resistor, with value between 330Ω to 3.3kΩ, required on DONE.
Pullnone	No	Multi	External pull-up resistor, with value between 330Ω to 3.3kΩ, required on common node connecting to all DONE pins.
Pullnone	Yes	Single	OK, no external requirements.
Pullnone	Yes	Multi	DriveDone on last device in daisy-chain only. No external requirements.
Pullup	No	Single	OK, but pull-up on DONE pin has slow rise time. May require 330Ω pull-up resistor for high CCLK frequencies.
Pullup	No	Multi	External pull-up resistor, with value between 330Ω to 3.3kΩ, required on common node connecting to all DONE pins.
Pullup	Yes	Single	OK, no external requirements.
Pullup	Yes	Multi	DriveDone on last device in daisy-chain only. No external requirements.

M2, M1, M0: Configuration Mode Selection

The M2, M1, and M0 inputs select the FPGA configuration mode, as described in Table 75. The logic levels applied to the mode pins are sampled on the rising edge of INIT_B.

Table 75: **Spartan-3 FPGA Mode Select Settings**

Configuration Mode	M2	M1	M0
Master Serial	0	0	0
Slave Serial	1	1	1
Master Parallel	0	1	1
Slave Parallel	1	1	0
JTAG	1	0	1
Reserved	0	0	1
Reserved	0	1	0
Reserved	1	0	0
After Configuration	X	X	X

Notes:

1. X = don't care, either 0 or 1.

Before and during configuration, the mode pins have an internal pull-up resistor to VCCAUX, regardless of the HSWAP_EN pin. If the mode pins are unconnected, then the FPGA defaults to the Slave Serial configuration mode. After configuration successfully completes, any levels applied to these input are ignored. Furthermore, the bitstream generator options M0Pin, M1Pin, and M2Pin determines whether a pull-up resistor, pull-down resistor, or no resistor is present on its respective mode pin, M0, M1, or M2.

Table 79: **Pin Behavior After Power-Up, During Configuration *(Cont'd)***

Pin Name	Configuration Mode Settings <M2:M1:M0>					Bitstream Configuration Option
	Serial Modes		SelectMap Parallel Modes		JTAG Mode <1:0:1>	
	Master <0:0:0>	Slave <1:1:1>	Master <0:1:1>	Slave <1:1:0>		
IO_Lxxy_#/ D5			D5 (I/O)	D5 (I/O)		Persist UnusedPin
IO_Lxxy_#/ D6			D6 (I/O)	D6 (I/O)		Persist UnusedPin
IO_Lxxy_#/ D7			D7 (I/O)	D7 (I/O)		Persist UnusedPin
IO_Lxxy_#/ CS_B			CS_B (I)	CS_B (I)		Persist UnusedPin
IO_Lxxy_#/ RDWR_B			RDWR_B (I)	RDWR_B (I)		Persist UnusedPin
IO_Lxxy_#/ BUSY/DOUT	DOUT (O)	DOUT (O)	BUSY (O)	BUSY (O)		Persist UnusedPin
DUAL: Dual-purpose configuration pins (INIT_B has a pull-up resistor to VCCO_4 or VCCO_BOTTOM always active during configuration, regardless of HSWAP_EN pin)						
IO_Lxxy_#/ INIT_B	INIT_B (I/OD)	INIT_B (I/OD)	INIT_B (I/OD)	INIT_B (I/OD)		UnusedPin
DCI: Digitally Controlled Impedance reference resistor input pins						
IO_Lxxy_#/ VRN_#						UnusedPin
IO/VRN_#						UnusedPin
IO_Lxxy_#/ VRP_#						UnusedPin
IO/VRP_#						UnusedPin
GCLK: Global clock buffer inputs						
IO_Lxxy_#/ GCLK0 through GCLK7						UnusedPin
VREF: I/O bank input reference voltage pins						
IO_Lxxy_#/ VREF_#						UnusedPin
IO/VREF_#						UnusedPin
CONFIG: Dedicated configuration pins (pull-up resistor to VCCAUX always active during configuration, regardless of HSWAP_EN pin)						
CCLK	CCLK (I/O)	CCLK (I)	CCLK (I/O)	CCLK (I)		CclkPin ConfigRate
PROG_B	PROG_B (I) (pull-up)	PROG_B (I) (pull-up)	PROG_B (I) (pull-up)	PROG_B (I) (pull-up)	PROG_B (I), Via JPROG_B instruction	ProgPin
DONE	DONE (I/OD)	DONE (I/OD)	DONE (I/OD)	DONE (I/OD)	DONE (I/OD)	DriveDone DonePin DonePipe
M2	M2=0 (I)	M2=1 (I)	M2=0 (I)	M2=1 (I)	M2=1 (I)	M2Pin
M1	M1=0 (I)	M1=1 (I)	M1=1 (I)	M1=1 (I)	M1=0 (I)	M1Pin
M0	M0=0 (I)	M0=1 (I)	M0=1 (I)	M0=0 (I)	M0=1 (I)	M0Pin
HSWAP_EN	HSWAP_EN (I)	HSWAP_EN (I)	HSWAP_EN (I)	HSWAP_EN (I)	HSWAP_EN (I)	HswapenPin

Table 91: **TQ144 Package Pinout *(Cont'd)***

Bank	XC3S50, XC3S200, XC3S400 Pin Name	TQ144 Pin Number	Type
6,7	VCCO_LEFT	P34	VCCO
6,7	VCCO_LEFT	P3	VCCO
N/A	GND	P136	GND
N/A	GND	P139	GND
N/A	GND	P114	GND
N/A	GND	P117	GND
N/A	GND	P94	GND
N/A	GND	P101	GND
N/A	GND	P81	GND
N/A	GND	P88	GND
N/A	GND	P64	GND
N/A	GND	P67	GND
N/A	GND	P42	GND
N/A	GND	P45	GND
N/A	GND	P22	GND
N/A	GND	P29	GND
N/A	GND	P9	GND
N/A	GND	P16	GND
N/A	VCCAUX	P134	VCCAUX
N/A	VCCAUX	P120	VCCAUX
N/A	VCCAUX	P62	VCCAUX
N/A	VCCAUX	P48	VCCAUX
N/A	VCCINT	P133	VCCINT
N/A	VCCINT	P121	VCCINT
N/A	VCCINT	P61	VCCINT
N/A	VCCINT	P49	VCCINT
VCCAUX	CCLK	P72	CONFIG
VCCAUX	DONE	P71	CONFIG
VCCAUX	HSWAP_EN	P142	CONFIG
VCCAUX	M0	P38	CONFIG
VCCAUX	M1	P37	CONFIG
VCCAUX	M2	P39	CONFIG
VCCAUX	PROG_B	P143	CONFIG
VCCAUX	TCK	P110	JTAG
VCCAUX	TDI	P144	JTAG
VCCAUX	TDO	P109	JTAG
VCCAUX	TMS	P111	JTAG

Table 93: **PQ208 Package Pinout *(Cont'd)***

Bank	XC3S50 Pin Name	XC3S200, XC3S400 Pin Names	PQ208 Pin Number	Type
N/A	GND	GND	P14	GND
N/A	GND	GND	P25	GND
N/A	VCCAUX	VCCAUX	P193	VCCAUX
N/A	VCCAUX	VCCAUX	P173	VCCAUX
N/A	VCCAUX	VCCAUX	P142	VCCAUX
N/A	VCCAUX	VCCAUX	P121	VCCAUX
N/A	VCCAUX	VCCAUX	P89	VCCAUX
N/A	VCCAUX	VCCAUX	P69	VCCAUX
N/A	VCCAUX	VCCAUX	P38	VCCAUX
N/A	VCCAUX	VCCAUX	P17	VCCAUX
N/A	VCCINT	VCCINT	P192	VCCINT
N/A	VCCINT	VCCINT	P174	VCCINT
N/A	VCCINT	VCCINT	P88	VCCINT
N/A	VCCINT	VCCINT	P70	VCCINT
VCCAUX	CCLK	CCLK	P104	CONFIG
VCCAUX	DONE	DONE	P103	CONFIG
VCCAUX	HSWAP_EN	HSWAP_EN	P206	CONFIG
VCCAUX	M0	M0	P55	CONFIG
VCCAUX	M1	M1	P54	CONFIG
VCCAUX	M2	M2	P56	CONFIG
VCCAUX	PROG_B	PROG_B	P207	CONFIG
VCCAUX	TCK	TCK	P159	JTAG
VCCAUX	TDI	TDI	P208	JTAG
VCCAUX	TDO	TDO	P158	JTAG
VCCAUX	TMS	TMS	P160	JTAG

Table 96: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S200, XC3S400, XC3S1000 Pin Name	FT256 Pin Number	Type
7	IO_L24P_7	G4	I/O
7	IO_L39N_7	H3	I/O
7	IO_L39P_7	H4	I/O
7	IO_L40N_7/VREF_7	H1	VREF
7	IO_L40P_7	G1	I/O
7	VCCO_7	G6	VCCO
7	VCCO_7	H5	VCCO
7	VCCO_7	H6	VCCO
N/A	GND	A1	GND
N/A	GND	A16	GND
N/A	GND	B2	GND
N/A	GND	B9	GND
N/A	GND	B15	GND
N/A	GND	F6	GND
N/A	GND	F11	GND
N/A	GND	G7	GND
N/A	GND	G8	GND
N/A	GND	G9	GND
N/A	GND	G10	GND
N/A	GND	H2	GND
N/A	GND	H7	GND
N/A	GND	H8	GND
N/A	GND	H9	GND
N/A	GND	H10	GND
N/A	GND	J7	GND
N/A	GND	J8	GND
N/A	GND	J9	GND
N/A	GND	J10	GND
N/A	GND	J15	GND
N/A	GND	K7	GND
N/A	GND	K8	GND
N/A	GND	K9	GND
N/A	GND	K10	GND
N/A	GND	L6	GND
N/A	GND	L11	GND
N/A	GND	R2	GND
N/A	GND	R8	GND
N/A	GND	R15	GND
N/A	GND	T1	GND

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
7	IO_L20P_7	E1	I/O
7	IO_L21N_7	E4	I/O
7	IO_L21P_7	F4	I/O
7	IO_L22N_7	G5	I/O
7	IO_L22P_7	F5	I/O
7	IO_L23N_7	G1	I/O
7	IO_L23P_7	F2	I/O
7	IO_L24N_7	G4	I/O
7	IO_L24P_7	G3	I/O
7	IO_L27N_7	H5	I/O
7	IO_L27P_7/VREF_7	H6	VREF
7	IO_L34N_7	H4	I/O
7	IO_L34P_7	H3	I/O
7	IO_L35N_7	H1	I/O
7	IO_L35P_7	H2	I/O
7	IO_L39N_7	J1	I/O
7	IO_L39P_7	J2	I/O
7	IO_L40N_7/VREF_7	J5	VREF
7	IO_L40P_7	J4	I/O
7	VCCO_7	F3	VCCO
7	VCCO_7	H7	VCCO
7	VCCO_7	J7	VCCO
N/A	GND	A1	GND
N/A	GND	A13	GND
N/A	GND	A18	GND
N/A	GND	A6	GND
N/A	GND	B17	GND
N/A	GND	B2	GND
N/A	GND	C10	GND
N/A	GND	C9	GND
N/A	GND	F1	GND
N/A	GND	F18	GND
N/A	GND	G12	GND
N/A	GND	G7	GND
N/A	GND	H10	GND
N/A	GND	H11	GND
N/A	GND	H8	GND
N/A	GND	H9	GND
N/A	GND	J11	GND
N/A	GND	J16	GND

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
N/A	GND	J3	GND
N/A	GND	J8	GND
N/A	GND	K11	GND
N/A	GND	K16	GND
N/A	GND	K3	GND
N/A	GND	K8	GND
N/A	GND	L10	GND
N/A	GND	L11	GND
N/A	GND	L8	GND
N/A	GND	L9	GND
N/A	GND	M12	GND
N/A	GND	M7	GND
N/A	GND	N1	GND
N/A	GND	N18	GND
N/A	GND	T10	GND
N/A	GND	T9	GND
N/A	GND	U17	GND
N/A	GND	U2	GND
N/A	GND	V1	GND
N/A	GND	V13	GND
N/A	GND	V18	GND
N/A	GND	V6	GND
N/A	VCCAUX	B12	VCCAUX
N/A	VCCAUX	B7	VCCAUX
N/A	VCCAUX	G17	VCCAUX
N/A	VCCAUX	G2	VCCAUX
N/A	VCCAUX	M17	VCCAUX
N/A	VCCAUX	M2	VCCAUX
N/A	VCCAUX	U12	VCCAUX
N/A	VCCAUX	U7	VCCAUX
N/A	VCCINT	F12	VCCINT
N/A	VCCINT	F13	VCCINT
N/A	VCCINT	F6	VCCINT
N/A	VCCINT	F7	VCCINT
N/A	VCCINT	G13	VCCINT
N/A	VCCINT	G6	VCCINT
N/A	VCCINT	M13	VCCINT
N/A	VCCINT	M6	VCCINT
N/A	VCCINT	N12	VCCINT
N/A	VCCINT	N13	VCCINT

User I/Os by Bank

Table 101 indicates how the available user-I/O pins are distributed between the eight I/O banks for the XC3S400 in the FG456 package. Similarly, Table 102 shows how the available user-I/O pins are distributed between the eight I/O banks for the XC3S1000, XC3S1500, and XC3S2000 in the FG456 package.

Table 101: **User I/Os Per Bank for XC3S400 in FG456 Package**

Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	35	27	0	2	4	2
	1	35	27	0	2	4	2
Right	2	31	25	0	2	4	0
	3	31	25	0	2	4	0
Bottom	4	35	21	6	2	4	2
	5	35	21	6	2	4	2
Left	6	31	25	0	2	4	0
	7	31	25	0	2	4	0

Table 102: **User I/Os Per Bank for XC3S1000, XC3S1500, and XC3S2000 in FG456 Package**

Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	40	31	0	2	5	2
	1	40	31	0	2	5	2
Right	2	43	37	0	2	4	0
	3	43	37	0	2	4	0
Bottom	4	41	26	6	2	5	2
	5	40	25	6	2	5	2
Left	6	43	37	0	2	4	0
	7	43	37	0	2	4	0

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
4	IO_L22N_4/VREF_4	IO_L22N_4/VREF_4	IO_L22N_4/VREF_4	IO_L22N_4/VREF_4	IO_L22N_4/VREF_4	AD17	VREF
4	IO_L22P_4	IO_L22P_4	IO_L22P_4	IO_L22P_4	IO_L22P_4	AB17	I/O
4	N.C. (◆)	IO_L23N_4	IO_L23N_4	IO_L23N_4	IO_L23N_4	AE17	I/O
4	N.C. (◆)	IO_L23P_4	IO_L23P_4	IO_L23P_4	IO_L23P_4	AF17	I/O
4	IO_L24N_4	IO_L24N_4	IO_L24N_4	IO_L24N_4	IO_L24N_4	Y16	I/O
4	IO_L24P_4	IO_L24P_4	IO_L24P_4	IO_L24P_4	IO_L24P_4	AA16	I/O
4	IO_L25N_4	IO_L25N_4	IO_L25N_4	IO_L25N_4	IO_L25N_4	AB16	I/O
4	IO_L25P_4	IO_L25P_4	IO_L25P_4	IO_L25P_4	IO_L25P_4	AC16	I/O
4	N.C. (◆)	IO_L26N_4	IO_L26N_4	IO_L26N_4	IO_L26N_4	AE16	I/O
4	N.C. (◆)	IO_L26P_4/VREF_4	IO_L26P_4/VREF_4	IO_L26P_4/VREF_4	IO_L26P_4/VREF_4	AF16	VREF
4	IO_L27N_4/DIN/D0	IO_L27N_4/DIN/D0	IO_L27N_4/DIN/D0	IO_L27N_4/DIN/D0	IO_L27N_4/DIN/D0	Y15	DUAL
4	IO_L27P_4/D1	IO_L27P_4/D1	IO_L27P_4/D1	IO_L27P_4/D1	IO_L27P_4/D1	W14	DUAL
4	IO_L28N_4	IO_L28N_4	IO_L28N_4	IO_L28N_4	IO_L28N_4	AA15	I/O
4	IO_L28P_4	IO_L28P_4	IO_L28P_4	IO_L28P_4	IO_L28P_4	AB15	I/O
4	IO_L29N_4	IO_L29N_4	IO_L29N_4	IO_L29N_4	IO_L29N_4	AE15	I/O
4	IO_L29P_4	IO_L29P_4	IO_L29P_4	IO_L29P_4	IO_L29P_4	AF15	I/O
4	IO_L30N_4/D2	IO_L30N_4/D2	IO_L30N_4/D2	IO_L30N_4/D2	IO_L30N_4/D2	Y14	DUAL
4	IO_L30P_4/D3	IO_L30P_4/D3	IO_L30P_4/D3	IO_L30P_4/D3	IO_L30P_4/D3	AA14	DUAL
4	IO_L31N_4/INIT_B	IO_L31N_4/INIT_B	IO_L31N_4/INIT_B	IO_L31N_4/INIT_B	IO_L31N_4/INIT_B	AC14	DUAL
4	IO_L31P_4/ DOUT/BUSY	IO_L31P_4/ DOUT/BUSY	IO_L31P_4/ DOUT/BUSY	IO_L31P_4/ DOUT/BUSY	IO_L31P_4/ DOUT/BUSY	AD14	DUAL
4	IO_L32N_4/GCLK1	IO_L32N_4/GCLK1	IO_L32N_4/GCLK1	IO_L32N_4/GCLK1	IO_L32N_4/GCLK1	AE14	GCLK
4	IO_L32P_4/GCLK0	IO_L32P_4/GCLK0	IO_L32P_4/GCLK0	IO_L32P_4/GCLK0	IO_L32P_4/GCLK0	AF14	GCLK
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	AD16	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	AD20	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	U14	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	V14	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	V15	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	V16	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	W17	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	W18	VCCO
5	IO	IO	IO	IO	IO	AA7	I/O
5	IO	IO	IO	IO	IO	AA13	I/O
5	IO	IO	IO	IO	IO_L17P_5[(3)]	AB9	I/O
5	N.C. (◆)	IO	IO	IO	IO_L17N_5[(3)]	AC9	I/O
5	IO	IO	IO	IO	IO	AC11	I/O
5	IO	IO	IO	IO	IO	AD10	I/O
5	IO	IO	IO	IO	IO	AD12	I/O
5	IO	IO	IO	IO	IO	AF4	I/O
5	IO	IO	IO	IO	IO	Y8	I/O
5	IO/VREF_5	IO/VREF_5	IO/VREF_5	IO/VREF_5	IO/VREF_5	AF5	VREF
5	IO/VREF_5	IO/VREF_5	IO/VREF_5	IO/VREF_5	IO/VREF_5	AF13	VREF
5	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	AC5	DUAL

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
7	IO_L29P_7	IO_L29P_7	IO_L29P_7	IO_L29P_7	IO_L29P_7	L2	I/O
7	IO_L31N_7	IO_L31N_7	IO_L31N_7	IO_L31N_7	IO_L31N_7	M7	I/O
7	IO_L31P_7	IO_L31P_7	IO_L31P_7	IO_L31P_7	IO_L31P_7	M8	I/O
7	IO_L32N_7	IO_L32N_7	IO_L32N_7	IO_L32N_7	IO_L32N_7	M6	I/O
7	IO_L32P_7	IO_L32P_7	IO_L32P_7	IO_L32P_7	IO_L32P_7	M5	I/O
7	IO_L33N_7	IO_L33N_7	IO_L33N_7	IO_L33N_7	IO_L33N_7	M3	I/O
7	IO_L33P_7	IO_L33P_7	IO_L33P_7	IO_L33P_7	IO_L33P_7	L4	I/O
7	IO_L34N_7	IO_L34N_7	IO_L34N_7	IO_L34N_7	IO_L34N_7	M1	I/O
7	IO_L34P_7	IO_L34P_7	IO_L34P_7	IO_L34P_7	IO_L34P_7	M2	I/O
7	IO_L35N_7	IO_L35N_7	IO_L35N_7	IO_L35N_7	IO_L35N_7	N7	I/O
7	IO_L35P_7	IO_L35P_7	IO_L35P_7	IO_L35P_7	IO_L35P_7	N8	I/O
7	IO_L38N_7	IO_L38N_7	IO_L38N_7	IO_L38N_7	IO_L38N_7	N5	I/O
7	IO_L38P_7	IO_L38P_7	IO_L38P_7	IO_L38P_7	IO_L38P_7	N6	I/O
7	IO_L39N_7	IO_L39N_7	IO_L39N_7	IO_L39N_7	IO_L39N_7	N3	I/O
7	IO_L39P_7	IO_L39P_7	IO_L39P_7	IO_L39P_7	IO_L39P_7	N4	I/O
7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	N1	VREF
7	IO_L40P_7	IO_L40P_7	IO_L40P_7	IO_L40P_7	IO_L40P_7	N2	I/O
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	G3	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	J8	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	K8	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	L3	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	L9	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	M9	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	N9	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	N10	VCCO
N/A	GND	GND	GND	GND	GND	A1	GND
N/A	GND	GND	GND	GND	GND	A26	GND
N/A	GND	GND	GND	GND	GND	AC4	GND
N/A	GND	GND	GND	GND	GND	AC12	GND
N/A	GND	GND	GND	GND	GND	AC15	GND
N/A	GND	GND	GND	GND	GND	AC23	GND
N/A	GND	GND	GND	GND	GND	AD3	GND
N/A	GND	GND	GND	GND	GND	AD24	GND
N/A	GND	GND	GND	GND	GND	AE2	GND
N/A	GND	GND	GND	GND	GND	AE25	GND
N/A	GND	GND	GND	GND	GND	AF1	GND
N/A	GND	GND	GND	GND	GND	AF26	GND
N/A	GND	GND	GND	GND	GND	B2	GND
N/A	GND	GND	GND	GND	GND	B25	GND
N/A	GND	GND	GND	GND	GND	C3	GND
N/A	GND	GND	GND	GND	GND	C24	GND
N/A	GND	GND	GND	GND	GND	D4	GND
N/A	GND	GND	GND	GND	GND	D12	GND

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
5	IO_L07N_5	IO_L07N_5	AK8	I/O
5	IO_L07P_5	IO_L07P_5	AJ8	I/O
5	IO_L08N_5	IO_L08N_5	AC9	I/O
5	IO_L08P_5	IO_L08P_5	AB9	I/O
5	IO_L09N_5	IO_L09N_5	AG9	I/O
5	IO_L09P_5	IO_L09P_5	AF9	I/O
5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	AK9	DCI
5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	AJ9	DCI
5	IO_L11N_5/VREF_5	IO_L11N_5/VREF_5	AE10	VREF
5	IO_L11P_5	IO_L11P_5	AE9	I/O
5	IO_L12N_5	IO_L12N_5	AJ10	I/O
5	IO_L12P_5	IO_L12P_5	AH10	I/O
5	IO_L13N_5	IO_L13N_5	AD11	I/O
5	IO_L13P_5	IO_L13P_5	AD10	I/O
5	IO_L14N_5	IO_L14N_5	AF11	I/O
5	IO_L14P_5	IO_L14P_5	AE11	I/O
5	IO_L15N_5	IO_L15N_5	AH11	I/O
5	IO_L15P_5	IO_L15P_5	AG11	I/O
5	IO_L16N_5	IO_L16N_5	AK11	I/O
5	IO_L16P_5	IO_L16P_5	AJ11	I/O
5	IO_L17N_5	IO_L17N_5	AB12	I/O
5	IO_L17P_5	IO_L17P_5	AC11	I/O
5	IO_L18N_5	IO_L18N_5	AD12	I/O
5	IO_L18P_5	IO_L18P_5	AC12	I/O
5	IO_L19N_5	IO_L19N_5	AF12	I/O
5	IO_L19P_5/VREF_5	IO_L19P_5/VREF_5	AE12	VREF
5	IO_L20N_5	IO_L20N_5	AH12	I/O
5	IO_L20P_5	IO_L20P_5	AG12	I/O
5	IO_L21N_5	IO_L21N_5	AK12	I/O
5	IO_L21P_5	IO_L21P_5	AJ12	I/O
5	IO_L22N_5	IO_L22N_5	AA13	I/O
5	IO_L22P_5	IO_L22P_5	AA12	I/O
5	IO_L23N_5	IO_L23N_5	AC13	I/O
5	IO_L23P_5	IO_L23P_5	AB13	I/O
5	IO_L24N_5	IO_L24N_5	AG13	I/O
5	IO_L24P_5	IO_L24P_5	AF13	I/O
5	IO_L25N_5	IO_L25N_5	AK13	I/O
5	IO_L25P_5	IO_L25P_5	AJ13	I/O
5	IO_L26N_5	IO_L26N_5	AB14	I/O
5	IO_L26P_5	IO_L26P_5	AA14	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	AE14	VREF
5	IO_L27P_5	IO_L27P_5	AE13	I/O
5	IO_L28N_5/D6	IO_L28N_5/D6	AJ14	DUAL
5	IO_L28P_5/D7	IO_L28P_5/D7	AH14	DUAL
5	IO_L29N_5	IO_L29N_5	AC15	I/O
5	IO_L29P_5/VREF_5	IO_L29P_5/VREF_5	AB15	VREF
5	IO_L30N_5	IO_L30N_5	AD15	I/O
5	IO_L30P_5	IO_L30P_5	AD14	I/O
5	IO_L31N_5/D4	IO_L31N_5/D4	AG15	DUAL
5	IO_L31P_5/D5	IO_L31P_5/D5	AF15	DUAL
5	IO_L32N_5/GCLK3	IO_L32N_5/GCLK3	AJ15	GCLK
5	IO_L32P_5/GCLK2	IO_L32P_5/GCLK2	AH15	GCLK
5	N.C. (◆)	IO_L35N_5	AK7	I/O
5	N.C. (◆)	IO_L35P_5	AJ7	I/O
5	N.C. (◆)	IO_L36N_5	AD8	I/O
5	N.C. (◆)	IO_L36P_5	AC8	I/O
5	N.C. (◆)	IO_L37N_5	AF8	I/O
5	N.C. (◆)	IO_L37P_5	AE8	I/O
5	N.C. (◆)	IO_L38N_5	AH8	I/O
5	N.C. (◆)	IO_L38P_5	AG8	I/O
5	VCCO_5	VCCO_5	AH5	VCCO
5	VCCO_5	VCCO_5	AF7	VCCO
5	VCCO_5	VCCO_5	AD9	VCCO
5	VCCO_5	VCCO_5	AH9	VCCO
5	VCCO_5	VCCO_5	AB11	VCCO
5	VCCO_5	VCCO_5	Y12	VCCO
5	VCCO_5	VCCO_5	Y13	VCCO
5	VCCO_5	VCCO_5	AD13	VCCO
5	VCCO_5	VCCO_5	AH13	VCCO
5	VCCO_5	VCCO_5	Y14	VCCO
6	IO	IO	AB6	I/O
6	IO_L01N_6/VRP_6	IO_L01N_6/VRP_6	AH2	DCI
6	IO_L01P_6/VRN_6	IO_L01P_6/VRN_6	AH1	DCI
6	IO_L02N_6	IO_L02N_6	AG4	I/O
6	IO_L02P_6	IO_L02P_6	AG3	I/O
6	IO_L03N_6/VREF_6	IO_L03N_6/VREF_6	AG2	VREF
6	IO_L03P_6	IO_L03P_6	AG1	I/O
6	IO_L04N_6	IO_L04N_6	AF2	I/O
6	IO_L04P_6	IO_L04P_6	AF1	I/O
6	IO_L05N_6	IO_L05N_6	AF4	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
3	IO_L48P_3	IO_L48P_3	AB24	I/O
3	N.C. (◆)	IO_L49N_3	AA26	I/O
3	N.C. (◆)	IO_L49P_3	AA25	I/O
3	IO_L50N_3	IO_L50N_3	Y25	I/O
3	IO_L50P_3	IO_L50P_3	Y24	I/O
3	N.C. (◆)	IO_L51N_3	V24	I/O
3	N.C. (◆)	IO_L51P_3	W24	I/O
3	VCCO_3	VCCO_3	AA23	VCCO
3	VCCO_3	VCCO_3	AB23	VCCO
3	VCCO_3	VCCO_3	AB29	VCCO
3	VCCO_3	VCCO_3	AB33	VCCO
3	VCCO_3	VCCO_3	AD27	VCCO
3	VCCO_3	VCCO_3	AD31	VCCO
3	VCCO_3	VCCO_3	AG28	VCCO
3	VCCO_3	VCCO_3	AG32	VCCO
3	VCCO_3	VCCO_3	AL32	VCCO
3	VCCO_3	VCCO_3	W23	VCCO
3	VCCO_3	VCCO_3	W31	VCCO
3	VCCO_3	VCCO_3	Y23	VCCO
3	VCCO_3	VCCO_3	Y27	VCCO
4	IO	IO	AD18	I/O
4	IO	IO	AD19	I/O
4	IO	IO	AD20	I/O
4	IO	IO	AD22	I/O
4	IO	IO	AE18	I/O
4	IO	IO	AE19	I/O
4	IO	IO	AE22	I/O
4	N.C. (◆)	IO	AE24	I/O
4	IO	IO	AF24	I/O
4	N.C. (◆)	IO	AF26	I/O
4	IO	IO	AG26	I/O
4	IO	IO	AG27	I/O
4	IO	IO	AJ27	I/O
4	IO	IO	AJ29	I/O
4	IO	IO	AK25	I/O
4	IO	IO	AN26	I/O
4	IO/VREF_4	IO/VREF_4	AF21	VREF
4	IO/VREF_4	IO/VREF_4	AH23	VREF
4	IO/VREF_4	IO/VREF_4	AK18	VREF
4	IO/VREF_4	IO/VREF_4	AL30	VREF