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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	192
Number of Logic Elements/Cells	1728
Total RAM Bits	73728
Number of I/O	97
Number of Gates	50000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s50-5tqg144c

Table 8: **Single-Ended I/O Standards**

Signal Standard (IOSTANDARD)	V_{CCO} (Volts)		V_{REF} for Inputs (Volts)[1]	Board Termination Voltage (V_{TT}) in Volts
	For Outputs	For Inputs		
GTL	Note 2	Note 2	0.8	1.2
GTLP	Note 2	Note 2	1	1.5
HSTL_I	1.5	–	0.75	0.75
HSTL_III	1.5	–	0.9	1.5
HSTL_I_18	1.8	–	0.9	0.9
HSTL_II_18	1.8	–	0.9	0.9
HSTL_III_18	1.8	–	1.1	1.8
LVCMOS12	1.2	1.2	–	–
LVCMOS15	1.5	1.5	–	–
LVCMOS18	1.8	1.8	–	–
LVCMOS25	2.5	2.5	–	–
LVCMOS33	3.3	3.3	–	–
LVTTL	3.3	3.3	–	–
PCI33_3	3.0	3.0	–	–
SSTL18_I	1.8	–	0.9	0.9
SSTL18_II	1.8	–	0.9	0.9
SSTL2_I	2.5	–	1.25	1.25
SSTL2_II	2.5	–	1.25	1.25

Notes:

1. Banks 4 and 5 of any Spartan-3 device in a VQ100 package do not support signal standards using V_{REF}.
2. The V_{CCO} level used for the GTL and GTLP standards must be no lower than the termination voltage (V_{TT}), nor can it be lower than the voltage at the I/O pad.
3. See Table 10 for a listing of the single-ended DCI standards.

Differential standards employ a pair of signals, one the opposite polarity of the other. The noise canceling (e.g., Common-Mode Rejection) properties of these standards permit exceptionally high data transfer rates. This section introduces the differential signaling capabilities of Spartan-3 devices.

Each device-package combination designates specific I/O pairs that are specially optimized to support differential standards. A unique "L-number", part of the pin name, identifies the line-pairs associated with each bank (see Figure 40, page 112). For each pair, the letters 'P' and 'N' designate the true and inverted lines, respectively. For example, the pin names IO_L43P_7 and IO_L43N_7 indicate the true and inverted lines comprising the line pair L43 on Bank 7. The V_{CCO} lines provide current to the outputs. The V_{CCAUX} lines supply power to the differential inputs, making them independent of the V_{CCO} voltage for an I/O bank. The V_{REF} lines are not used. Select the V_{CCO} level to suit the desired differential standard according to Table 9.

The DCI feature operates independently for each of the device's eight banks. Each bank has an 'N' reference pin (VRN) and a 'P' reference pin, (VRP), to calibrate driver and termination resistance. Only when using a DCI standard on a given bank do these two pins function as VRN and VRP. When not using a DCI standard, the two pins function as user I/Os. As shown in Figure 9, add an external reference resistor to pull the VRN pin up to V_{CCO} and another reference resistor to pull the VRP pin down to GND. Also see Figure 42, page 116. Both resistors have the same value—commonly 50Ω—with one-percent tolerance, which is either the characteristic impedance of the line or twice that, depending on the DCI standard in use. Standards having a symbol name that contains the letters "DV2" use a reference resistor value that is twice the line impedance. DCI adjusts the output driver impedance to match the reference resistors' value or half that, according to the standard. DCI always adjusts the on-chip termination resistors to directly match the reference resistors' value.

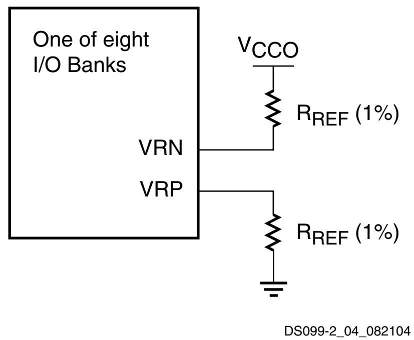


Figure 9: **Connection of Reference Resistors (R_{REF})**

The rules guiding the use of DCI standards on banks are as follows:

- No more than one DCI I/O standard with a Single Termination is allowed per bank.
- No more than one DCI I/O standard with a Split Termination is allowed per bank.
- Single Termination, Split Termination, Controlled- Impedance Driver, and Controlled-Impedance Driver with Half Impedance can co-exist in the same bank.

See also The Organization of IOBs into Banks, immediately below, and DCI: User I/O or Digitally Controlled Impedance Resistor Reference Input, page 115.

The Organization of IOBs into Banks

IOBs are allocated among eight banks, so that each side of the device has two banks, as shown in Figure 10. For all packages, each bank has independent V_{REF} lines. For example, V_{REF} Bank 3 lines are separate from the V_{REF} lines going to all other banks.

For the Very Thin Quad Flat Pack (VQ), Plastic Quad Flat Pack (PQ), Fine Pitch Thin Ball Grid Array (FT), and Fine Pitch Ball Grid Array (FG) packages, each bank has dedicated V_{CCO} lines. For example, the V_{CCO} Bank 7 lines are separate from the V_{CCO} lines going to all other banks. Thus, Spartan-3 devices in these packages support eight independent V_{CCO} supplies.

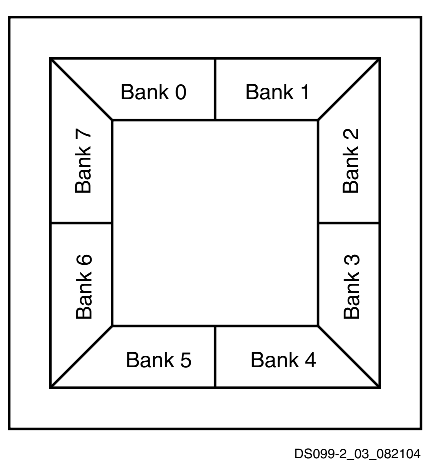
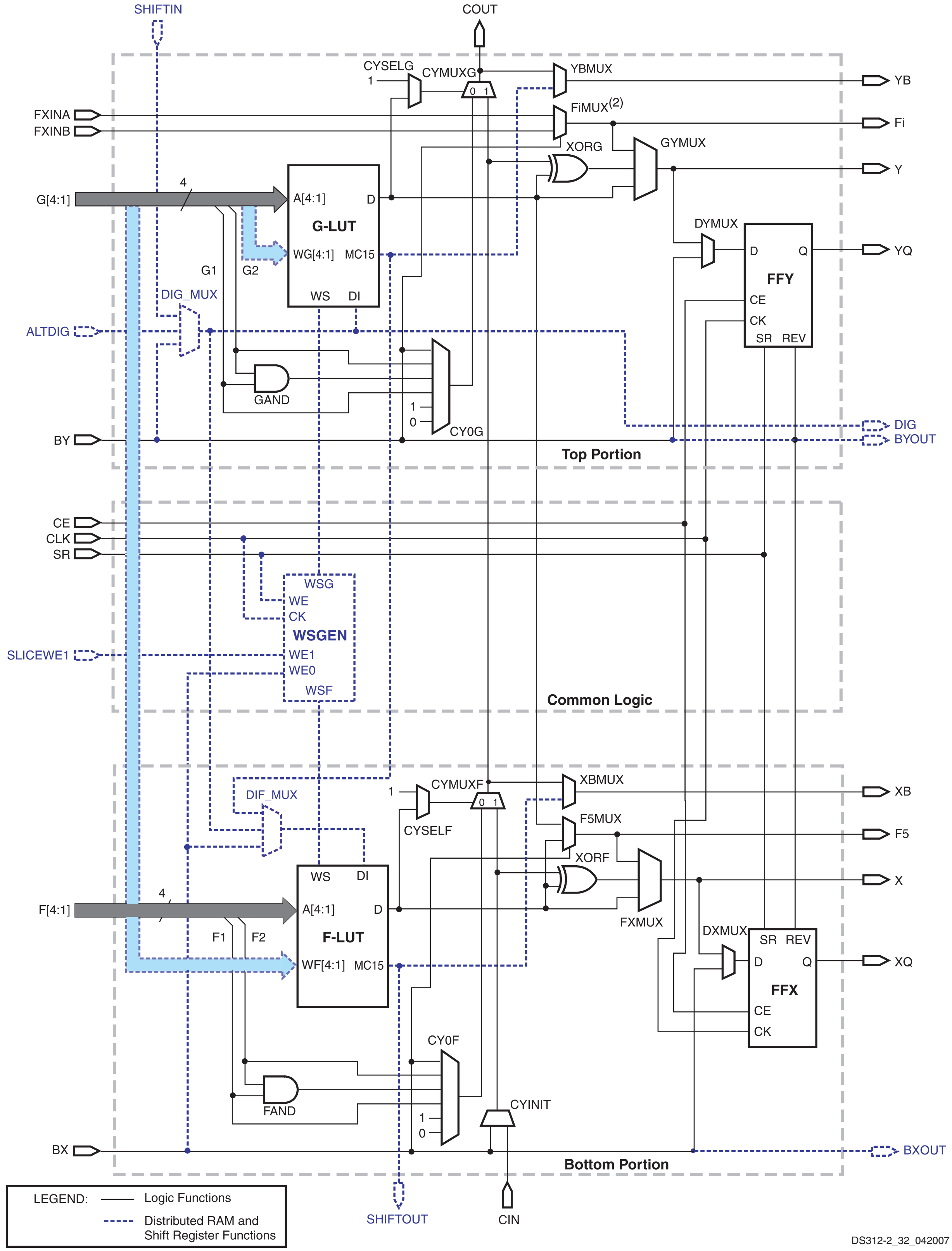


Figure 10: **Spartan-3 FPGA I/O Banks (Top View)**



Notes:

1. Options to invert signal polarity as well as other options that enable lines for various functions are not shown.
2. The index i can be 6, 7, or 8, depending on the slice. In this position, the upper right-hand slice has an F8MUX, and the upper left-hand slice has an F7MUX. The lower right-hand and left-hand slices both have an F6MUX.

Figure 12: **Simplified Diagram of the Left-Hand SLICEM**

Arrangement of RAM Blocks on Die

The XC3S50 has one column of block RAM. The Spartan-3 devices ranging from the XC3S200 to XC3S2000 have two columns of block RAM. The XC3S4000 and XC3S5000 have four columns. The position of the columns on the die is shown in Figure 1, page 3. For a given device, the total available RAM blocks are distributed equally among the columns. Table 12 shows the number of RAM blocks, the data storage capacity, and the number of columns for each device.

Table 12: **Number of RAM Blocks by Device**

Device	Total Number of RAM Blocks	Total Addressable Locations (Bits)	Number of Columns
XC3S50	4	73,728	1
XC3S200	12	221,184	2
XC3S400	16	294,912	2
XC3S1000	24	442,368	2
XC3S1500	32	589,824	2
XC3S2000	40	737,280	2
XC3S4000	96	1,769,472	4
XC3S5000	104	1,916,928	4

Block RAM and multipliers have interconnects between them that permit simultaneous operation; however, since the multiplier shares inputs with the upper data bits of block RAM, the maximum data path width of the block RAM is 18 bits in this case.

The Internal Structure of the Block RAM

The block RAM has a dual port structure. The two identical data ports called A and B permit independent access to the common RAM block, which has a maximum capacity of 18,432 bits—or 16,384 bits when no parity lines are used. Each port has its own dedicated set of data, control and clock lines for synchronous read and write operations. There are four basic data paths, as shown in Figure 13: (1) write to and read from Port A, (2) write to and read from Port B, (3) data transfer from Port A to Port B, and (4) data transfer from Port B to Port A.

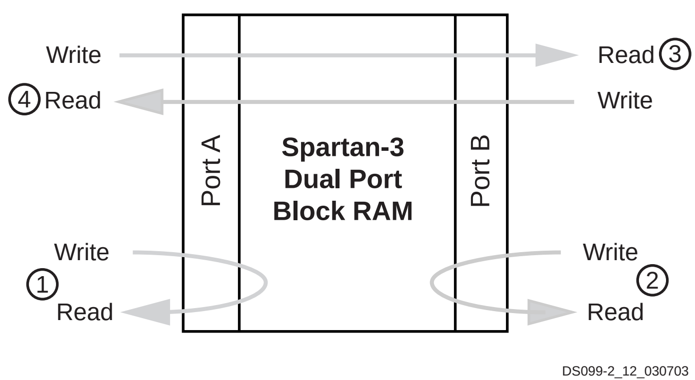
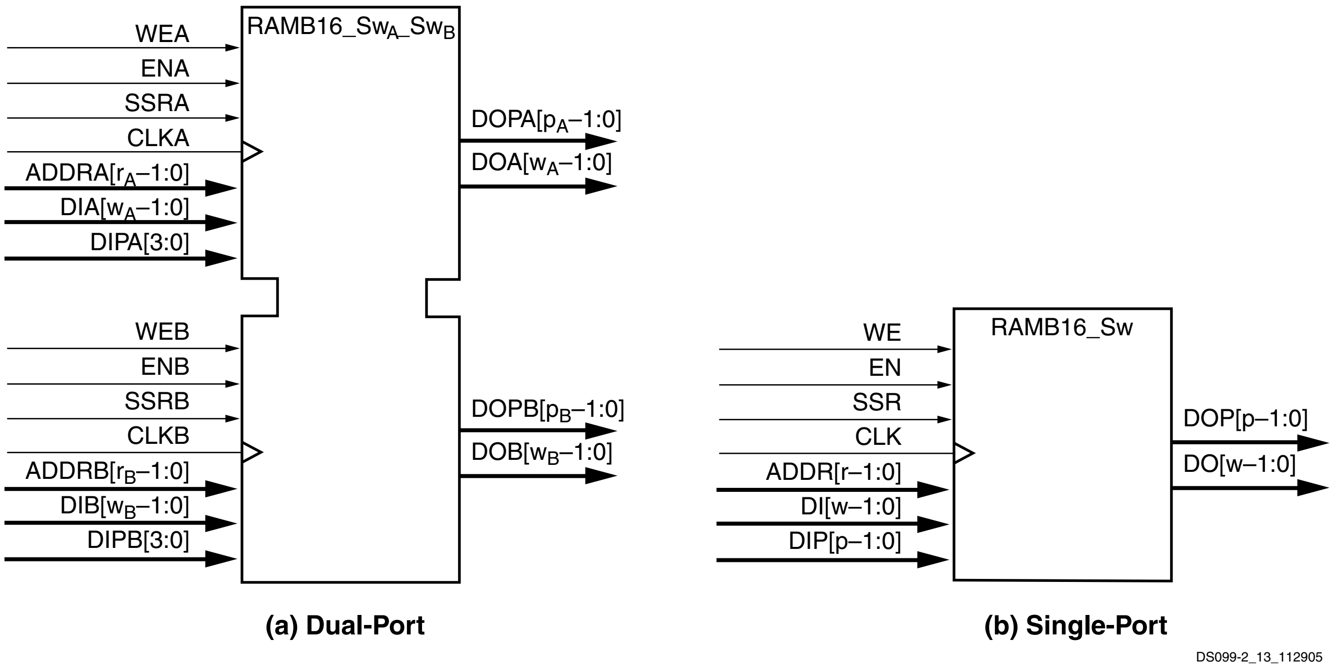


Figure 13: **Block RAM Data Paths**

Block RAM Port Signal Definitions

Representations of the dual-port primitive RAMB16_S[w_A]_S[w_B] and the single-port primitive RAMB16_S[w] with their associated signals are shown in Figure 14. These signals are defined in Table 13.



Notes:

1. w_A and w_B are integers representing the total data path width (i.e., data bits plus parity bits) at ports A and B, respectively.
2. p_A and p_B are integers that indicate the number of data path lines serving as parity bits.
3. r_A and r_B are integers representing the address bus width at ports A and B, respectively.
4. The control signals CLK, WE, EN, and SSR on both ports have the option of inverted polarity.

Figure 14: **Block RAM Primitives**

Table 13: **Block RAM Port Signals**

Signal Description	Port A Signal Name	Port B Signal Name	Direction	Function
Address Bus	ADDRA	ADDRB	Input	The Address Bus selects a memory location for read or write operations. The width (w) of the port's associated data path determines the number of available address lines (r). Whenever a port is enabled (ENA or ENB = High), address transitions must meet the data sheet setup and hold times with respect to the port clock (CLKA or CLKB). This requirement must be met, even if the RAM read output is of no interest.
Data Input Bus	DIA	DIB	Input	Data at the DI input bus is written to the addressed memory location addressed on an enabled active CLK edge. It is possible to configure a port's total data path width (w) to be 1, 2, 4, 9, 18, or 36 bits. This selection applies to both the DI and DO paths of a given port. Each port is independent. For a port assigned a width (w), the number of addressable locations is 16,384/(w-p) where "p" is the number of parity bits. Each memory location has a width of "w" (including parity bits). See the DIP signal description for more information of parity.
Parity Data Input(s)	DIPA	DIPB	Input	Parity inputs represent additional bits included in the data input path to support error detection. The number of parity bits "p" included in the DI (same as for the DO bus) depends on a port's total data path width (w). See Table 14.

Each BUFGMUX element, shown in Figure 24, is a 2-to-1 multiplexer that can receive signals from any of the four following sources:

- One of the four Global Clock inputs on the same side of the die—top or bottom—as the BUFGMUX element in use.
- Any of four nearby horizontal Double lines.
- Any of four outputs from the DCM in the right-hand quadrant that is on the same side of the die as the BUFGMUX element in use.
- Any of four outputs from the DCM in the left-hand quadrant that is on the same side of the die as the BUFGMUX element in use.

The multiplexer select line, S, chooses which of the two inputs, I0 or I1, drives the BUFGMUX's output signal, O, as described in Table 25. The switching from one clock to the other is glitchless, and done in such a way that the output High and Low times are never shorter than the shortest High or Low time of either input clock.

Table 25: **BUFGMUX Select Mechanism**

S Input	O Output
0	I0 Input
1	I1 Input

The two clock inputs can be asynchronous with regard to each other, and the S input can change at any time, except for a short setup time prior to the rising edge of the presently selected clock (I0 or I1). Violating this setup time requirement can result in an undefined runt pulse output.

The BUFG clock buffer primitive drives a single clock signal onto the clock network and is essentially the same element as a BUFGMUX, just without the clock select mechanism. Similarly, the BUFGCE primitive creates an enabled clock buffer using the BUFGMUX select mechanism.

Each BUFGMUX buffers incoming clock signals to two possible destinations:

- The vertical spine belonging to the same side of the die—top or bottom—as the BUFGMUX element in use. The two spines—top and bottom—each comprise four vertical clock lines, each running from one of the BUFGMUX elements on the same side towards the center of the die. At the center of the die, clock signals reach the eight-line horizontal spine, which spans the width of the die. In turn, the horizontal spine branches out into a subsidiary clock interconnect that accesses the CLBs.
- The clock input of either DCM on the same side of the die—top or bottom—as the BUFGMUX element in use.

Use either a BUFGMUX element or a BUFG (Global Clock Buffer) element to place a Global input in the design. For the purpose of minimizing the dynamic power dissipation of the clock network, the Xilinx development software automatically disables all clock line segments that a design does not use.

A global clock line ideally drives clock inputs on the various clocked elements within the FPGA, such as CLB or IOB flip-flops or block RAMs. A global clock line also optionally drives combinatorial inputs. However, doing so provides additional loading on the clock line that might also affect clock jitter. Ideally, drive combinatorial inputs using the signal that also drives the input to the BUFGMUX or BUFG element.

For more details, refer to the chapter entitled "Using Global Clock Resources" in UG331.

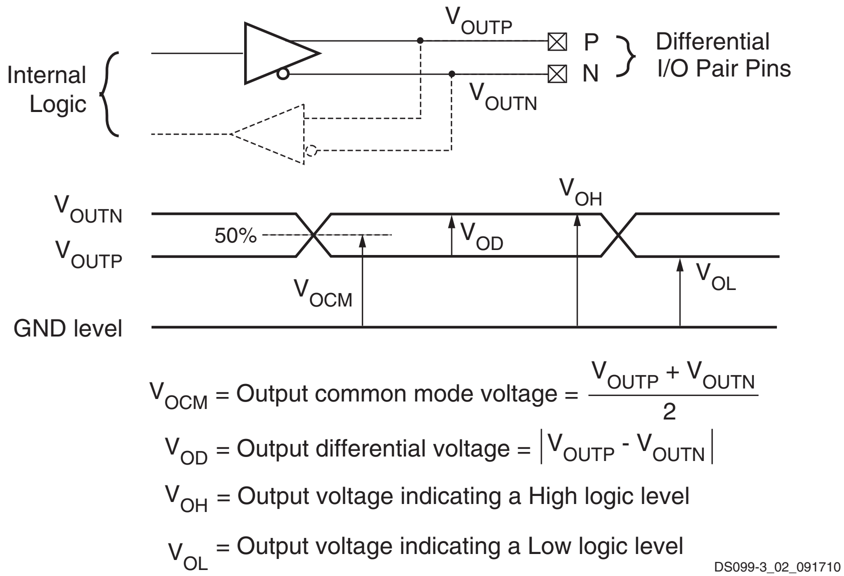


Figure 33: **Differential Output Voltages**

Table 38: **DC Characteristics of User I/Os Using Differential Signal Standards**

Signal Standard	Mask[3] Revision	V_{OD}			V_{OCM}			V_{OH}	V_{OL}
		Min (mV)	Typ (mV)	Max (mV)	Min (V)	Typ (V)	Max (V)	Min (V)	Max (V)
LDT_25 (ULVDS_25)	All	430[4]	600	670	0.495	0.600	0.715	0.71	0.50
LVDS_25	All	100	–	600	0.80	–	1.6	0.85	1.55
	'E'	200	–	500	1.0	–	1.5	1.10	1.40
BLVDS_25[5]	All	250	350	450	–	1.20	–	–	–
LVDSEXT_25	All	100	–	600	0.80	–	1.6	0.85	1.55
	'E'	300	–	700	1.0	–	1.5	1.15	1.35
LVPECL_25[5]	All	–	–	-	–	–	-	1.35	1.005
RSDS_25[6]	All	100	–	600	0.80	–	1.6	0.85	1.55
	'E'	200	–	500	1.0	–	1.5	1.10	1.40
DIFF_HSTL_II_18	All	–	–	–	–	–	–	$V_{CCO} - 0.40$	0.40
DIFF_SSTL2_II	All	–	–	–	–	–	–	$V_{TT} + 0.80$	$V_{TT} - 0.80$

Notes:

1. The numbers in this table are based on the conditions set forth in Table 32 and Table 37.
2. Output voltage measurements for all differential standards are made with a termination resistor (R_T) of 100Ω across the N and P pins of the differential signal pair.
3. Mask revision E devices have tighter output ranges but can be used in any design that was in a previous revision. See Mask and Fab Revisions, page 58.
4. This value must be compatible with the receiver to which the FPGA's output pair is connected.
5. Each LVPECL_25 or BLVDS_25 output-pair requires three external resistors for proper output operation as shown in Figure 34. Each LVPECL_25 or BLVDS_25 input-pair uses a 100W termination resistor at the receiver.
6. Only one of the differential standards RSDS_25, LDT_25, LVDS_25, and LVDSEXT_25 may be used for outputs within a bank. Each differential standard input-pair requires an external 100Ω termination resistor.

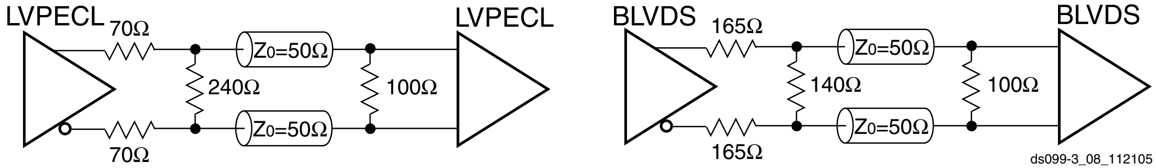


Figure 34: **External Termination Required for LVPECL and BLVDS Output and Input**

Table 45: **Timing for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade -5 Max[3]	Speed Grade -4 Max[3]	Units
Clock-to-Output Times						
T_{IOCKP}	When reading from the Output Flip-Flop (OFF), the time from the active transition at the OTCLK input to data appearing at the Output pin	LVCMOS25[2], 12 mA output drive, Fast slew rate	XC3S200 XC3S400	1.28	1.47	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	1.95	2.24	ns
Propagation Times						
T_{IOOP}	The time it takes for data to travel from the IOB's O input to the Output pin	LVCMOS25[2], 12 mA output drive, Fast slew rate	XC3S200 XC3S400	1.28	1.46	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	1.94	2.23	ns
T_{IOOLP}	The time it takes for data to travel from the O input through the OFF latch to the Output pin		XC3S200 XC3S400	1.28	1.47	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	1.95	2.24	ns
Set/Reset Times						
T_{IOSRP}	Time from asserting the OFF's SR input to setting/resetting data at the Output pin	LVCMOS25[2], 12 mA output drive, Fast slew rate	XC3S200 XC3S400	2.10	2.41	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	2.77	3.18	ns
T_{IOGSRQ}	Time from asserting the Global Set Reset (GSR) net to setting/resetting data at the Output pin		All	8.07	9.28	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32 and Table 35.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 47.
3. For minimums, use the values reported by the Xilinx timing analyzer.

Table 48: **Test Methods for Timing Measurement at I/Os *(Cont'd)***

Signal Standard (IOSTANDARD)		Inputs			Outputs		Inputs and Outputs
		V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
HSTL_III_18		1.1	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	1.8	V_{REF}
HSTL_III_DCI_18							
LVCMOS12		-	0	1.2	1M	0	0.6
LVCMOS15		-	0	1.5	1M	0	0.75
LVDCI_15							
LVDCI_DV2_15							
HSLVDCI_15							
LVCMOS18		-	0	1.8	1M	0	0.9
LVDCI_18							
LVDCI_DV2_18							
HSLVDCI_18							
LVCMOS25		-	0	2.5	1M	0	1.25
LVDCI_25							
LVDCI_DV2_25							
HSLVDCI_25							
LVCMOS33		-	0	3.3	1M	0	1.65
LVDCI_33							
LVDCI_DV2_33							
HSLVDCI_33							
LVTTL		-	0	3.3	1M	0	1.4
PCI33_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
SSTL18_I		0.9	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	0.9	V_{REF}
SSTL18_I_DCI							
SSTL18_II		0.9	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	0.9	V_{REF}
SSTL2_I		1.25	$V_{REF} - 0.75$	$V_{REF} + 0.75$	50	1.25	V_{REF}
SSTL2_I_DCI							
SSTL2_II		1.25	$V_{REF} - 0.75$	$V_{REF} + 0.75$	25	1.25	V_{REF}
SSTL2_II_DCI					50	1.25	
Differential							
LDT_25 (ULVDS_25)		-	$V_{ICM} - 0.125$	$V_{ICM} + 0.125$	60	0.6	V_{ICM}
LVDS_25		-	$V_{ICM} - 0.125$	$V_{ICM} + 0.125$	50	1.2	V_{ICM}
LVDS_25_DCI					N/A	N/A	
BLVDS_25		-	$V_{ICM} - 0.125$	$V_{ICM} + 0.125$	1M	0	V_{ICM}
LVDSEXT_25		-	$V_{ICM} - 0.125$	$V_{ICM} + 0.125$	50	1.2	V_{ICM}
LVDSEXT_25_DCI					N/A	N/A	
LVPECL_25		-	$V_{ICM} - 0.3$	$V_{ICM} + 0.3$	1M	0	V_{ICM}
RSDS_25		-	$V_{ICM} - 0.1$	$V_{ICM} + 0.1$	50	1.2	V_{ICM}
DIFF_HSTL_II_18		-	$V_{ICM} - 0.5$	$V_{ICM} + 0.5$	50	1.8	V_{ICM}
DIFF_HSTL_II_18_DCI							

Table 52: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	-5		-4		Units
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{SHCKO}	Time from the active edge at the CLK input to data appearing on the distributed RAM output	–	1.87	–	2.15	ns
Setup Times						
T_{DS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the distributed RAM	0.46	–	0.52	–	ns
T_{AS}	Setup time of the F/G address inputs before the active transition at the CLK input of the distributed RAM	0.46	–	0.53	–	ns
T_{WS}	Setup time of the write enable input before the active transition at the CLK input of the distributed RAM	0.33	–	0.37	–	ns
Hold Times						
T_{DH}, T_{AH}, T_{WH}	Hold time of the BX, BY data inputs, the F/G address inputs, or the write enable input after the active transition at the CLK input of the distributed RAM	0	–	0	–	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.85	–	0.97	–	ns

Table 53: **CLB Shift Register Switching Characteristics**

Symbol	Description	-5		-4		Units
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{REG}	Time from the active edge at the CLK input to data appearing on the shift register output	–	3.30	–	3.79	ns
Setup Times						
T_{SRLDS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the shift register	0.46	–	0.52	–	ns
Hold Times						
T_{SRLDH}	Hold time of the BX or BY data input after the active transition at the CLK input of the shift register	0	–	0	–	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.85	–	0.97	–	ns

Table 85: **Maximum User I/Os by Package**

Device	Package	Maximum User I/Os	Maximum Differential Pairs	All Possible I/O Pins by Type					N.C.
				I/O	DUAL	DCI	VREF	GCLK	
XC3S50	VQ100	63	29	22	12	14	7	8	0
XC3S200	VQ100	63	29	22	12	14	7	8	0
XC3S50	CP132[(1)]	89	44	44	12	14	11	8	0
XC3S50	TQ144	97	46	51	12	14	12	8	0
XC3S200	TQ144	97	46	51	12	14	12	8	0
XC3S400	TQ144	97	46	51	12	14	12	8	0
XC3S50	PQ208	124	56	72	12	16	16	8	17
XC3S200	PQ208	141	62	83	12	16	22	8	0
XC3S400	PQ208	141	62	83	12	16	22	8	0
XC3S200	FT256	173	76	113	12	16	24	8	0
XC3S400	FT256	173	76	113	12	16	24	8	0
XC3S1000	FT256	173	76	113	12	16	24	8	0
XC3S400	FG320	221	100	156	12	16	29	8	0
XC3S1000	FG320	221	100	156	12	16	29	8	0
XC3S1500	FG320	221	100	156	12	16	29	8	0
XC3S400	FG456	264	116	196	12	16	32	8	69
XC3S1000	FG456	333	149	261	12	16	36	8	0
XC3S1500	FG456	333	149	261	12	16	36	8	0
XC3S2000	FG456	333	149	261	12	16	36	8	0
XC3S1000	FG676	391	175	315	12	16	40	8	98
XC3S1500	FG676	487	221	403	12	16	48	8	2
XC3S2000	FG676	489	221	405	12	16	48	8	0
XC3S4000	FG676	489	221	405	12	16	48	8	0
XC3S5000	FG676	489	221	405	12	16	48	8	0
XC3S2000	FG900	565	270	481	12	16	48	8	68
XC3S4000	FG900	633	300	549	12	16	48	8	0
XC3S5000	FG900	633	300	549	12	16	48	8	0
XC3S4000	FG1156[(1)]	712	312	621	12	16	55	8	73
XC3S5000	FG1156[(1)]	784	344	692	12	16	56	8	1

Notes:

1. The CP132, CPG132, FG1156, and FGG1156 packages are discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

Electronic versions of the package pinout tables and footprints are available for download from the Xilinx website. Using a spreadsheet program, the data can be sorted and reformatted according to any specific needs. Similarly, the ASCII-text file is easily parsed by most scripting programs. Download the files from the following location:

http://www.xilinx.com/support/documentation/data_sheets/s3_pin.zip

Package Thermal Characteristics

The power dissipated by an FPGA application has implications on package selection and system design. The power consumed by a Spartan-3 FPGA is reported using either the XPower Estimator (XPE) or the XPower Analyzer integrated in the Xilinx ISE development software. Table 86 provides the thermal characteristics for the various Spartan-3 device/package offerings.

The junction-to-case thermal resistance (θ_{JC}) indicates the difference between the temperature measured on the package body (case) and the die junction temperature per watt of power consumption. The junction-to-board (θ_{JB}) value similarly reports the difference between the board and junction temperature. The junction-to-ambient (θ_{JA}) value reports the temperature difference per watt between the ambient environment and the junction temperature. The θ_{JA} value is reported at different air velocities, measured in linear feet per minute (LFM). The "Still Air (0 LFM)" column shows the θ_{JA} value in a system without a fan. The thermal resistance drops with increasing air flow.

Table 86: **Spartan-3 FPGA Package Thermal Characteristics**

Package	Device	Junction-to-Case (θ_{JC})	Junction-to-Board (θ_{JB})	Junction-to-Ambient (θ_{JA}) at Different Air Flows				Units
				Still Air (0 LFM)	250 LFM	500 LFM	750 LFM	
VQ(G)100	XC3S50	12.0	–	46.2	38.4	35.8	34.9	°C/Watt
	XC3S200	10.0	–	40.5	33.7	31.3	30.5	°C/Watt
CP(G)132[(1)]	XC3S50	14.5	32.8	53.0	46.4	44.0	42.5	°C/Watt
TQ(G)144	XC3S50	7.6	–	41.0	31.9	27.2	25.6	°C/Watt
	XC3S200	6.6	–	34.5	26.9	23.0	21.6	°C/Watt
	XC3S400	6.1	–	32.8	25.5	21.8	20.4	°C/Watt
PQ(G)208	XC3S50	10.6	–	37.4	27.6	24.4	22.6	°C/Watt
	XC3S200	8.6	–	36.2	26.7	23.6	21.9	°C/Watt
	XC3S400	7.5	–	35.4	26.1	23.1	21.4	°C/Watt
FT(G)256	XC3S200	9.9	22.9	31.7	25.6	24.5	24.2	°C/Watt
	XC3S400	7.9	19.0	28.4	22.8	21.5	21.0	°C/Watt
	XC3S1000	5.6	14.7	24.8	19.2	18.0	17.5	°C/Watt
FG(G)320	XC3S400	8.9	13.9	24.4	19.0	17.8	17.0	°C/Watt
	XC3S1000	7.8	11.8	22.3	17.0	15.8	15.0	°C/Watt
	XC3S1500	6.7	9.8	20.3	15.18	13.8	13.1	°C/Watt
FG(G)456	XC3S400	8.4	13.6	20.8	15.1	13.9	13.4	°C/Watt
	XC3S1000	6.4	10.6	19.3	13.4	12.3	11.7	°C/Watt
	XC3S1500	4.9	8.3	18.3	12.4	11.2	10.7	°C/Watt
	XC3S2000	3.7	6.5	17.7	11.7	10.5	10.0	°C/Watt
FG(G)676	XC3S1000	6.0	10.4	17.9	13.7	12.6	12.0	°C/Watt
	XC3S1500	4.9	8.8	16.8	12.4	11.3	10.7	°C/Watt
	XC3S2000	4.1	7.9	15.6	11.1	9.9	9.3	°C/Watt
	XC3S4000	3.6	7.0	15.0	10.5	9.3	8.7	°C/Watt
	XC3S5000	3.4	6.3	14.7	10.3	9.1	8.5	°C/Watt
FG(G)900	XC3S2000	3.7	7.0	14.3	10.3	9.3	8.8	°C/Watt
	XC3S4000	3.3	6.4	13.6	9.7	8.7	8.2	°C/Watt
	XC3S5000	2.9	5.9	13.1	9.2	8.1	7.6	°C/Watt

VQ100 Footprint

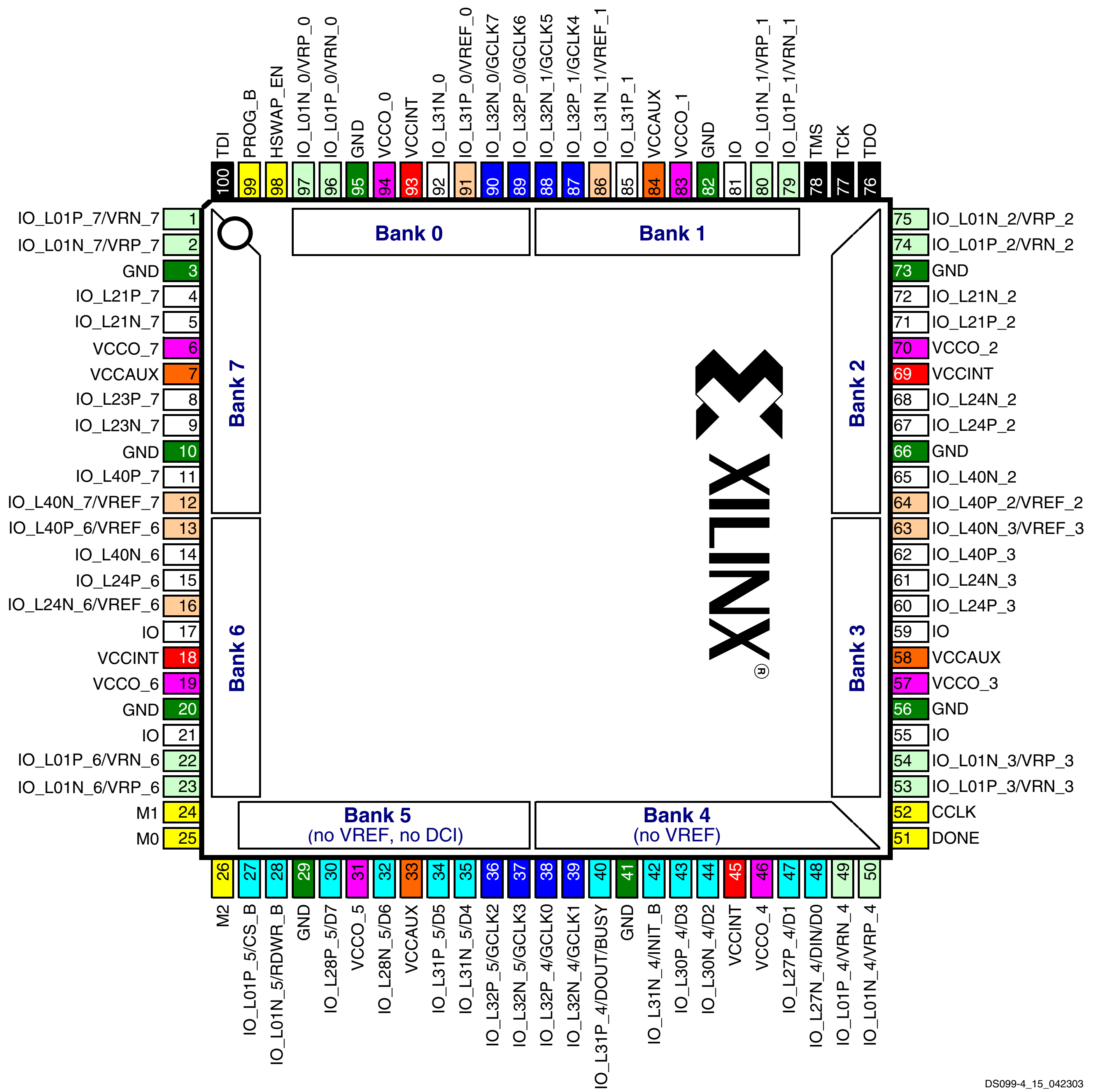


Figure 44: **VQ100 Package Footprint (Top View). Note pin 1 indicator in top-left corner and logo orientation.**

22	**I/O:** Unrestricted, general-purpose user I/O	12	**DUAL:** Configuration pin, then possible user I/O	7	**VREF:** User I/O or input voltage reference for bank
14	**DCI:** User I/O or reference resistor input for bank	8	**GCLK:** User I/O or global clock buffer input	8	**VCCO:** Output voltage supply for bank
7	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	4	**VCCINT:** Internal core voltage supply (+1.2V)
0	**N.C.:** No unconnected pins in this package	10	**GND:** Ground	4	**VCCAUX:** Auxiliary voltage supply (+2.5V)

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
N/A	VCCINT	N6	VCCINT
N/A	VCCINT	N7	VCCINT
VCCAUX	CCLK	T15	CONFIG
VCCAUX	DONE	R15	CONFIG
VCCAUX	HSWAP_EN	E6	CONFIG
VCCAUX	M0	P5	CONFIG
VCCAUX	M1	U3	CONFIG
VCCAUX	M2	R4	CONFIG
VCCAUX	PROG_B	E5	CONFIG
VCCAUX	TCK	E14	JTAG
VCCAUX	TDI	D4	JTAG
VCCAUX	TDO	D15	JTAG
VCCAUX	TMS	B16	JTAG

User I/Os by Bank

Table 99 indicates how the available user-I/O pins are distributed between the eight I/O banks on the FG320 package.

Table 99: **User I/Os Per Bank in FG320 Package**

Package Edge	I/O Bank	Maximum I/O	Maximum LVDS Pairs	All Possible I/O Pins by Type				
				I/O	DUAL	DCI	VREF	GCLK
Top	0	26	11	19	0	2	3	2
	1	26	11	19	0	2	3	2
Right	2	29	14	23	0	2	4	0
	3	29	14	23	0	2	4	0
Bottom	4	27	11	13	6	2	4	2
	5	26	11	13	6	2	3	2
Left	6	29	14	23	0	2	4	0
	7	29	14	23	0	2	4	0

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
2	N.C. (◆)	IO_L06N_2	IO_L06N_2	IO_L06N_2	IO_L06N_2	G20	I/O
2	N.C. (◆)	IO_L06P_2	IO_L06P_2	IO_L06P_2	IO_L06P_2	G21	I/O
2	N.C. (◆)	IO_L07N_2	IO_L07N_2	IO_L07N_2	IO_L07N_2	F23	I/O
2	N.C. (◆)	IO_L07P_2	IO_L07P_2	IO_L07P_2	IO_L07P_2	F24	I/O
2	N.C. (◆)	IO_L08N_2	IO_L08N_2	IO_L08N_2	IO_L08N_2	G22	I/O
2	N.C. (◆)	IO_L08P_2	IO_L08P_2	IO_L08P_2	IO_L08P_2	G23	I/O
2	N.C. (◆)	IO_L09N_2/VREF_2(1)	IO_L09N_2/VREF_2	IO_L09N_2/VREF_2	IO_L09N_2/VREF_2	F25	VREF(1)
2	N.C. (◆)	IO_L09P_2	IO_L09P_2	IO_L09P_2	IO_L09P_2	F26	I/O
2	N.C. (◆)	IO_L10N_2	IO_L10N_2	IO_L10N_2	IO_L10N_2	G25	I/O
2	N.C. (◆)	IO_L10P_2	IO_L10P_2	IO_L10P_2	IO_L10P_2	G26	I/O
2	IO_L14N_2	IO_L14N_2	IO_L14N_2(2)	IO_L11N_2(2)	IO_L11N_2	H20	I/O
2	IO_L14P_2	IO_L14P_2	IO_L14P_2(2)	IO_L11P_2(2)	IO_L11P_2	H21	I/O
2	IO_L16N_2	IO_L16N_2	IO_L16N_2(2)	IO_L12N_2(2)	IO_L12N_2	H22	I/O
2	IO_L16P_2	IO_L16P_2	IO_L16P_2(2)	IO_L12P_2(2)	IO_L12P_2	J21	I/O
2	IO_L17N_2	IO_L17N_2	IO_L17N_2(2)	IO_L13N_2(2)	IO(3)	H23	I/O
2	IO_L17P_2/VREF_2	IO_L17P_2/VREF_2	IO_L17P_2(2)/VREF_2	IO_L13P_2(2)/VREF_2	IO/VREF_2(3)	H24	VREF
2	IO_L19N_2	IO_L19N_2	IO_L19N_2	IO_L19N_2	IO_L19N_2	H25	I/O
2	IO_L19P_2	IO_L19P_2	IO_L19P_2	IO_L19P_2	IO_L19P_2	H26	I/O
2	IO_L20N_2	IO_L20N_2	IO_L20N_2	IO_L20N_2	IO_L20N_2	J20	I/O
2	IO_L20P_2	IO_L20P_2	IO_L20P_2	IO_L20P_2	IO_L20P_2	K20	I/O
2	IO_L21N_2	IO_L21N_2	IO_L21N_2	IO_L21N_2	IO_L21N_2	J22	I/O
2	IO_L21P_2	IO_L21P_2	IO_L21P_2	IO_L21P_2	IO_L21P_2	J23	I/O
2	IO_L22N_2	IO_L22N_2	IO_L22N_2	IO_L22N_2	IO_L22N_2	J24	I/O
2	IO_L22P_2	IO_L22P_2	IO_L22P_2	IO_L22P_2	IO_L22P_2	J25	I/O
2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	K21	VREF
2	IO_L23P_2	IO_L23P_2	IO_L23P_2	IO_L23P_2	IO_L23P_2	K22	I/O
2	IO_L24N_2	IO_L24N_2	IO_L24N_2	IO_L24N_2	IO_L24N_2	K23	I/O
2	IO_L24P_2	IO_L24P_2	IO_L24P_2	IO_L24P_2	IO_L24P_2	K24	I/O
2	IO_L26N_2	IO_L26N_2	IO_L26N_2	IO_L26N_2	IO_L26N_2	K25	I/O
2	IO_L26P_2	IO_L26P_2	IO_L26P_2	IO_L26P_2	IO_L26P_2	K26	I/O
2	IO_L27N_2	IO_L27N_2	IO_L27N_2	IO_L27N_2	IO_L27N_2	L19	I/O
2	IO_L27P_2	IO_L27P_2	IO_L27P_2	IO_L27P_2	IO_L27P_2	L20	I/O
2	IO_L28N_2	IO_L28N_2	IO_L28N_2	IO_L28N_2	IO_L28N_2	L21	I/O
2	IO_L28P_2	IO_L28P_2	IO_L28P_2	IO_L28P_2	IO_L28P_2	L22	I/O
2	IO_L29N_2	IO_L29N_2	IO_L29N_2	IO_L29N_2	IO_L29N_2	L25	I/O
2	IO_L29P_2	IO_L29P_2	IO_L29P_2	IO_L29P_2	IO_L29P_2	L26	I/O
2	IO_L31N_2	IO_L31N_2	IO_L31N_2	IO_L31N_2	IO_L31N_2	M19	I/O
2	IO_L31P_2	IO_L31P_2	IO_L31P_2	IO_L31P_2	IO_L31P_2	M20	I/O
2	IO_L32N_2	IO_L32N_2	IO_L32N_2	IO_L32N_2	IO_L32N_2	M21	I/O
2	IO_L32P_2	IO_L32P_2	IO_L32P_2	IO_L32P_2	IO_L32P_2	M22	I/O
2	IO_L33N_2	IO_L33N_2	IO_L33N_2	IO_L33N_2	IO_L33N_2	L23	I/O
2	IO_L33P_2	IO_L33P_2	IO_L33P_2	IO_L33P_2	IO_L33P_2	M24	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
7	IO_L22P_7	IO_L22P_7	M6	I/O
7	IO_L23N_7	IO_L23N_7	M3	I/O
7	IO_L23P_7	IO_L23P_7	M4	I/O
7	IO_L24N_7	IO_L24N_7	N10	I/O
7	IO_L24P_7	IO_L24P_7	M9	I/O
7	IO_L25N_7	IO_L25N_7	N3	I/O
7	IO_L25P_7	IO_L25P_7	N4	I/O
7	IO_L26N_7	IO_L26N_7	P11	I/O
7	IO_L26P_7	IO_L26P_7	N11	I/O
7	IO_L27N_7	IO_L27N_7	P7	I/O
7	IO_L27P_7/VREF_7	IO_L27P_7/VREF_7	P8	VREF
7	IO_L28N_7	IO_L28N_7	P5	I/O
7	IO_L28P_7	IO_L28P_7	P6	I/O
7	IO_L29N_7	IO_L29N_7	P3	I/O
7	IO_L29P_7	IO_L29P_7	P4	I/O
7	IO_L30N_7	IO_L30N_7	R6	I/O
7	IO_L30P_7	IO_L30P_7	R7	I/O
7	IO_L31N_7	IO_L31N_7	R3	I/O
7	IO_L31P_7	IO_L31P_7	R4	I/O
7	IO_L32N_7	IO_L32N_7	R1	I/O
7	IO_L32P_7	IO_L32P_7	R2	I/O
7	IO_L33N_7	IO_L33N_7	T10	I/O
7	IO_L33P_7	IO_L33P_7	R9	I/O
7	IO_L34N_7	IO_L34N_7	T6	I/O
7	IO_L34P_7	IO_L34P_7	T7	I/O
7	IO_L35N_7	IO_L35N_7	T2	I/O
7	IO_L35P_7	IO_L35P_7	T3	I/O
7	IO_L37N_7	IO_L37N_7	U7	I/O
7	IO_L37P_7/VREF_7	IO_L37P_7/VREF_7	U8	VREF
7	IO_L38N_7	IO_L38N_7	U5	I/O
7	IO_L38P_7	IO_L38P_7	U6	I/O
7	IO_L39N_7	IO_L39N_7	U3	I/O
7	IO_L39P_7	IO_L39P_7	U4	I/O
7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	U1	VREF
7	IO_L40P_7	IO_L40P_7	U2	I/O
7	N.C. (◆)	IO_L41N_7	G3	I/O
7	N.C. (◆)	IO_L41P_7	G4	I/O
7	N.C. (◆)	IO_L44N_7	L6	I/O
7	N.C. (◆)	IO_L44P_7	L7	I/O
7	IO_L45N_7	IO_L45N_7	M1	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
N/A	GND	GND	J22	GND
N/A	GND	GND	J30	GND
N/A	GND	GND	J34	GND
N/A	GND	GND	J5	GND
N/A	GND	GND	K10	GND
N/A	GND	GND	K25	GND
N/A	GND	GND	L3	GND
N/A	GND	GND	L32	GND
N/A	GND	GND	N1	GND
N/A	GND	GND	N17	GND
N/A	GND	GND	N18	GND
N/A	GND	GND	N26	GND
N/A	GND	GND	N30	GND
N/A	GND	GND	N34	GND
N/A	GND	GND	N5	GND
N/A	GND	GND	N9	GND
N/A	GND	GND	P14	GND
N/A	GND	GND	P15	GND
N/A	GND	GND	P16	GND
N/A	GND	GND	P17	GND
N/A	GND	GND	P18	GND
N/A	GND	GND	P19	GND
N/A	GND	GND	P20	GND
N/A	GND	GND	P21	GND
N/A	GND	GND	R14	GND
N/A	GND	GND	R15	GND
N/A	GND	GND	R16	GND
N/A	GND	GND	R17	GND
N/A	GND	GND	R18	GND
N/A	GND	GND	R19	GND
N/A	GND	GND	R20	GND
N/A	GND	GND	R21	GND
N/A	GND	GND	T1	GND
N/A	GND	GND	T14	GND
N/A	GND	GND	T15	GND
N/A	GND	GND	T16	GND
N/A	GND	GND	T17	GND
N/A	GND	GND	T18	GND
N/A	GND	GND	T19	GND
N/A	GND	GND	T20	GND

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
N/A	VCCAUX	VCCAUX	Y5	VCCAUX
N/A	VCCINT	VCCINT	AA13	VCCINT
N/A	VCCINT	VCCINT	AA22	VCCINT
N/A	VCCINT	VCCINT	AB13	VCCINT
N/A	VCCINT	VCCINT	AB14	VCCINT
N/A	VCCINT	VCCINT	AB15	VCCINT
N/A	VCCINT	VCCINT	AB16	VCCINT
N/A	VCCINT	VCCINT	AB19	VCCINT
N/A	VCCINT	VCCINT	AB20	VCCINT
N/A	VCCINT	VCCINT	AB21	VCCINT
N/A	VCCINT	VCCINT	AB22	VCCINT
N/A	VCCINT	VCCINT	AC12	VCCINT
N/A	VCCINT	VCCINT	AC17	VCCINT
N/A	VCCINT	VCCINT	AC18	VCCINT
N/A	VCCINT	VCCINT	AC23	VCCINT
N/A	VCCINT	VCCINT	M12	VCCINT
N/A	VCCINT	VCCINT	M17	VCCINT
N/A	VCCINT	VCCINT	M18	VCCINT
N/A	VCCINT	VCCINT	M23	VCCINT
N/A	VCCINT	VCCINT	N13	VCCINT
N/A	VCCINT	VCCINT	N14	VCCINT
N/A	VCCINT	VCCINT	N15	VCCINT
N/A	VCCINT	VCCINT	N16	VCCINT
N/A	VCCINT	VCCINT	N19	VCCINT
N/A	VCCINT	VCCINT	N20	VCCINT
N/A	VCCINT	VCCINT	N21	VCCINT
N/A	VCCINT	VCCINT	N22	VCCINT
N/A	VCCINT	VCCINT	P13	VCCINT
N/A	VCCINT	VCCINT	P22	VCCINT
N/A	VCCINT	VCCINT	R13	VCCINT
N/A	VCCINT	VCCINT	R22	VCCINT
N/A	VCCINT	VCCINT	T13	VCCINT
N/A	VCCINT	VCCINT	T22	VCCINT
N/A	VCCINT	VCCINT	U12	VCCINT
N/A	VCCINT	VCCINT	U23	VCCINT
N/A	VCCINT	VCCINT	V12	VCCINT
N/A	VCCINT	VCCINT	V23	VCCINT
N/A	VCCINT	VCCINT	W13	VCCINT
N/A	VCCINT	VCCINT	W22	VCCINT
N/A	VCCINT	VCCINT	Y13	VCCINT

Revision History

Date	Version	Description
04/03/03	1.0	Initial Xilinx release.
04/21/03	1.1	Added information on the VQ100 package footprint, including a complete pinout table (Table 87) and footprint diagram (Figure 44). Updated Table 85 with final I/O counts for the VQ100 package. Also added final differential I/O pair counts for the TQ144 package. Added clarifying comments to HSWAP_EN pin description on page 119. Updated the footprint diagram for the FG900 package shown in Figure 55a and Figure 55b. Some thick lines separating I/O banks were incorrect. Made cosmetic changes to Figure 40, Figure 42, and Figure 43. Updated Xilinx hypertext links. Added XC3S200 and XC3S400 to Pin Name column in Table 91.
05/12/03	1.1.1	AM32 pin was missing GND label in FG1156 package diagram (Figure 53).
07/11/03	1.1.2	Corrected misspellings of GCLK in Table 69 and Table 70. Changed CMOS25 to LVCMOS25 in Dual-Purpose Pin I/O Standard During Configuration section. Clarified references to Module 2. For XC3S5000 in FG1156 package, corrected N.C. symbol to a black square in Table 110, key, and package drawing.
07/29/03	1.2	Corrected pin names on FG1156 package. Some package balls incorrectly included LVDS pair names. The affected balls on the FG1156 package include G1, G2, G33, G34, U9, U10, U25, U26, V9, V10, V25, V26, AH1, AH2, AH33, AH34. The number of LVDS pairs is unaffected. Modified affected balls and re-sorted rows in Table 110. Updated affected balls in Figure 53. Also updated ASCII and Excel electronic versions of FG1156 pinout.
08/19/03	1.2.1	Removed 100 MHz ConfigRate option in CCLK: Configuration Clock section and in Table 80. Added note that TDO is a totem-pole output in Table 77.
10/09/03	1.2.2	Some pins had incorrect bank designations and were improperly sorted in Table 93. No pin names or functions changed. Renamed DCI_IN to DCI and added black diamond to N.C. pins in Table 93. In Figure 47, removed some extraneous text from pin 106 and corrected spelling of pins 45, 48, and 81.
12/17/03	1.3	Added FG320 pin tables and pinout diagram (FG320: 320-lead Fine-pitch Ball Grid Array). Made cosmetic changes to the TQ144 footprint (Figure 46), the PQ208 footprint (Figure 47), the FG676 footprint (Figure 53), and the FG900 footprint (Figure 55). Clarified wording in Precautions When Using the JTAG Port in 3.3V Environments section.
02/27/04	1.4	Clarified wording in Using JTAG Port After Configuration section. In Table 81, reduced package height for FG320 and increased maximum I/O values for the FG676, FG900, and FG1156 packages.
07/13/04	1.5	Added information on lead-free (Pb-free) package options to the Package Overview section plus Table 81 and Table 83. Clarified the VRN_# reference resistor requirements for I/O standards that use single termination as described in the DCI Termination Types section and in Figure 42b. Graduated from Advance Product Specification to Product Specification.
08/24/04	1.5.1	Removed XC3S2000 references from FG1156: 1156-lead Fine-pitch Ball Grid Array.
01/17/05	1.6	Added XC3S50 in CP132 package option. Added XC3S2000 in FG456 package option. Added XC3S4000 in FG676 package option. Added Selecting the Right Package Option section. Modified or added Table 81, Table 83, Table 84, Table 85, Table 89, Table 90, Table 100, Table 102, Table 103, Table 106, Figure 45, and Figure 53.
08/19/05	1.7	Removed term “weak” from the description of pull-up and pull-down resistors. Added IDCODE Register values. Added signal integrity precautions to CCLK: Configuration Clock and indicated that CCLK should be treated as an I/O during Master mode in Table 79.
04/03/06	2.0	Added Package Thermal Characteristics. Updated Figure 41 to make it a more obvious example. Added detail about which pins have dedicated pull-up resistors during configuration, regardless of the HSWAP_EN value to Table 70 and to Pin Behavior During Configuration. Updated Precautions When Using the JTAG Port in 3.3V Environments.
04/26/06	2.1	Corrected swapped data row in Table 86. The Theta-JA with zero airflow column was swapped with the Theta-JC column. Made additional notations on CONFIG and JTAG pins that have pull-up resistors during configuration, regardless of the HSWAP_EN input.
05/25/07	2.2	Added link on page 128 to Material Declaration Data Sheets. Corrected units typo in Table 74. Added Note 1 to Table 103 about VREF for XC3S1500 in FG676.

Date	Version	Description
11/30/07	2.3	Added XC3S5000 FG(G)676 package. Noted that the FG(G)1156 package is being discontinued. Updated Table 86 with latest thermal characteristics data.
06/25/08	2.4	Updated formatting and links.
12/04/09	2.5	Added link to UG332 in CCLK: Configuration Clock. Noted that the CP132, CPG132, FG1156, and FGG1156 packages are being discontinued in Table 81, Table 83, Table 84, Table 85, and Table 86. Updated CP132: 132-Ball Chip-Scale Package to indicate that the CP132 and CPG132 packages are being discontinued.
10/29/12	3.0	Added Notice of Disclaimer. Per XCN07022, updated the FG1156 and FGG1156 package discussion throughout document including in Table 81, Table 83, Table 84, Table 85, and Table 86. Per XCN08011, updated CP132 and CPG132 package discussion throughout document including in Table 81, Table 83, Table 84, Table 85, and Table 86. This product is not recommended for new designs.

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