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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	192
Number of Logic Elements/Cells	1728
Total RAM Bits	73728
Number of I/O	63
Number of Gates	50000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s50-5vqg100c

power, the configuration data is written to the FPGA using any of five different modes: Master Parallel, Slave Parallel, Master Serial, Slave Serial, and Boundary Scan (JTAG). The Master and Slave Parallel modes use an 8-bit-wide SelectMAP port.

The recommended memory for storing the configuration data is the low-cost Xilinx Platform Flash PROM family, which includes the XCF00S PROMs for serial configuration and the higher density XCF00P PROMs for parallel or serial configuration.

I/O Capabilities

The SelectIO feature of Spartan-3 devices supports eighteen single-ended standards and eight differential standards as listed in Table 2. Many standards support the DCI feature, which uses integrated terminations to eliminate unwanted signal reflections.

Table 2: **Signal Standards Supported by the Spartan-3 Family**

Standard Category	Description	V_{CCO} (V)	Class	Symbol (IOSTANDARD)	DCI Option
Single-Ended					
GTL	Gunning Transceiver Logic	N/A	Terminated	GTL	Yes
			Plus	GTLP	Yes
HSTL	High-Speed Transceiver Logic	1.5	I	HSTL_I	Yes
			III	HSTL_III	Yes
		1.8	I	HSTL_I_18	Yes
			II	HSTL_II_18	Yes
			III	HSTL_III_18	Yes
LVCMOS	Low-Voltage CMOS	1.2	N/A	LVCMOS12	No
		1.5	N/A	LVCMOS15	Yes
		1.8	N/A	LVCMOS18	Yes
		2.5	N/A	LVCMOS25	Yes
		3.3	N/A	LVCMOS33	Yes
LVTTL	Low-Voltage Transistor-Transistor Logic	3.3	N/A	LVTTL	No
PCI	Peripheral Component Interconnect	3.0	33 MHz(1)	PCI33_3	No
SSTL	Stub Series Terminated Logic	1.8	N/A (±6.7 mA)	SSTL18_I	Yes
			N/A (±13.4 mA)	SSTL18_II	No
		2.5	I	SSTL2_I	Yes
			II	SSTL2_II	Yes
Differential					
LDT (ULVDS)	Lightning Data Transport (HyperTransport™) Logic	2.5	N/A	LDT_25	No
LVDS	Low-Voltage Differential Signaling		Standard	LVDS_25	Yes
			Bus	BLVDS_25	No
			Extended Mode	LVDSEXT_25	Yes
LVPECL	Low-Voltage Positive Emitter-Coupled Logic	2.5	N/A	LVPECL_25	No
RSDS	Reduced-Swing Differential Signaling	2.5	N/A	RSDS_25	No
HSTL	Differential High-Speed Transceiver Logic	1.8	II	DIFF_HSTL_II_18	Yes
SSTL	Differential Stub Series Terminated Logic	2.5	II	DIFF_SSTL2_II	Yes

Notes:

1. 66 MHz PCI is not supported by the Xilinx IP core although PCI66_3 is an available I/O standard.

Table 3 shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination.

Table 3: **Spartan-3 Device I/O Chart**

Available User I/Os and Differential (Diff) I/O Pairs by Package Type																				
Package	**VQ100 VQG100**		**CP132(1) CPG132**		**TQ144 TQG144**		**PQ208 PQG208**		**FT256 FTG256**		**FG320 FGG320**		**FG456 FGG456**		**FG676 FGG676**		**FG900 FGG900**		**FG1156(1) FGG1156**	
Footprint (mm)	**16 x 16**		**8 x 8**		**22 x 22**		**30.6 x 30.6**		**17 x 17**		**19 x 19**		**23 x 23**		**27 x 27**		**31 x 31**		**35 x 35**	
Device	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**
XC3S50	63	29	89(1)	44(1)	97	46	124	56	–	–	–	–	–	–	–	–	–	–	–	–
XC3S200	63	29	–	–	97	46	141	62	173	76	–	–	–	–	–	–	–	–	–	–
XC3S400	–	–	–	–	97	46	141	62	173	76	221	100	264	116	–	–	–	–	–	–
XC3S1000	–	–	–	–	–	–	–	–	173	76	221	100	333	149	391	175	–	–	–	–
XC3S1500	–	–	–	–	–	–	–	–	–	–	221	100	333	149	487	221	–	–	–	–
XC3S2000	–	–	–	–	–	–	–	–	–	–	–	–	333	149	489	221	565	270	–	–
XC3S4000	–	–	–	–	–	–	–	–	–	–	–	–	–	–	489	221	633	300	712(1)	312(1)
XC3S5000	–	–	–	–	–	–	–	–	–	–	–	–	–	–	489	221	633	300	784(1)	344(1)

Notes:

1. The CP132, CPG132, FG1156, and FGG1156 packages are discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.
2. All device options listed in a given package column are pin-compatible.
3. User = Single-ended user I/O pins. Diff = Differential I/O pairs.

Package Marking

Figure 2 shows the top marking for Spartan-3 FPGAs in the quad-flat packages. Figure 3 shows the top marking for Spartan-3 FPGAs in BGA packages except the 132-ball chip-scale package (CP132 and CPG132). The markings for the BGA packages are nearly identical to those for the quad-flat packages, except that the marking is rotated with respect to the ball A1 indicator. Figure 4 shows the top marking for Spartan-3 FPGAs in the CP132 and CPG132 packages.

The "5C" and "4I" part combinations may be dual marked as "5C/4I". Devices with the dual mark can be used as either -5C or -4I devices. Devices with a single mark are only guaranteed for the marked speed grade and temperature range. Some specifications vary according to mask revision. Mask revision E devices are errata-free. All shipments since 2006 have been mask revision E.

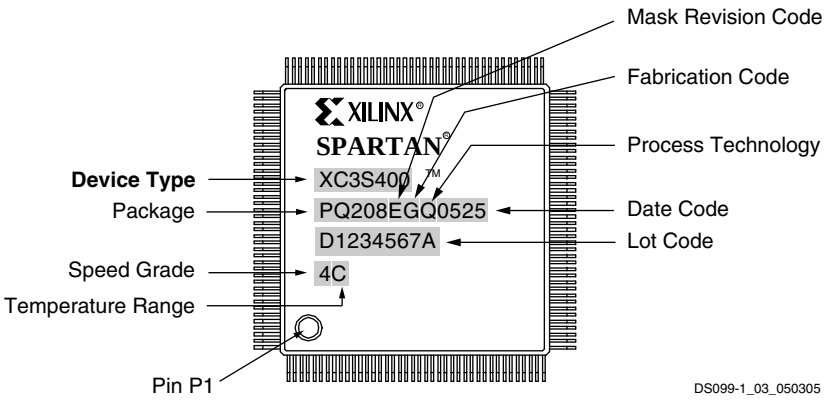


Figure 2: **Spartan-3 FPGA QFP Package Marking Example for Part Number XC3S400-4PQ208C**

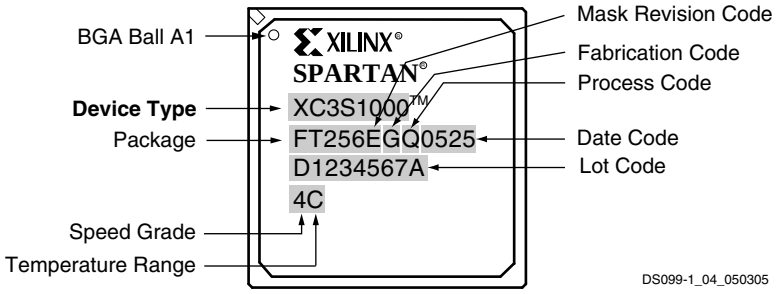


Figure 3: **Spartan-3 FPGA BGA Package Marking Example for Part Number XC3S1000-4FT256C**

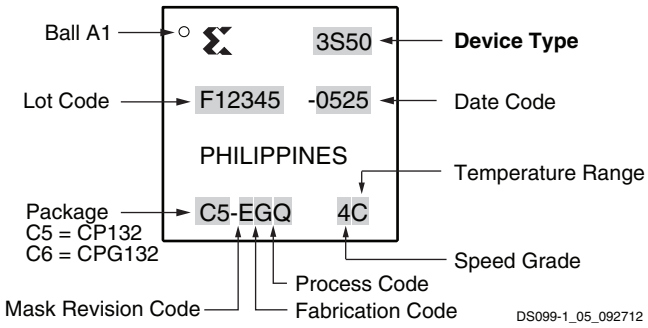


Figure 4: **Spartan-3 FPGA CP132 and CPG132 Package Marking Example for XC3S50-4CP132C**

Ordering Information

Spartan-3 FPGAs are available in both standard (Figure 5) and Pb-free (Figure 6) packaging options for all device/package combinations. The Pb-free packages include a special 'G' character in the ordering code.

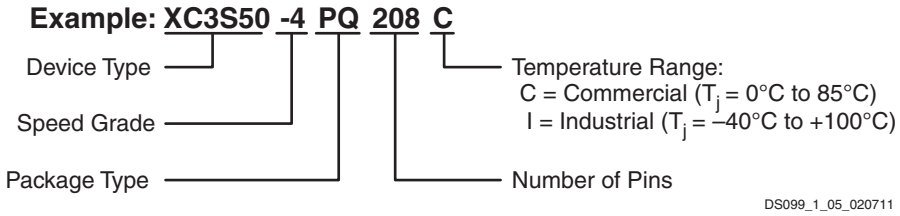


Figure 5: **Standard Packaging**

For additional information on Pb-free packaging, see XAPP427: *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

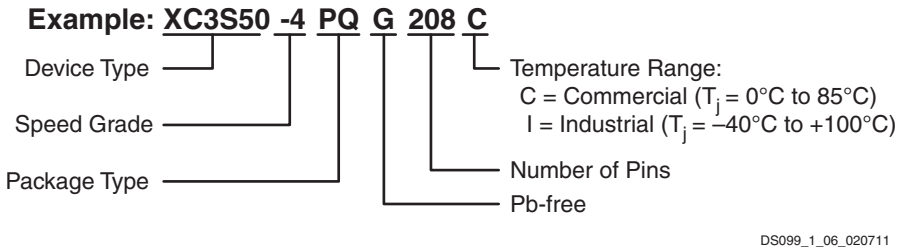


Figure 6: **Pb-Free Packaging**

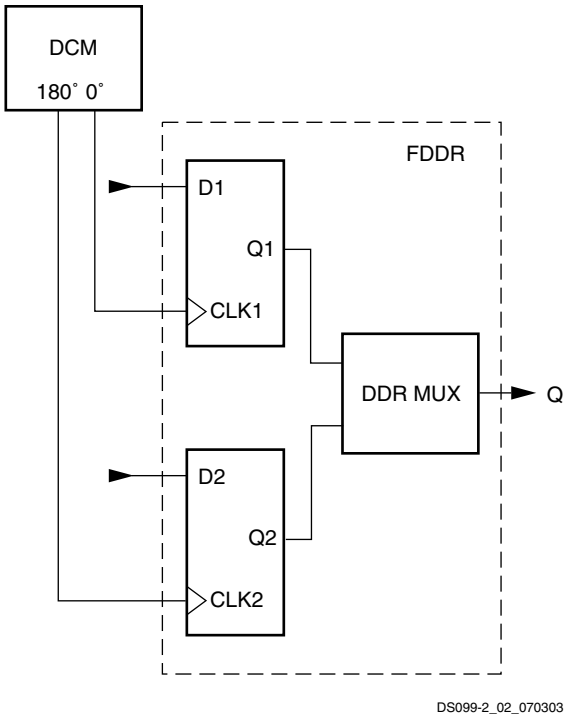


Figure 8: **Clocking the DDR Register**

Aside from high bandwidth data transfers, DDR can also be used to reproduce, or “mirror”, a clock signal on the output. This approach is used to transmit clock and data signals together. A similar approach is used to reproduce a clock signal at multiple outputs. The advantage for both approaches is that skew across the outputs will be minimal.

Some adjacent I/O blocks (IOBs) share common routing connecting the ICLK1, ICLK2, OTCLK1, and OTCLK2 clock inputs of both IOBs. These IOB pairs are identified by their differential pair names IO_LxxN_# and IO_LxxP_#, where "xx" is an I/O pair number and ‘#’ is an I/O bank number. Two adjacent IOBs containing DDR registers must share common clock inputs, otherwise one or more of the clock signals will be unroutable.

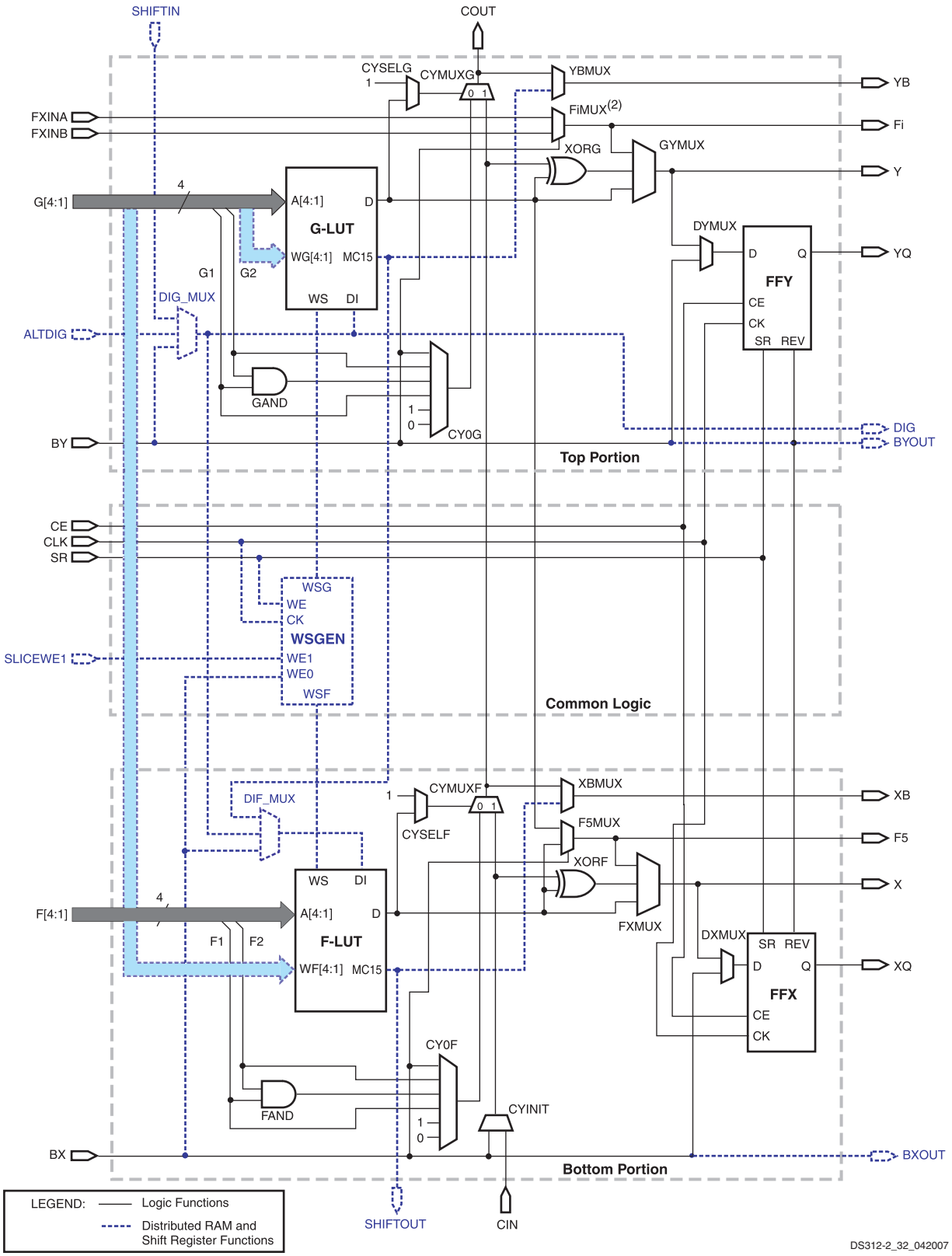
Pull-Up and Pull-Down Resistors

The optional pull-up and pull-down resistors are intended to establish High and Low levels, respectively, at unused I/Os. The pull-up resistor optionally connects each IOB pad to V_{CCO}. A pull-down resistor optionally connects each pad to GND. These resistors are placed in a design using the PULLUP and PULLDOWN symbols in a schematic, respectively. They can also be instantiated as components, set as constraints or passed as attributes in HDL code. These resistors can also be selected for all unused I/O using the Bitstream Generator (BitGen) option UnusedPin. A Low logic level on HSWAP_EN activates the pull-up resistors on all I/Os during configuration (see The I/Os During Power-On, Configuration, and User Mode, page 21).

The Spartan-3 FPGAs I/O pull-up and pull-down resistors are significantly stronger than the "weak" pull-up/pull-down resistors used in previous Xilinx FPGA families. See Table 33, page 61 for equivalent resistor strengths.

Keeper Circuit

Each I/O has an optional keeper circuit that retains the last logic level on a line after all drivers have been turned off. This is useful to keep bus lines from floating when all connected drivers are in a high-impedance state. This function is placed in a design using the KEEPER symbol. Pull-up and pull-down resistors override the keeper circuit.



Notes:

1. Options to invert signal polarity as well as other options that enable lines for various functions are not shown.
2. The index i can be 6, 7, or 8, depending on the slice. In this position, the upper right-hand slice has an F8MUX, and the upper left-hand slice has an F7MUX. The lower right-hand and left-hand slices both have an F6MUX.

Figure 12: **Simplified Diagram of the Left-Hand SLICEM**

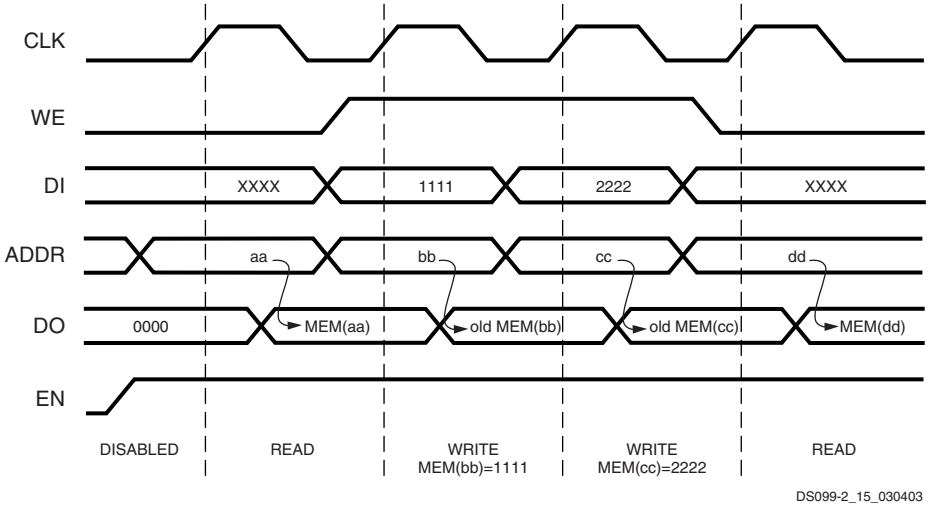


Figure 16: **Waveforms of Block RAM Data Operations with READ_FIRST Selected**

Choosing a third attribute called NO_CHANGE puts the DO outputs in a latched state when asserting WE. Under this condition, the DO outputs will retain the data driven just before WE was asserted. NO_CHANGE timing is shown in the portion of Figure 17 during which WE is High.

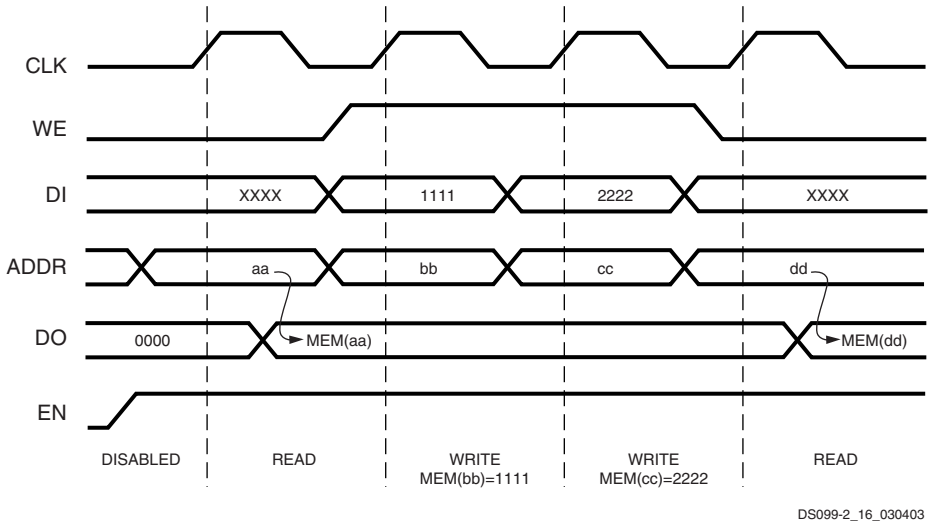


Figure 17: **Waveforms of Block RAM Data Operations with NO_CHANGE Selected**

Dedicated Multipliers

All Spartan-3 devices provide embedded multipliers that accept two 18-bit words as inputs to produce a 36-bit product. This section provides an introduction to multipliers. For further details, refer to the chapter entitled “Using Embedded Multipliers” in UG331.

The input buses to the multiplier accept data in two’s-complement form (either 18-bit signed or 17-bit unsigned). One such multiplier is matched to each block RAM on the die. The close physical proximity of the two ensures efficient data handling. Cascading multipliers permits multiplicands more than three in number as well as wider than 18-bits. The multiplier is placed in a design using one of two primitives: an asynchronous version called MULT18X18 and a version with a register called MULT18X18S, as shown in Figure 18. The signals for these primitives are defined in Table 15.

The CORE Generator system produces multipliers based on these primitives that can be configured to suit a wide range of requirements.

DFS Clock Output Connections

There are two basic cases that determine how to connect the DFS clock outputs: on-chip and off-chip, which are illustrated in sections [a] and [c], respectively, of Figure 21. This is similar to what has already been described for the DLL component. See DLL Clock Output and Feedback Connections, page 34.

In the on-chip case, it is possible to connect either of the DFS's two output clock signals through general routing resources to the FPGA's internal registers. Either a Global Clock Buffer (BUFG) or a BUFGMUX affords access to the global clock network. The optional feedback loop is formed in this way, routing CLK0 to a global clock net, which in turn drives the CLKFB input.

In the off-chip case, the DFS's two output clock signals, plus CLK0 for an optional feedback loop, can exit the FPGA using output buffers (OBUF) to drive a clock network plus registers on the board. The feedback loop is formed by feeding the CLK0 signal back into the FPGA using an IBUFG, which directly accesses the global clock network, or an IBUF. Then, the global clock net is connected directly to the CLKFB input.

Phase Shifter (PS)

The DCM provides two approaches to controlling the phase of a DCM clock output signal relative to the CLKIN signal: First, there are nine clock outputs that employ the DLL to achieve a desired phase relationship: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, CLKDV CLKFX, and CLKFX180. These outputs afford "coarse" phase control.

The second approach uses the PS component described in this section to provide a still finer degree of control. The PS component is only available when the DLL is operating in its low-frequency mode. The PS component phase shifts the DCM output clocks by introducing a "fine phase shift" (T_{PS}) between the CLKFB and CLKIN signals inside the DLL component. The user can control this fine phase shift down to a resolution of 1/256 of a CLKIN cycle or one tap delay (DCM_TAP), whichever is greater. When in use, the PS component shifts the phase of all nine DCM clock output signals together. If the PS component is used together with a DCM clock output such as the CLK90, CLK180, CLK270, CLK2X180 and CLKFX180, then the fine phase shift of the former gets added to the coarse phase shift of the latter.

PS Component Enabling and Mode Selection

The CLKOUT_PHASE_SHIFT attribute enables the PS component for use in addition to selecting between two operating modes. As described in Table 20, this attribute has three possible values: NONE, FIXED and VARIABLE. When CLKOUT_PHASE_SHIFT is set to NONE, the PS component is disabled and its inputs, PSEN, PSCLK, and PSINCDEC, must be tied to GND. The set of waveforms in section [a] of Figure 22 shows the disabled case, where the DLL maintains a zero-phase alignment of signals CLKFB and CLKIN upon which the PS component has no effect. The PS component is enabled by setting the attribute to either the FIXED or VARIABLE values, which select the Fixed Phase mode and the Variable Phase mode, respectively. These two modes are described in the sections that follow

Determining the Fine Phase Shift

The user controls the phase shift of CLKFB relative to CLKIN by setting and/or adjusting the value of the PHASE_SHIFT attribute. This value must be an integer ranging from –255 to +255. The PS component uses this value to calculate the desired fine phase shift (T_{PS}) as a fraction of the CLKIN period (T_{CLKIN}). Given values for PHASE-SHIFT and T_{CLKIN}, it is possible to calculate T_{PS} as follows:

$$T_{PS} = T_{CLKIN}(PHASE\_SHIFT/256) \qquad \textit{Equation 4}$$

Both the Fixed Phase and Variable Phase operating modes employ this calculation. If the PHASE_SHIFT value is zero, then CLKFB and CLKIN will be in phase, the same as when the PS component is disabled. When the PHASE_SHIFT value is positive, the CLKFB signal will be shifted later in time with respect to CLKIN. If the attribute value is negative, the CLKFB signal will be shifted earlier in time with respect to CLKIN.

The Fixed Phase Mode

This mode fixes the desired fine phase shift to a fraction of the T_{CLKIN}, as determined by Equation 4 and its user-selected PHASE_SHIFT value P. The set of waveforms insection [b] of Figure 22 illustrates the relationship between CLKFB and CLKIN in the Fixed Phase mode. In the Fixed Phase mode, the PSEN, PSCLK and PSINCDEC inputs are not used and must be tied to GND. Fixed phase shift requires ISE software version 10.1.03 or later.

Table 22: **Status Logic Signals**

Signal	Direction	Description
RST	Input	A High resets the entire DCM to its initial power-on state. Initializes the DLL taps for a delay of zero. Sets the LOCKED output Low. This input is asynchronous.
STATUS[7:0]	Output	The bit values on the STATUS bus provide information regarding the state of DLL and PS operation
LOCKED	Output	Indicates that the CLKIN and CLKFB signals are in phase by going High. The two signals are out-of-phase when Low.

Table 23: **DCM STATUS Bus**

Bit	Name	Description
0	Phase Shift Overflow	A value of 1 indicates a phase shift overflow when one of two conditions occurs: Incrementing (or decrementing) TPS beyond 255/256 of a CLKIN cycle. The DLL is producing its maximum possible phase shift (i.e., all delay taps are active).(1)
1	CLKIN Input Stopped Toggling	A value of 1 indicates that the CLKIN input signal is not toggling. A value of 0 indicates toggling. This bit functions only when the CLKFB input is connected.(2)
2	CLKFX/CLKFX180 Output Stopped Toggling	A value of 1 indicates that the CLKFX or CLKFX180 output signals are not toggling. A value of 0 indicates toggling. This bit functions only when using the Digital Frequency Synthesizer (DFS).
3:7	Reserved	–

Notes:

1. The DLL phase shift with all delay taps active is specified as the parameter FINE_SHIFT_RANGE.
2. If only the DFS clock outputs are used, but none of the DLL clock outputs, this bit will not go High when the CLKIN signal stops.

Table 24: **Status Attributes**

Attribute	Description	Values
STARTUP_WAIT	Delays transition from configuration to user mode until lock condition is achieved.	TRUE, FALSE

Stabilizing DCM Clocks Before User Mode

It is possible to delay the completion of device configuration until after the DLL has achieved a lock condition using the STARTUP_WAIT attribute described in Table 24. This option ensures that the FPGA does not enter user mode—i.e., begin functional operation—until all system clocks generated by the DCM are stable. In order to achieve the delay, it is necessary to set the attribute to TRUE as well as set the BitGen option LCK_cycle to one of the six cycles making up the Startup phase of configuration. The selected cycle defines the point at which configuration will halt until the LOCKED output goes High.

Global Clock Network

Spartan-3 devices have eight Global Clock inputs called GCLK0 - GCLK7. These inputs provide access to a low-capacitance, low-skew network that is well-suited to carrying high-frequency signals. The Spartan-3 FPGAs clock network is shown in Figure 23. GCLK0 through GCLK3 are located in the center of the bottom edge. GCLK4 through GCLK7 are located in the center of the top edge.

Eight Global Clock Multiplexers (also called BUFGMUX elements) are provided that accept signals from Global Clock inputs and route them to the internal clock network as well as DCMs. Four BUFGMUX elements are located in the center of the bottom edge, just above the GCLK0 - GCLK3 inputs. The remaining four BUFGMUX elements are located in the center of the top edge, just below the GCLK4 - GCLK7 inputs.

Pairs of BUFGMUX elements share global inputs, as shown in Figure 24. For example, the GCLK4 and GCLK5 inputs both potentially connect to BUFGMUX4 and BUFGMUX5 located in the upper right center. A differential clock input uses a pair of GCLK inputs to connect to a single BUFGMUX element.

Table 47: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
PCI33_3	0.74	0.85	ns
SSTL18_I	0.07	0.07	ns
SSTL18_I_DCI	0.22	0.25	ns
SSTL18_II	0.30	0.34	ns
SSTL2_I	0.23	0.26	ns
SSTL2_I_DCI	0.19	0.22	ns
SSTL2_II	0.13	0.15	ns
SSTL2_II_DCI	0.10	0.11	ns
Differential Standards			
LDT_25 (ULVDS_25)	–0.06	–0.05	ns
LVDS_25	–0.09	–0.07	ns
BLVDS_25	0.02	0.04	ns
LVDSEXT_25	–0.15	–0.13	ns
LVPECL_25	0.16	0.18	ns
RSDS_25	0.05	0.06	ns
DIFF_HSTL_II_18	–0.02	–0.01	ns
DIFF_HSTL_II_18_DCI	0.75	0.86	ns
DIFF_SSTL2_II	0.13	0.15	ns
DIFF_SSTL2_II_DCI	0.10	0.11	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32, Table 35, and Table 37.
2. These adjustments are used to convert output- and three-state-path times originally specified for the LVCMOS25 standard with 12 mA drive and Fast slew rate to times that correspond to other signal standards. Do not adjust times that measure when outputs go into a high-impedance state.
3. For minimums, use the values reported by the Xilinx timing analyzer.

Table 61: **Switching Characteristics for the DFS**

Symbol	Description	Frequency Mode	Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Output Frequency Ranges								
CLKOUT_FREQ_FX_LF	Frequency for the CLKFX and CLKFX180 outputs	Low	All	18	210	18	210	MHz
CLKOUT_FREQ_FX_HF		High	All	210	326(2)	210	307(2)	MHz
Output Clock Jitter								
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs	All	All	Note 3	Note 3	Note 3	Note 3	ps
Duty Cycle(4)								
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs	All	XC3S50	–	±100	–	±100	ps
			XC3S200	–	±100	–	±100	ps
			XC3S400	–	±250	–	±250	ps
			XC3S1000	–	±400	–	±400	ps
			XC3S1500	–	±400	–	±400	ps
			XC3S2000	–	±400	–	±400	ps
			XC3S4000	–	±400	–	±400	ps
			XC3S5000	–	±400	–	±400	ps
Phase Alignment								
CLKOUT_PHASE	Phase offset between the DFS output and the CLK0 output	All	All	–	±300	–	±300	ps
Lock Time								
LOCK_DLL_FX	When using the DFS in conjunction with the DLL: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase.	All	All	–	10.0	–	10.0	ms
LOCK_FX	When using the DFS without the DLL: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. By asserting the LOCKED signal, the DFS indicates valid CLKFX and CLKFX180 signals.	All	All	–	10.0	–	10.0	ms

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32 and Table 60.
2. Mask revisions prior to the E mask revision have a CLKOUT_FREQ_FX_HF max of 280 MHz. See Mask and Fab Revisions, page 58.
3. Use the DCM Clocking Wizard in the ISE software for a Spartan-3 device specific number. Jitter number assumes 150 ps of input clock jitter.
4. The CLKFX and CLKFX180 outputs always approximate 50% duty cycles.
5. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) is in use.

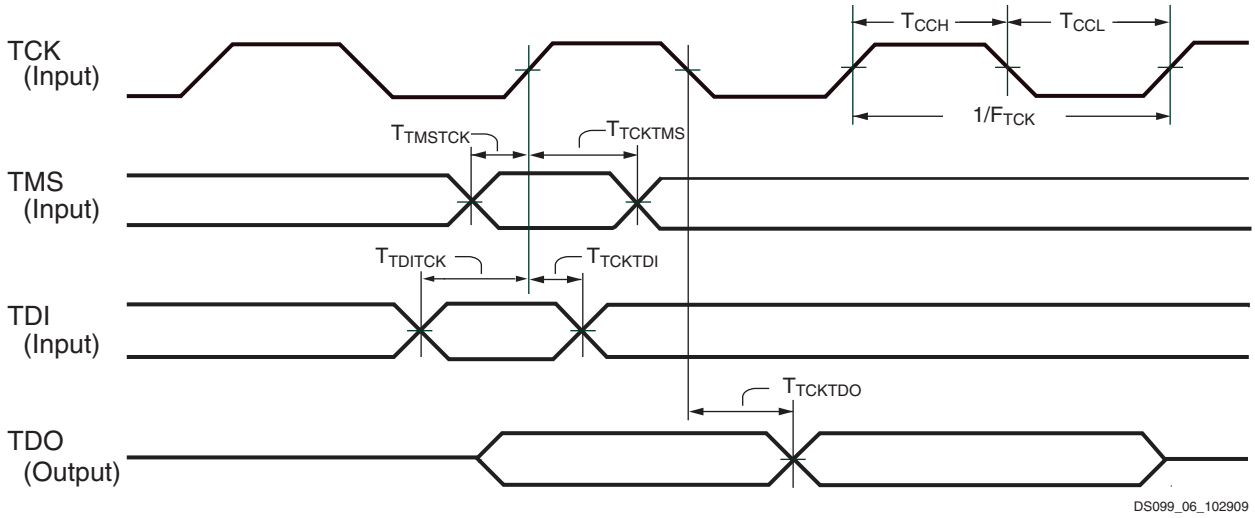


Figure 39: **JTAG Waveforms**

Table 68: **Timing for the JTAG Test Access Port**

Symbol	Description		All Speed Grades		Units
			Min	Max	
Clock-to-Output Times					
T_{TCKTDO}	The time from the falling transition on the TCK pin to data appearing at the TDO pin		1.0	11.0	ns
Setup Times					
T_{TDITCK}	The time from the setup of data at the TDI pin to the rising transition at the TCK pin		7.0	–	ns
T_{TMSTCK}	The time from the setup of a logic level at the TMS pin to the rising transition at the TCK pin		7.0	–	ns
Hold Times					
T_{TCKTDI}	The time from the rising transition at the TCK pin to the point when data is last held at the TDI pin		0	–	ns
T_{TCKTMS}	The time from the rising transition at the TCK pin to the point when a logic level is last held at the TMS pin		0	–	ns
Clock Timing					
T_{TCKH}	TCK pin High pulse width		5	∞	ns
T_{TCKL}	TCK pin Low pulse width		5	∞	ns
F_{TCK}	Frequency of the TCK signal	JTAG Configuration	0	33	MHz
		Boundary-Scan	0	25	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32.

Table 69: **Types of Pins on Spartan-3 FPGAs *(Cont'd)***

Pin Type/ Color Code	Description	Pin Name
VREF	Dual-purpose pin that is either a user-I/O pin or, along with all other VREF pins in the same bank, provides a reference voltage input for certain I/O standards. If used for a reference voltage within a bank, all VREF pins within the bank must be connected.	IO/VREF_# IO_Lxxy_#/VREF_#
GND	Dedicated ground pin. The number of GND pins depends on the package used. All must be connected.	GND
VCCAUX	Dedicated auxiliary power supply pin. The number of VCCAUX pins depends on the package used. All must be connected to +2.5V.	VCCAUX
VCCINT	Dedicated internal core logic power supply pin. The number of VCCINT pins depends on the package used. All must be connected to +1.2V.	VCCINT
VCCO	Dedicated I/O bank, output buffer power supply pin. Along with other VCCO pins in the same bank, this pin supplies power to the output buffers within the I/O bank and sets the input threshold voltage for some I/O standards.	VCCO_# **CP132 and TQ144 Packages Only:** VCCO_LEFT, VCCO_TOP, VCCO_RIGHT, VCCO_BOTTOM
GCLK	Dual-purpose pin that is either a user-I/O pin or an input to a specific global buffer input. Every package has eight dedicated GCLK pins.	IO_Lxxy_#/GCLK0, IO_Lxxy_#/GCLK1, IO_Lxxy_#/GCLK2, IO_Lxxy_#/GCLK3, IO_Lxxy_#/GCLK4, IO_Lxxy_#/GCLK5, IO_Lxxy_#/GCLK6, IO_Lxxy_#/GCLK7
N.C.	This package pin is not connected in this specific device/package combination but may be connected in larger devices in the same package.	N.C.

Notes:

1. # = I/O bank number, an integer between 0 and 7.

I/Os with Lxxy_# are part of a differential output pair. 'L' indicates differential output capability. The "xx" field is a two-digit integer, unique to each bank that identifies a differential pin-pair. The 'y' field is either 'P' for the true signal or 'N' for the inverted signal in the differential pair. The '#' field is the I/O bank number.

Pin Definitions

Table 70 provides a brief description of each pin listed in the Spartan-3 FPGA pinout tables and package footprint diagrams. Pins are categorized by their pin type, as listed in Table 69. See Detailed, Functional Pin Descriptions for more information.

FG320: 320-lead Fine-pitch Ball Grid Array

The 320-lead fine-pitch ball grid array package, FG320, supports three different Spartan-3 devices, including the XC3S400, the XC3S1000, and the XC3S1500. The footprint for all three devices is identical, as shown in Table 98 and Figure 50.

The FG320 package is an 18 x 18 array of solder balls minus the four center balls.

All the package pins appear in Table 98 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

Pinout Table

Table 98: **FG320 Package Pinout**

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
0	IO	D9	I/O
0	IO	E7	I/O
0	IO/VREF_0	B3	VREF
0	IO/VREF_0	D6	VREF
0	IO_L01N_0/VRP_0	A2	DCI
0	IO_L01P_0/VRN_0	A3	DCI
0	IO_L09N_0	B4	I/O
0	IO_L09P_0	C4	I/O
0	IO_L10N_0	C5	I/O
0	IO_L10P_0	D5	I/O
0	IO_L15N_0	A4	I/O
0	IO_L15P_0	A5	I/O
0	IO_L25N_0	B5	I/O
0	IO_L25P_0	B6	I/O
0	IO_L27N_0	C7	I/O
0	IO_L27P_0	D7	I/O
0	IO_L28N_0	C8	I/O
0	IO_L28P_0	D8	I/O
0	IO_L29N_0	E8	I/O
0	IO_L29P_0	F8	I/O
0	IO_L30N_0	A7	I/O
0	IO_L30P_0	A8	I/O
0	IO_L31N_0	B9	I/O
0	IO_L31P_0/VREF_0	A9	VREF
0	IO_L32N_0/GCLK7	E9	GCLK
0	IO_L32P_0/GCLK6	F9	GCLK
0	VCCO_0	B8	VCCO
0	VCCO_0	C6	VCCO
0	VCCO_0	G8	VCCO

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
N/A	VCCINT	N6	VCCINT
N/A	VCCINT	N7	VCCINT
VCCAUX	CCLK	T15	CONFIG
VCCAUX	DONE	R15	CONFIG
VCCAUX	HSWAP_EN	E6	CONFIG
VCCAUX	M0	P5	CONFIG
VCCAUX	M1	U3	CONFIG
VCCAUX	M2	R4	CONFIG
VCCAUX	PROG_B	E5	CONFIG
VCCAUX	TCK	E14	JTAG
VCCAUX	TDI	D4	JTAG
VCCAUX	TDO	D15	JTAG
VCCAUX	TMS	B16	JTAG

User I/Os by Bank

Table 99 indicates how the available user-I/O pins are distributed between the eight I/O banks on the FG320 package.

Table 99: **User I/Os Per Bank in FG320 Package**

Package Edge	I/O Bank	Maximum I/O	Maximum LVDS Pairs	All Possible I/O Pins by Type				
				I/O	DUAL	DCI	VREF	GCLK
Top	0	26	11	19	0	2	3	2
	1	26	11	19	0	2	3	2
Right	2	29	14	23	0	2	4	0
	3	29	14	23	0	2	4	0
Bottom	4	27	11	13	6	2	4	2
	5	26	11	13	6	2	3	2
Left	6	29	14	23	0	2	4	0
	7	29	14	23	0	2	4	0

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	W9	VREF
5	IO_L27P_5	IO_L27P_5	V9	I/O
5	IO_L28N_5/D6	IO_L28N_5/D6	AB9	DUAL
5	IO_L28P_5/D7	IO_L28P_5/D7	AA9	DUAL
5	IO_L29N_5	IO_L29N_5	Y10	I/O
5	IO_L29P_5/VREF_5	IO_L29P_5/VREF_5	W10	VREF
5	IO_L30N_5	IO_L30N_5	AB10	I/O
5	IO_L30P_5	IO_L30P_5	AA10	I/O
5	IO_L31N_5/D4	IO_L31N_5/D4	W11	DUAL
5	IO_L31P_5/D5	IO_L31P_5/D5	V11	DUAL
5	IO_L32N_5/GCLK3	IO_L32N_5/GCLK3	AA11	GCLK
5	IO_L32P_5/GCLK2	IO_L32P_5/GCLK2	Y11	GCLK
5	VCCO_5	VCCO_5	T9	VCCO
5	VCCO_5	VCCO_5	T10	VCCO
5	VCCO_5	VCCO_5	T11	VCCO
5	VCCO_5	VCCO_5	U8	VCCO
5	VCCO_5	VCCO_5	Y8	VCCO
6	IO	IO	Y1	I/O
6	IO_L01N_6/VRP_6	IO_L01N_6/VRP_6	Y3	DCI
6	IO_L01P_6/VRN_6	IO_L01P_6/VRN_6	Y2	DCI
6	IO_L16N_6	IO_L16N_6	W4	I/O
6	IO_L16P_6	IO_L16P_6	W3	I/O
6	IO_L17N_6	IO_L17N_6	W2	I/O
6	IO_L17P_6/VREF_6	IO_L17P_6/VREF_6	W1	VREF
6	IO_L19N_6	IO_L19N_6	V5	I/O
6	IO_L19P_6	IO_L19P_6	U5	I/O
6	IO_L20N_6	IO_L20N_6	V4	I/O
6	IO_L20P_6	IO_L20P_6	V3	I/O
6	IO_L21N_6	IO_L21N_6	V2	I/O
6	IO_L21P_6	IO_L21P_6	V1	I/O
6	IO_L22N_6	IO_L22N_6	T6	I/O
6	IO_L22P_6	IO_L22P_6	T5	I/O
6	IO_L23N_6	IO_L23N_6	U4	I/O
6	IO_L23P_6	IO_L23P_6	T4	I/O
6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	U3	VREF
6	IO_L24P_6	IO_L24P_6	U2	I/O
6	N.C. (◆)	IO_L26N_6	T3	I/O
6	N.C. (◆)	IO_L26P_6	R4	I/O
6	IO_L27N_6	IO_L27N_6	T2	I/O
6	IO_L27P_6	IO_L27P_6	T1	I/O

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
0	IO_L09N_0	IO_L09N_0	IO_L09N_0	IO_L09N_0	IO_L09N_0	E7	I/O
0	IO_L09P_0	IO_L09P_0	IO_L09P_0	IO_L09P_0	IO_L09P_0	D7	I/O
0	IO_L10N_0	IO_L10N_0	IO_L10N_0	IO_L10N_0	IO_L10N_0	B7	I/O
0	IO_L10P_0	IO_L10P_0	IO_L10P_0	IO_L10P_0	IO_L10P_0	A7	I/O
0	N.C. (◆)	IO_L11N_0	IO_L11N_0	IO_L11N_0	IO_L11N_0	G8	I/O
0	N.C. (◆)	IO_L11P_0	IO_L11P_0	IO_L11P_0	IO_L11P_0	F8	I/O
0	N.C. (◆)	IO_L12N_0	IO_L12N_0	IO_L12N_0	IO(3)	E8	I/O
0	N.C. (◆)	IO_L12P_0	IO_L12P_0	IO_L12P_0	IO(3)	D8	I/O
0	IO_L15N_0	IO_L15N_0	IO_L15N_0	IO_L15N_0	IO_L13P_0(3)	B8	I/O
0	IO_L15P_0	IO_L15P_0	IO_L15P_0	IO_L15P_0	IO(3)	A8	I/O
0	IO_L16N_0	IO_L16N_0	IO_L16N_0	IO_L16N_0	IO_L16N_0	G9	I/O
0	IO_L16P_0	IO_L16P_0	IO_L16P_0	IO_L16P_0	IO_L16P_0	F9	I/O
0	N.C. (◆)	IO_L17N_0	IO_L17N_0	IO_L17N_0	IO_L17N_0	E9	I/O
0	N.C. (◆)	IO_L17P_0	IO_L17P_0	IO_L17P_0	IO_L17P_0	D9	I/O
0	N.C. (◆)	IO_L18N_0	IO_L18N_0	IO_L18N_0	IO_L18N_0	C9	I/O
0	N.C. (◆)	IO_L18P_0	IO_L18P_0	IO_L18P_0	IO_L18P_0	B9	I/O
0	IO_L19N_0	IO_L19N_0	IO_L19N_0	IO_L19N_0	IO_L19N_0	F10	I/O
0	IO_L19P_0	IO_L19P_0	IO_L19P_0	IO_L19P_0	IO_L19P_0	E10	I/O
0	IO_L22N_0	IO_L22N_0	IO_L22N_0	IO_L22N_0	IO_L22N_0	D10	I/O
0	IO_L22P_0	IO_L22P_0	IO_L22P_0	IO_L22P_0	IO_L22P_0	C10	I/O
0	N.C. (◆)	IO_L23N_0	IO_L23N_0	IO_L23N_0	IO_L23N_0	B10	I/O
0	N.C. (◆)	IO_L23P_0	IO_L23P_0	IO_L23P_0	IO_L23P_0	A10	I/O
0	IO_L24N_0	IO_L24N_0	IO_L24N_0	IO_L24N_0	IO_L24N_0	G11	I/O
0	IO_L24P_0	IO_L24P_0	IO_L24P_0	IO_L24P_0	IO_L24P_0	F11	I/O
0	IO_L25N_0	IO_L25N_0	IO_L25N_0	IO_L25N_0	IO_L25N_0	E11	I/O
0	IO_L25P_0	IO_L25P_0	IO_L25P_0	IO_L25P_0	IO_L25P_0	D11	I/O
0	N.C. (◆)	IO_L26N_0	IO_L26N_0	IO_L26N_0	IO_L26N_0	B11	I/O
0	N.C. (◆)	IO_L26P_0/VREF_0	IO_L26P_0/VREF_0	IO_L26P_0/VREF_0	IO_L26P_0/VREF_0	A11	VREF
0	IO_L27N_0	IO_L27N_0	IO_L27N_0	IO_L27N_0	IO_L27N_0	G12	I/O
0	IO_L27P_0	IO_L27P_0	IO_L27P_0	IO_L27P_0	IO_L27P_0	H13	I/O
0	IO_L28N_0	IO_L28N_0	IO_L28N_0	IO_L28N_0	IO_L28N_0	F12	I/O
0	IO_L28P_0	IO_L28P_0	IO_L28P_0	IO_L28P_0	IO_L28P_0	E12	I/O
0	IO_L29N_0	IO_L29N_0	IO_L29N_0	IO_L29N_0	IO_L29N_0	B12	I/O
0	IO_L29P_0	IO_L29P_0	IO_L29P_0	IO_L29P_0	IO_L29P_0	A12	I/O
0	IO_L30N_0	IO_L30N_0	IO_L30N_0	IO_L30N_0	IO_L30N_0	G13	I/O
0	IO_L30P_0	IO_L30P_0	IO_L30P_0	IO_L30P_0	IO_L30P_0	F13	I/O
0	IO_L31N_0	IO_L31N_0	IO_L31N_0	IO_L31N_0	IO_L31N_0	D13	I/O
0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	C13	VREF
0	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	B13	GCLK
0	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	A13	GCLK
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	C7	VCCO
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	C11	VCCO

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
4	IO_L22N_4/VREF_4	IO_L22N_4/VREF_4	IO_L22N_4/VREF_4	IO_L22N_4/VREF_4	IO_L22N_4/VREF_4	AD17	VREF
4	IO_L22P_4	IO_L22P_4	IO_L22P_4	IO_L22P_4	IO_L22P_4	AB17	I/O
4	N.C. (◆)	IO_L23N_4	IO_L23N_4	IO_L23N_4	IO_L23N_4	AE17	I/O
4	N.C. (◆)	IO_L23P_4	IO_L23P_4	IO_L23P_4	IO_L23P_4	AF17	I/O
4	IO_L24N_4	IO_L24N_4	IO_L24N_4	IO_L24N_4	IO_L24N_4	Y16	I/O
4	IO_L24P_4	IO_L24P_4	IO_L24P_4	IO_L24P_4	IO_L24P_4	AA16	I/O
4	IO_L25N_4	IO_L25N_4	IO_L25N_4	IO_L25N_4	IO_L25N_4	AB16	I/O
4	IO_L25P_4	IO_L25P_4	IO_L25P_4	IO_L25P_4	IO_L25P_4	AC16	I/O
4	N.C. (◆)	IO_L26N_4	IO_L26N_4	IO_L26N_4	IO_L26N_4	AE16	I/O
4	N.C. (◆)	IO_L26P_4/VREF_4	IO_L26P_4/VREF_4	IO_L26P_4/VREF_4	IO_L26P_4/VREF_4	AF16	VREF
4	IO_L27N_4/DIN/D0	IO_L27N_4/DIN/D0	IO_L27N_4/DIN/D0	IO_L27N_4/DIN/D0	IO_L27N_4/DIN/D0	Y15	DUAL
4	IO_L27P_4/D1	IO_L27P_4/D1	IO_L27P_4/D1	IO_L27P_4/D1	IO_L27P_4/D1	W14	DUAL
4	IO_L28N_4	IO_L28N_4	IO_L28N_4	IO_L28N_4	IO_L28N_4	AA15	I/O
4	IO_L28P_4	IO_L28P_4	IO_L28P_4	IO_L28P_4	IO_L28P_4	AB15	I/O
4	IO_L29N_4	IO_L29N_4	IO_L29N_4	IO_L29N_4	IO_L29N_4	AE15	I/O
4	IO_L29P_4	IO_L29P_4	IO_L29P_4	IO_L29P_4	IO_L29P_4	AF15	I/O
4	IO_L30N_4/D2	IO_L30N_4/D2	IO_L30N_4/D2	IO_L30N_4/D2	IO_L30N_4/D2	Y14	DUAL
4	IO_L30P_4/D3	IO_L30P_4/D3	IO_L30P_4/D3	IO_L30P_4/D3	IO_L30P_4/D3	AA14	DUAL
4	IO_L31N_4/INIT_B	IO_L31N_4/INIT_B	IO_L31N_4/INIT_B	IO_L31N_4/INIT_B	IO_L31N_4/INIT_B	AC14	DUAL
4	IO_L31P_4/ DOUT/BUSY	IO_L31P_4/ DOUT/BUSY	IO_L31P_4/ DOUT/BUSY	IO_L31P_4/ DOUT/BUSY	IO_L31P_4/ DOUT/BUSY	AD14	DUAL
4	IO_L32N_4/GCLK1	IO_L32N_4/GCLK1	IO_L32N_4/GCLK1	IO_L32N_4/GCLK1	IO_L32N_4/GCLK1	AE14	GCLK
4	IO_L32P_4/GCLK0	IO_L32P_4/GCLK0	IO_L32P_4/GCLK0	IO_L32P_4/GCLK0	IO_L32P_4/GCLK0	AF14	GCLK
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	AD16	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	AD20	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	U14	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	V14	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	V15	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	V16	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	W17	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	W18	VCCO
5	IO	IO	IO	IO	IO	AA7	I/O
5	IO	IO	IO	IO	IO	AA13	I/O
5	IO	IO	IO	IO	IO_L17P_5[3]	AB9	I/O
5	N.C. (◆)	IO	IO	IO	IO_L17N_5[3]	AC9	I/O
5	IO	IO	IO	IO	IO	AC11	I/O
5	IO	IO	IO	IO	IO	AD10	I/O
5	IO	IO	IO	IO	IO	AD12	I/O
5	IO	IO	IO	IO	IO	AF4	I/O
5	IO	IO	IO	IO	IO	Y8	I/O
5	IO/VREF_5	IO/VREF_5	IO/VREF_5	IO/VREF_5	IO/VREF_5	AF5	VREF
5	IO/VREF_5	IO/VREF_5	IO/VREF_5	IO/VREF_5	IO/VREF_5	AF13	VREF
5	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	AC5	DUAL

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
1	IO_L05P_1	IO_L05P_1	F25	I/O
1	IO_L06N_1/VREF_1	IO_L06N_1/VREF_1	C24	VREF
1	IO_L06P_1	IO_L06P_1	D24	I/O
1	IO_L07N_1	IO_L07N_1	A24	I/O
1	IO_L07P_1	IO_L07P_1	B24	I/O
1	IO_L08N_1	IO_L08N_1	H23	I/O
1	IO_L08P_1	IO_L08P_1	G24	I/O
1	IO_L09N_1	IO_L09N_1	F23	I/O
1	IO_L09P_1	IO_L09P_1	G23	I/O
1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	C23	VREF
1	IO_L10P_1	IO_L10P_1	D23	I/O
1	IO_L11N_1	IO_L11N_1	A23	I/O
1	IO_L11P_1	IO_L11P_1	B23	I/O
1	IO_L12N_1	IO_L12N_1	H22	I/O
1	IO_L12P_1	IO_L12P_1	J22	I/O
1	IO_L13N_1	IO_L13N_1	F22	I/O
1	IO_L13P_1	IO_L13P_1	E23	I/O
1	IO_L14N_1	IO_L14N_1	D22	I/O
1	IO_L14P_1	IO_L14P_1	E22	I/O
1	IO_L15N_1	IO_L15N_1	A22	I/O
1	IO_L15P_1	IO_L15P_1	B22	I/O
1	IO_L16N_1	IO_L16N_1	F21	I/O
1	IO_L16P_1	IO_L16P_1	G21	I/O
1	IO_L17N_1/VREF_1	IO_L17N_1/VREF_1	B21	VREF
1	IO_L17P_1	IO_L17P_1	C21	I/O
1	IO_L18N_1	IO_L18N_1	G20	I/O
1	IO_L18P_1	IO_L18P_1	H20	I/O
1	IO_L19N_1	IO_L19N_1	E20	I/O
1	IO_L19P_1	IO_L19P_1	F20	I/O
1	IO_L20N_1	IO_L20N_1	C20	I/O
1	IO_L20P_1	IO_L20P_1	D20	I/O
1	IO_L21N_1	IO_L21N_1	A20	I/O
1	IO_L21P_1	IO_L21P_1	B20	I/O
1	IO_L22N_1	IO_L22N_1	J19	I/O
1	IO_L22P_1	IO_L22P_1	K19	I/O
1	IO_L23N_1	IO_L23N_1	G19	I/O
1	IO_L23P_1	IO_L23P_1	H19	I/O
1	IO_L24N_1	IO_L24N_1	E19	I/O
1	IO_L24P_1	IO_L24P_1	F19	I/O
1	IO_L25N_1	IO_L25N_1	C19	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
N/A	GND	GND	T12	GND
N/A	GND	GND	N13	GND
N/A	GND	GND	P13	GND
N/A	GND	GND	R13	GND
N/A	GND	GND	T13	GND
N/A	GND	GND	U13	GND
N/A	GND	GND	V13	GND
N/A	GND	GND	A14	GND
N/A	GND	GND	E14	GND
N/A	GND	GND	H14	GND
N/A	GND	GND	N14	GND
N/A	GND	GND	P14	GND
N/A	GND	GND	R14	GND
N/A	GND	GND	T14	GND
N/A	GND	GND	U14	GND
N/A	GND	GND	V14	GND
N/A	GND	GND	AC14	GND
N/A	GND	GND	AF14	GND
N/A	GND	GND	AK14	GND
N/A	GND	GND	M15	GND
N/A	GND	GND	N15	GND
N/A	GND	GND	P15	GND
N/A	GND	GND	R15	GND
N/A	GND	GND	T15	GND
N/A	GND	GND	U15	GND
N/A	GND	GND	V15	GND
N/A	GND	GND	W15	GND
N/A	GND	GND	M16	GND
N/A	GND	GND	N16	GND
N/A	GND	GND	P16	GND
N/A	GND	GND	R16	GND
N/A	GND	GND	T16	GND
N/A	GND	GND	U16	GND
N/A	GND	GND	V16	GND
N/A	GND	GND	W16	GND
N/A	GND	GND	A17	GND
N/A	GND	GND	E17	GND
N/A	GND	GND	H17	GND
N/A	GND	GND	N17	GND
N/A	GND	GND	P17	GND

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
7	IO_L45P_7	IO_L45P_7	M2	I/O
7	IO_L46N_7	IO_L46N_7	N7	I/O
7	IO_L46P_7	IO_L46P_7	N8	I/O
7	N.C. (◆)	IO_L47N_7	P9	I/O
7	N.C. (◆)	IO_L47P_7	P10	I/O
7	IO_L49N_7	IO_L49N_7	P1	I/O
7	IO_L49P_7	IO_L49P_7	P2	I/O
7	IO_L50N_7	IO_L50N_7	R10	I/O
7	IO_L50P_7	IO_L50P_7	R11	I/O
7	N.C. (◆)	IO_L51N_7	U11	I/O
7	N.C. (◆)	IO_L51P_7	T11	I/O
7	VCCO_7	VCCO_7	D3	VCCO
7	VCCO_7	VCCO_7	H3	VCCO
7	VCCO_7	VCCO_7	H7	VCCO
7	VCCO_7	VCCO_7	L4	VCCO
7	VCCO_7	VCCO_7	L8	VCCO
7	VCCO_7	VCCO_7	N12	VCCO
7	VCCO_7	VCCO_7	N2	VCCO
7	VCCO_7	VCCO_7	N6	VCCO
7	VCCO_7	VCCO_7	P12	VCCO
7	VCCO_7	VCCO_7	R12	VCCO
7	VCCO_7	VCCO_7	R8	VCCO
7	VCCO_7	VCCO_7	T12	VCCO
7	VCCO_7	VCCO_7	T4	VCCO
N/A	GND	GND	A1	GND
N/A	GND	GND	A13	GND
N/A	GND	GND	A16	GND
N/A	GND	GND	A19	GND
N/A	GND	GND	A2	GND
N/A	GND	GND	A22	GND
N/A	GND	GND	A26	GND
N/A	GND	GND	A30	GND
N/A	GND	GND	A33	GND
N/A	GND	GND	A34	GND
N/A	GND	GND	A5	GND
N/A	GND	GND	A9	GND
N/A	GND	GND	AA14	GND
N/A	GND	GND	AA15	GND
N/A	GND	GND	AA16	GND
N/A	GND	GND	AA17	GND