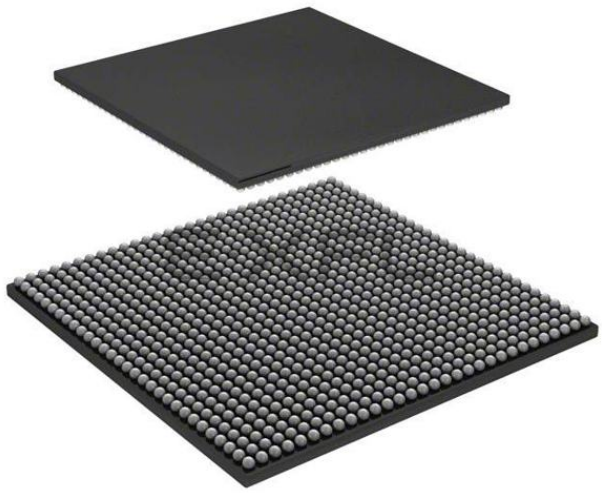
AMD Xilinx - XC3S5000-4FG900I Datasheet



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Details	
Product Status	Active
Number of LABs/CLBs	8320
Number of Logic Elements/Cells	74880
Total RAM Bits	1916928
Number of I/O	633
Number of Gates	5000000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	900-BBGA
Supplier Device Package	900-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s5000-4fg900i

Table 33: **General DC Characteristics of User I/O, Dual-Purpose, and Dedicated Pins**

Symbol	Description	Test Conditions		Min	Typ	Max	Units
I_L (2)(4)	Leakage current at User I/O, Dual-Purpose, and Dedicated pins	Driver is Hi-Z, V_{IN} = 0V or V_{CCO} max, sample-tested	$V_{CCO} \geq 3.0V$	–	-	±25	µA
			$V_{CCO} < 3.0V$	–	-	±10	µA
I_{RPU} (3)	Current through pull-up resistor at User I/O, Dual-Purpose, and Dedicated pins	V_{IN} = 0V, V_{CCO} = 3.3V		–0.84	-	–2.35	mA
		V_{IN} = 0V, V_{CCO} = 3.0V		–0.69	-	–1.99	mA
		V_{IN} = 0V, V_{CCO} = 2.5V		–0.47	-	–1.41	mA
		V_{IN} = 0V, V_{CCO} = 1.8V		–0.21	-	–0.69	mA
		V_{IN} = 0V, V_{CCO} = 1.5V		–0.13	-	–0.43	mA
		V_{IN} = 0V, V_{CCO} = 1.2V		–0.06	-	–0.22	mA
R_{PU} (3)	Equivalent resistance of pull-up resistor at User I/O, Dual-Purpose, and Dedicated pins, derived from I_{RPU}	V_{CCO} = 3.0V to 3.465V		1.27	-	4.11	kΩ
		V_{CCO} = 2.3V to 2.7V		1.15	-	3.25	kΩ
		V_{CCO} = 1.7V to 1.9V		2.45	-	9.10	kΩ
		V_{CCO} = 1.4V to 1.6V		3.25	-	12.10	kΩ
		V_{CCO} = 1.14 to 1.26V		5.15	-	21.00	kΩ
I_{RPD} (3)	Current through pull-down resistor at User I/O, Dual-Purpose, and Dedicated pins	$V_{IN} = V_{CCO}$		0.37	-	1.67	mA
R_{PD} (3)	Equivalent resistance of pull-down resistor at User I/O, Dual-Purpose, and Dedicated pins, driven from I_{RPD}	$V_{IN} = V_{CCO}$ = 3.0V to 3.465V		1.75	-	9.35	kΩ
		$V_{IN} = V_{CCO}$ = 2.3V to 2.7V		1.35	-	7.30	kΩ
		$V_{IN} = V_{CCO}$ = 1.7V to 1.9V		1.00	-	5.15	kΩ
		$V_{IN} = V_{CCO}$ = 1.4V to 1.6V		0.85	-	4.35	kΩ
		$V_{IN} = V_{CCO}$ = 1.14 to 1.26V		0.68	-	3.465	kΩ
R_{DCI}	Value of external reference resistor to support DCI I/O standards			20	-	100	Ω
I_{REF}	V_{REF} current per pin	$V_{CCO} \geq 3.0V$		–	-	±25	µA
		$V_{CCO} < 3.0V$		–	-	±10	µA
C_{IN}	Input capacitance			3	-	10	pF

Notes:

1. The numbers in this table are based on the conditions set forth in Table 32.
2. The I_L specification applies to every I/O pin throughout power-on as long as the voltage on that pin stays between the absolute V_{IN} minimum and maximum values (Table 28). For hot-swap applications, at the time of card connection, be sure to keep all I/O voltages within this range before applying V_{CCO} power. Consider applying V_{CCO} power before connecting the signal lines, to avoid turning on the ESD protection diodes, shown in Module 2: Figure 7, page 11. When the FPGA is completely unpowered, the I/O pins are high impedance, but there is a path through the upper and lower ESD protection diodes.
3. This parameter is based on characterization. The pull-up resistance $R_{PU} = V_{CCO} / I_{RPU}$. The pull-down resistance $R_{PD} = V_{IN} / I_{RPD}$. Spartan-3 family values for both resistances are stronger than they have been for previous FPGA families.
4. For single-ended signals that are placed on a differential-capable I/O, V_{IN} of –0.2V to –0.3V is supported but can cause increased leakage between the two pins. See the *Parasitic Leakage* section in UG331, *Spartan-3 Generation FPGA User Guide*.

I/O Timing

Table 40: **Pin-to-Pin Clock-to-Output Times for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max(2)	Max(2)	
Clock-to-Output Times						
$T_{ICKOFDCM}$	When reading from the Output Flip-Flop (OFF), the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is in use.	LVCMOS25(3), 12 mA output drive, Fast slew rate, with DCM(4)	XC3S50	2.04	2.35	ns
			XC3S200	1.45	1.75	ns
			XC3S400	1.45	1.75	ns
			XC3S1000	2.07	2.39	ns
			XC3S1500	2.05	2.36	ns
			XC3S2000	2.03	2.34	ns
			XC3S4000	1.94	2.24	ns
			XC3S5000	2.00	2.30	ns
T_{ICKOF}	When reading from OFF, the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is not in use.	LVCMOS25(3), 12 mA output drive, Fast slew rate, without DCM	XC3S50	3.70	4.24	ns
			XC3S200	3.89	4.46	ns
			XC3S400	3.91	4.48	ns
			XC3S1000	4.00	4.59	ns
			XC3S1500	4.07	4.66	ns
			XC3S2000	4.19	4.80	ns
			XC3S4000	4.44	5.09	ns
			XC3S5000	4.38	5.02	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32 and Table 35.
2. For minimums, use the values reported by the Xilinx timing analyzer.
3. This clock-to-output time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or a standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. If the former is true, *add* the appropriate Input adjustment from Table 44. If the latter is true, *add* the appropriate Output adjustment from Table 47.
4. DCM output jitter is included in all measurements.

Table 43: **Propagation Times for the IOB Input Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Propagation Times						
T_{IOPLI}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with no input delay programmed	LVCMOS25(2), IOBDELAY = NONE	XC3S50	2.01	2.31	ns
			XC3S200	1.50	1.72	ns
			XC3S400	1.50	1.72	ns
			XC3S1000	2.01	2.31	ns
			XC3S1500	2.01	2.31	ns
			XC3S2000	2.01	2.31	ns
			XC3S4000	2.09	2.41	ns
			XC3S5000	2.18	2.51	ns
T_{IOPLID}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with the input delay programmed	LVCMOS25(2), IOBDELAY = IFD	XC3S50	4.75	5.46	ns
			XC3S200	4.89	5.62	ns
			XC3S400	4.76	5.48	ns
			XC3S1000	5.38	6.18	ns
			XC3S1500	5.76	6.62	ns
			XC3S2000	7.04	8.09	ns
			XC3S4000	7.52	8.65	ns
			XC3S5000	7.69	8.84	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32 and Table 35.
2. This propagation time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. When this is true, *add* the appropriate Input adjustment from Table 44.

Table 44: **Input Timing Adjustments for IOB**

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Single-Ended Standards			
GTL, GTL_DCI	0.44	0.50	ns
GTLP, GTLP_DCI	0.36	0.42	ns
HSLVDCI_15	0.51	0.59	ns
HSLVDCI_18	0.29	0.33	ns
HSLVDCI_25	0.51	0.59	ns
HSLVDCI_33	0.51	0.59	ns
HSTL_I, HSTL_I_DCI	0.51	0.59	ns
HSTL_III, HSTL_III_DCI	0.37	0.42	ns
HSTL_I_18, HSTL_I_DCI_18	0.36	0.41	ns
HSTL_II_18, HSTL_II_DCI_18	0.39	0.45	ns
HSTL_III_18, HSTL_III_DCI_18	0.45	0.52	ns
LVCMOS12	0.63	0.72	ns

Simultaneously Switching Output Guidelines

This section provides guidelines for the maximum allowable number of Simultaneous Switching Outputs (SSOs). These guidelines describe the maximum number of user I/O pins, of a given output signal standard, that should simultaneously switch in the same direction, while maintaining a safe level of switching noise. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of ground and power bounce.

Ground or power bounce occurs when a large number of outputs simultaneously switch in the same direction. The output drive transistors all conduct current to a common voltage rail. Low-to-High transitions conduct to the V_{CCO} rail; High-to-Low transitions conduct to the GND rail. The resulting cumulative current transient induces a voltage difference across the inductance that exists between the die pad and the power supply or ground return. The inductance is associated with bonding wires, the package lead frame, and any other signal routing inside the package. Other variables contribute to SSO noise levels, including stray inductance on the PCB as well as capacitive loading at receivers. Any SSO-induced voltage consequently affects internal switching noise margins and ultimately signal quality.

Table 49 and Table 50 provide the essential SSO guidelines. For each device/package combination, Table 49 provides the number of equivalent V_{CCO}/GND pairs. The equivalent number of pairs is based on characterization and will possibly not match the physical number of pairs. For each output signal standard and drive strength, Table 50 recommends the maximum number of SSOs, switching in the same direction, allowed per V_{CCO}/GND pair within an I/O bank. The Table 50 guidelines are categorized by package style. Multiply the appropriate numbers from Table 49 and Table 50 to calculate the maximum number of SSOs allowed within an I/O bank. Exceeding these SSO guidelines may result in increased power or ground bounce, degraded signal integrity, or increased system jitter.

SSO_{MAX}/IO Bank = Table 49 x Table 50

The recommended maximum SSO values assume that the FPGA is soldered on the printed circuit board and that the board uses sound design practices. The SSO values do not apply for FPGAs mounted in sockets, due to the lead inductance introduced by the socket.

The number of SSOs allowed for quad-flat packages (VQ, TQ, PQ) is lower than for ball grid array packages (FG) due to the larger lead inductance of the quad-flat packages. Ball grid array packages are recommended for applications with a large number of simultaneously switching outputs.

Table 49: **Equivalent V_{CCO}/GND Pairs per Bank**

Device	VQ100	CP132 (1)(2)	TQ144 (1)	PQ208	FT256	FG320	FG456	FG676	FG900	FG1156 (2)
XC3S50	1	1.5	1.5	2	–	–	–	–	–	–
XC3S200	1	–	1.5	2	3	–	–	–	–	–
XC3S400	–	–	1.5	2	3	3	5	–	–	–
XC3S1000	–	–	–	–	3	3	5	5	–	–
XC3S1500	–	–	–	–	–	3	5	6	–	–
XC3S2000	–	–	–	–	–	–	5	6	9	–
XC3S4000	–	–	–	–	–	–	–	6	10	12
XC3S5000	–	–	–	–	–	–	–	6	10	12

Notes:

1. The V_{CCO} lines for the pair of banks on each side of the CP132 and TQ144 packages are internally tied together. Each pair of interconnected banks shares three V_{CCO}/GND pairs. Consequently, the per bank number is 1.5.
2. The CP132, CPG132, FG1156, and FGG1156 packages are discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.
3. The information in this table also applies to Pb-free packages.

Miscellaneous DCM Timing

Table 64: **Miscellaneous DCM Timing**

Symbol	Description	DLL Frequency Mode	Temperature Range		Units
			Commercial	Industrial	
DCM_INPUT_CLOCK_STOP	Maximum duration that the CLKIN and CLKFB signals can be stopped(1,2)	Any	100	100	ms
DCM_RST_PW_MIN	Minimum duration of a RST pulse width	Any	3	3	CLKIN cycles
DCM_RST_PW_MAX(3)	Maximum duration of a RST pulse width(1,2)	Low	N/A	N/A	seconds
		High	N/A	10	seconds
DCM_CONFIG_LAG_TIME(4)	Maximum duration from V_{CCINT} applied to FPGA configuration successfully completed (DONE pin goes High) and clocks applied to DCM DLL(1,2)	Low	N/A	N/A	minutes
		High	N/A	10	minutes

Notes:

1. These limits only apply to applications that use the DCM DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV). The DCM DFS outputs (CLKFX, CLKFX180) are unaffected. Required due to effects of device cooling: see “Momentarily Stopping CLKIN” in Chapter 3 of UG331.
2. Industrial-temperature applications that use the DLL in High-Frequency mode must use a continuous or increasing operating frequency. The DLL under these conditions does not support reducing the operating frequency once establishing an initial operating frequency.
3. This specification is equivalent to the Virtex-4 FPGA DCM_RESET specification.
4. This specification is equivalent to the Virtex-4 FPGA TCONFIG specification.

User I/Os by Bank

Table 97 indicates how the available user-I/O pins are distributed between the eight I/O banks on the FT256 package.

Table 97: **User I/Os Per Bank in FT256 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	20	13	0	2	3	2
	1	20	13	0	2	3	2
Right	2	23	18	0	2	3	0
	3	23	18	0	2	3	0
Bottom	4	21	8	6	2	3	2
	5	20	7	6	2	3	2
Left	6	23	18	0	2	3	0
	7	23	18	0	2	3	0

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
N/A	GND	GND	B21	GND
N/A	GND	GND	C9	GND
N/A	GND	GND	C14	GND
N/A	GND	GND	J3	GND
N/A	GND	GND	J9	GND
N/A	GND	GND	J10	GND
N/A	GND	GND	J11	GND
N/A	GND	GND	J12	GND
N/A	GND	GND	J13	GND
N/A	GND	GND	J14	GND
N/A	GND	GND	J20	GND
N/A	GND	GND	K9	GND
N/A	GND	GND	K10	GND
N/A	GND	GND	K11	GND
N/A	GND	GND	K12	GND
N/A	GND	GND	K13	GND
N/A	GND	GND	K14	GND
N/A	GND	GND	L9	GND
N/A	GND	GND	L10	GND
N/A	GND	GND	L11	GND
N/A	GND	GND	L12	GND
N/A	GND	GND	L13	GND
N/A	GND	GND	L14	GND
N/A	GND	GND	M9	GND
N/A	GND	GND	M10	GND
N/A	GND	GND	M11	GND
N/A	GND	GND	M12	GND
N/A	GND	GND	M13	GND
N/A	GND	GND	M14	GND
N/A	GND	GND	N9	GND
N/A	GND	GND	N10	GND
N/A	GND	GND	N11	GND
N/A	GND	GND	N12	GND
N/A	GND	GND	N13	GND
N/A	GND	GND	N14	GND
N/A	GND	GND	P3	GND
N/A	GND	GND	P9	GND
N/A	GND	GND	P10	GND
N/A	GND	GND	P11	GND
N/A	GND	GND	P12	GND

FG456 Footprint

Left Half of FG456 Package (Top View)

XC3S400 (264 max. user I/O)

196 **I/O:** Unrestricted, general-purpose user I/O

32 **VREF:** User I/O or input voltage reference for bank

69 **N.C.:** Unconnected pins for XC3S400 (◆)

XC3S1000, XC3S1500, XC3S2000 (333 max user I/O)

261 **I/O:** Unrestricted, general-purpose user I/O

36 **VREF:** User I/O or input voltage reference for bank

0 **N.C.:** No unconnected pins in this package

All devices

12 **DUAL:** Configuration pin, then possible user I/O

8 **GCLK:** User I/O or global clock buffer input

16 **DCI:** User I/O or reference resistor input for bank

7 **CONFIG:** Dedicated configuration pins

4 **JTAG:** Dedicated JTAG port pins

12 **VCCINT:** Internal core voltage supply (+1.2V)

40 **VCCO:** Output voltage supply for bank

8 **VCCAUX:** Auxiliary voltage supply (+2.5V)

52 **GND:** Ground

	Bank 0										
	1	2	3	4	5	6	7	8	9	10	11
A	GND	PROG_B	IO VREF_0	I/O L01P_0 VRN_0	I/O L09P_0	VCCAUX	I/O L19P_0 ◆	I/O L24P_0	I/O L27P_0	I/O	I/O L32P_0 GCLK6
B	TDI	GND	HSWAP_EN	I/O L01N_0 VRP_0	I/O L09N_0	I/O L15P_0	I/O L19N_0 ◆	I/O L24N_0	I/O L27N_0	I/O L29P_0	I/O L32N_0 GCLK7
C	I/O L16P_7 VREF_7	I/O	I/O L01N_7 VRP_7	I/O L01P_7 VRN_7	I/O L06P_0	I/O L15N_0	IO VREF_0	VCCO_0	GND	I/O L29N_0	I/O L31P_0 VREF_0
D	I/O L16N_7	I/O L19P_7	I/O L19N_7 VREF_7	I/O L17P_7	I/O L06N_0	I/O L10P_0	I/O L16P_0	I/O L22P_0 ◆	I/O	I/O	I/O L31N_0
E	I/O L21N_7	I/O L21P_7	I/O L20P_7	I/O L17N_7	IO VREF_0 ◆	I/O L10N_0	I/O L16N_0	I/O L22N_0 ◆	I/O L25P_0	I/O L28P_0	I/O L30P_0
F	VCCAUX	I/O L23N_7	I/O L23P_7	I/O L20N_7	I/O L22P_7	I/O	IO VREF_0	VCCO_0	I/O L25N_0	I/O L28N_0	I/O L30N_0
G	I/O L27N_7	I/O L27P_7 VREF_7	I/O L26N_7 ◆	I/O L26P_7 ◆	I/O L24P_7	I/O L22N_7	VCCINT	VCCINT	VCCO_0	VCCO_0	VCCO_0
H	I/O L28N_7 ◆	I/O L28P_7 ◆	VCCO_7	I/O L29P_7 ◆	I/O L24N_7	VCCO_7	VCCINT				
J	I/O L32N_7 ◆	I/O L32P_7 ◆	GND	I/O L29N_7 ◆	I/O L31N_7 ◆	I/O L31P_7 ◆	VCCO_7		GND	GND	GND
K	I/O L35N_7	I/O L35P_7	I/O L34N_7	I/O L34P_7	I/O L33N_7 ◆	I/O L33P_7 ◆	VCCO_7		GND	GND	GND
L	I/O L40N_7 VREF_7	I/O L40P_7	I/O L39N_7	I/O L39P_7	I/O L38N_7	I/O L38P_7	VCCO_7		GND	GND	GND
M	I/O L40P_6 VREF_6	I/O L40N_6	I/O L39P_6	I/O L39N_6	I/O L38P_6	I/O L38N_6	VCCO_6		GND	GND	GND
N	I/O L35P_6	I/O L35N_6	I/O L34P_6	I/O L34N_6 VREF_6	I/O L33P_6 ◆	I/O L33N_6 ◆	VCCO_6		GND	GND	GND
P	I/O L32P_6 ◆	I/O L32N_6 ◆	GND	I/O L31P_6 ◆	I/O L31N_6 ◆	I/O L28P_6 ◆	VCCO_6		GND	GND	GND
R	I/O L29P_6 ◆	I/O L29N_6 ◆	VCCO_6	I/O L26P_6 ◆	I/O L28N_6 ◆	VCCO_6	VCCINT				
T	I/O L27P_6	I/O L27N_6	I/O L26N_6 ◆	I/O L23P_6	I/O L22P_6	I/O L22N_6	VCCINT	VCCINT	VCCO_5	VCCO_5	VCCO_5
U	VCCAUX	I/O L24P_6	I/O L24N_6 VREF_6	I/O L23N_6	I/O L19P_6	IO VREF_5	I/O	VCCO_5	I/O ◆	I/O	I/O
V	I/O L21P_6	I/O L21N_6	I/O L20P_6	I/O L20N_6	I/O L19N_6	I/O L15P_5	I/O	I/O L24P_5	I/O L27P_5	I/O	I/O L31P_5 D5
W	I/O L17P_6 VREF_6	I/O L17N_6	I/O L16P_6	I/O L16N_6	I/O L09P_5	I/O L15N_5	I/O L19P_5 VREF_5 ◆	I/O L24N_5	I/O L27N_5 VREF_5	I/O L29P_5 VREF_5	I/O L31N_5 D4
Y	I/O	I/O L01P_6 VRN_6	I/O L01N_6 VRP_6	I/O L01N_5 RDWR_B	I/O L09N_5	I/O L16P_5	I/O L19N_5 ◆	VCCO_5	GND	I/O L29N_5	I/O L32P_5 GCLK2
AA	M1	GND	I/O L01P_5 CS_B	I/O L06P_5	I/O L10P_5 VRN_5	I/O L16N_5	I/O L22P_5 ◆	I/O L25P_5	I/O L28P_5 D7	I/O L30P_5	I/O L32N_5 GCLK3
AB	GND	M0	M2	I/O L06N_5	I/O L10N_5 VRP_5	VCCAUX	I/O L22N_5 ◆	I/O L25N_5	I/O L28N_5 D6	I/O L30N_5	IO VREF_5

Bank 7 (rows G–L) · Bank 6 (rows M–T) · Bank 5 (columns 7–11)

DS099-4_11a_030203

Figure 51: **FG456 Package Footprint (Top View)**

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	H9	VCCO
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	H10	VCCO
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	J11	VCCO
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	J12	VCCO
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	J13	VCCO
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	K13	VCCO
1	IO	IO	IO	IO	IO	A14	I/O
1	IO	IO	IO	IO	IO	A22	I/O
1	IO	IO	IO	IO	IO	A23	I/O
1	IO	IO	IO	IO	IO	D16	I/O
1	IO	IO	IO	IO	IO_L17P_1(3)	E18	I/O
1	IO	IO	IO	IO	IO	F14	I/O
1	IO	IO	IO	IO	IO	F20	I/O
1	IO	IO	IO	IO	IO	G19	I/O
1	IO/VREF_1	IO/VREF_1	IO/VREF_1	IO/VREF_1	IO/VREF_1	C15	VREF
1	IO/VREF_1	IO/VREF_1	IO/VREF_1	IO/VREF_1	IO/VREF_1	C17	VREF
1	N.C. (◆)	IO/VREF_1	IO/VREF_1	IO/VREF_1	IO_L17N_1/VREF_1(3)	D18	VREF
1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	D22	DCI
1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	E22	DCI
1	IO_L04N_1	IO_L04N_1	IO_L04N_1	IO_L04N_1	IO_L04N_1	B23	I/O
1	IO_L04P_1	IO_L04P_1	IO_L04P_1	IO_L04P_1	IO_L04P_1	C23	I/O
1	IO_L05N_1	IO_L05N_1	IO_L05N_1	IO_L05N_1	IO_L05N_1	E21	I/O
1	IO_L05P_1	IO_L05P_1	IO_L05P_1	IO_L05P_1	IO_L05P_1	F21	I/O
1	IO_L06N_1/VREF_1	IO_L06N_1/VREF_1	IO_L06N_1/VREF_1	IO_L06N_1/VREF_1	IO_L06N_1/VREF_1	B22	VREF
1	IO_L06P_1	IO_L06P_1	IO_L06P_1	IO_L06P_1	IO_L06P_1	C22	I/O
1	IO_L07N_1	IO_L07N_1	IO_L07N_1	IO_L07N_1	IO_L07N_1	C21	I/O
1	IO_L07P_1	IO_L07P_1	IO_L07P_1	IO_L07P_1	IO_L07P_1	D21	I/O
1	IO_L08N_1	IO_L08N_1	IO_L08N_1	IO_L08N_1	IO_L08N_1	A21	I/O
1	IO_L08P_1	IO_L08P_1	IO_L08P_1	IO_L08P_1	IO_L08P_1	B21	I/O
1	IO_L09N_1	IO_L09N_1	IO_L09N_1	IO_L09N_1	IO_L09N_1	D20	I/O
1	IO_L09P_1	IO_L09P_1	IO_L09P_1	IO_L09P_1	IO_L09P_1	E20	I/O
1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	A20	VREF
1	IO_L10P_1	IO_L10P_1	IO_L10P_1	IO_L10P_1	IO_L10P_1	B20	I/O
1	N.C. (◆)	IO_L11N_1	IO_L11N_1	IO_L11N_1	IO_L11N_1	E19	I/O
1	N.C. (◆)	IO_L11P_1	IO_L11P_1	IO_L11P_1	IO_L11P_1	F19	I/O
1	N.C. (◆)	IO_L12N_1	IO_L12N_1	IO_L12N_1	IO_L12N_1	C19	I/O
1	N.C. (◆)	IO_L12P_1	IO_L12P_1	IO_L12P_1	IO_L12P_1	D19	I/O
1	IO_L15N_1	IO_L15N_1	IO_L15N_1	IO_L15N_1	IO_L15N_1	A19	I/O
1	IO_L15P_1	IO_L15P_1	IO_L15P_1	IO_L15P_1	IO_L15P_1	B19	I/O
1	IO_L16N_1	IO_L16N_1	IO_L16N_1	IO_L16N_1	IO_L16N_1	F18	I/O
1	IO_L16P_1	IO_L16P_1	IO_L16P_1	IO_L16P_1	IO_L16P_1	G18	I/O
1	N.C. (◆)	IO_L18N_1	IO_L18N_1	IO_L18N_1	IO(3)	B18	I/O

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
7	IO_L29P_7	IO_L29P_7	IO_L29P_7	IO_L29P_7	IO_L29P_7	L2	I/O
7	IO_L31N_7	IO_L31N_7	IO_L31N_7	IO_L31N_7	IO_L31N_7	M7	I/O
7	IO_L31P_7	IO_L31P_7	IO_L31P_7	IO_L31P_7	IO_L31P_7	M8	I/O
7	IO_L32N_7	IO_L32N_7	IO_L32N_7	IO_L32N_7	IO_L32N_7	M6	I/O
7	IO_L32P_7	IO_L32P_7	IO_L32P_7	IO_L32P_7	IO_L32P_7	M5	I/O
7	IO_L33N_7	IO_L33N_7	IO_L33N_7	IO_L33N_7	IO_L33N_7	M3	I/O
7	IO_L33P_7	IO_L33P_7	IO_L33P_7	IO_L33P_7	IO_L33P_7	L4	I/O
7	IO_L34N_7	IO_L34N_7	IO_L34N_7	IO_L34N_7	IO_L34N_7	M1	I/O
7	IO_L34P_7	IO_L34P_7	IO_L34P_7	IO_L34P_7	IO_L34P_7	M2	I/O
7	IO_L35N_7	IO_L35N_7	IO_L35N_7	IO_L35N_7	IO_L35N_7	N7	I/O
7	IO_L35P_7	IO_L35P_7	IO_L35P_7	IO_L35P_7	IO_L35P_7	N8	I/O
7	IO_L38N_7	IO_L38N_7	IO_L38N_7	IO_L38N_7	IO_L38N_7	N5	I/O
7	IO_L38P_7	IO_L38P_7	IO_L38P_7	IO_L38P_7	IO_L38P_7	N6	I/O
7	IO_L39N_7	IO_L39N_7	IO_L39N_7	IO_L39N_7	IO_L39N_7	N3	I/O
7	IO_L39P_7	IO_L39P_7	IO_L39P_7	IO_L39P_7	IO_L39P_7	N4	I/O
7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	N1	VREF
7	IO_L40P_7	IO_L40P_7	IO_L40P_7	IO_L40P_7	IO_L40P_7	N2	I/O
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	G3	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	J8	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	K8	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	L3	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	L9	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	M9	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	N9	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	N10	VCCO
N/A	GND	GND	GND	GND	GND	A1	GND
N/A	GND	GND	GND	GND	GND	A26	GND
N/A	GND	GND	GND	GND	GND	AC4	GND
N/A	GND	GND	GND	GND	GND	AC12	GND
N/A	GND	GND	GND	GND	GND	AC15	GND
N/A	GND	GND	GND	GND	GND	AC23	GND
N/A	GND	GND	GND	GND	GND	AD3	GND
N/A	GND	GND	GND	GND	GND	AD24	GND
N/A	GND	GND	GND	GND	GND	AE2	GND
N/A	GND	GND	GND	GND	GND	AE25	GND
N/A	GND	GND	GND	GND	GND	AF1	GND
N/A	GND	GND	GND	GND	GND	AF26	GND
N/A	GND	GND	GND	GND	GND	B2	GND
N/A	GND	GND	GND	GND	GND	B25	GND
N/A	GND	GND	GND	GND	GND	C3	GND
N/A	GND	GND	GND	GND	GND	C24	GND
N/A	GND	GND	GND	GND	GND	D4	GND
N/A	GND	GND	GND	GND	GND	D12	GND

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
4	IO_L11P_4	IO_L11P_4	AE21	I/O
4	IO_L12N_4	IO_L12N_4	AH21	I/O
4	IO_L12P_4	IO_L12P_4	AJ21	I/O
4	IO_L13N_4	IO_L13N_4	AB21	I/O
4	IO_L13P_4	IO_L13P_4	AA20	I/O
4	IO_L14N_4	IO_L14N_4	AC20	I/O
4	IO_L14P_4	IO_L14P_4	AD20	I/O
4	IO_L15N_4	IO_L15N_4	AE20	I/O
4	IO_L15P_4	IO_L15P_4	AF20	I/O
4	IO_L16N_4	IO_L16N_4	AG20	I/O
4	IO_L16P_4	IO_L16P_4	AH20	I/O
4	IO_L17N_4	IO_L17N_4	AJ20	I/O
4	IO_L17P_4	IO_L17P_4	AK20	I/O
4	IO_L18N_4	IO_L18N_4	AA19	I/O
4	IO_L18P_4	IO_L18P_4	AB19	I/O
4	IO_L19N_4	IO_L19N_4	AC19	I/O
4	IO_L19P_4	IO_L19P_4	AD19	I/O
4	IO_L20N_4	IO_L20N_4	AE19	I/O
4	IO_L20P_4	IO_L20P_4	AF19	I/O
4	IO_L21N_4	IO_L21N_4	AG19	I/O
4	IO_L21P_4	IO_L21P_4	AH19	I/O
4	IO_L22N_4/VREF_4	IO_L22N_4/VREF_4	AJ19	VREF
4	IO_L22P_4	IO_L22P_4	AK19	I/O
4	IO_L23N_4	IO_L23N_4	AB18	I/O
4	IO_L23P_4	IO_L23P_4	AC18	I/O
4	IO_L24N_4	IO_L24N_4	AE18	I/O
4	IO_L24P_4	IO_L24P_4	AF18	I/O
4	IO_L25N_4	IO_L25N_4	AJ18	I/O
4	IO_L25P_4	IO_L25P_4	AK18	I/O
4	IO_L26N_4	IO_L26N_4	AA17	I/O
4	IO_L26P_4/VREF_4	IO_L26P_4/VREF_4	AB17	VREF
4	IO_L27N_4/DIN/D0	IO_L27N_4/DIN/D0	AD17	DUAL
4	IO_L27P_4/D1	IO_L27P_4/D1	AE17	DUAL
4	IO_L28N_4	IO_L28N_4	AH17	I/O
4	IO_L28P_4	IO_L28P_4	AJ17	I/O
4	IO_L29N_4	IO_L29N_4	AB16	I/O
4	IO_L29P_4	IO_L29P_4	AC16	I/O
4	IO_L30N_4/D2	IO_L30N_4/D2	AD16	DUAL
4	IO_L30P_4/D3	IO_L30P_4/D3	AE16	DUAL
4	IO_L31N_4/INIT_B	IO_L31N_4/INIT_B	AG16	DUAL

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	C1	DCI
7	IO_L01P_7/VRN_7	IO_L01P_7/VRN_7	C2	DCI
7	IO_L02N_7	IO_L02N_7	D3	I/O
7	IO_L02P_7	IO_L02P_7	D4	I/O
7	IO_L03N_7/VREF_7	IO_L03N_7/VREF_7	D1	VREF
7	IO_L03P_7	IO_L03P_7	D2	I/O
7	IO_L04N_7	IO_L04N_7	E1	I/O
7	IO_L04P_7	IO_L04P_7	E2	I/O
7	IO_L05N_7	IO_L05N_7	F5	I/O
7	IO_L05P_7	IO_L05P_7	E4	I/O
7	IO_L06N_7	IO_L06N_7	F2	I/O
7	IO_L06P_7	IO_L06P_7	F3	I/O
7	IO_L07N_7	IO_L07N_7	G3	I/O
7	IO_L07P_7	IO_L07P_7	G4	I/O
7	IO_L08N_7	IO_L08N_7	G1	I/O
7	IO_L08P_7	IO_L08P_7	G2	I/O
7	IO_L09N_7	IO_L09N_7	H7	I/O
7	IO_L09P_7	IO_L09P_7	G6	I/O
7	IO_L10N_7	IO_L10N_7	H5	I/O
7	IO_L10P_7/VREF_7	IO_L10P_7/VREF_7	H6	VREF
7	IO_L11N_7	IO_L11N_7	H3	I/O
7	IO_L11P_7	IO_L11P_7	H4	I/O
7	IO_L13N_7	IO_L13N_7	H1	I/O
7	IO_L13P_7	IO_L13P_7	H2	I/O
7	IO_L14N_7	IO_L14N_7	J4	I/O
7	IO_L14P_7	IO_L14P_7	J5	I/O
7	IO_L15N_7	IO_L15N_7	J1	I/O
7	IO_L15P_7	IO_L15P_7	J2	I/O
7	IO_L16N_7	IO_L16N_7	K9	I/O
7	IO_L16P_7/VREF_7	IO_L16P_7/VREF_7	J8	VREF
7	IO_L17N_7	IO_L17N_7	K6	I/O
7	IO_L17P_7	IO_L17P_7	K7	I/O
7	IO_L19N_7/VREF_7	IO_L19N_7/VREF_7	K2	VREF
7	IO_L19P_7	IO_L19P_7	K3	I/O
7	IO_L20N_7	IO_L20N_7	L10	I/O
7	IO_L20P_7	IO_L20P_7	K10	I/O
7	IO_L21N_7	IO_L21N_7	L7	I/O
7	IO_L21P_7	IO_L21P_7	L8	I/O
7	IO_L22N_7	IO_L22N_7	L5	I/O
7	IO_L22P_7	IO_L22P_7	L6	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
7	IO_L23N_7	IO_L23N_7	L3	I/O
7	IO_L23P_7	IO_L23P_7	L4	I/O
7	IO_L24N_7	IO_L24N_7	L1	I/O
7	IO_L24P_7	IO_L24P_7	L2	I/O
7	N.C. (◆)	IO_L25N_7	M6	I/O
7	N.C. (◆)	IO_L25P_7	M7	I/O
7	IO_L26N_7	IO_L26N_7	M3	I/O
7	IO_L26P_7	IO_L26P_7	M4	I/O
7	IO_L27N_7	IO_L27N_7	M1	I/O
7	IO_L27P_7/VREF_7	IO_L27P_7/VREF_7	M2	VREF
7	IO_L28N_7	IO_L28N_7	N10	I/O
7	IO_L28P_7	IO_L28P_7	M10	I/O
7	IO_L29N_7	IO_L29N_7	N8	I/O
7	IO_L29P_7	IO_L29P_7	N9	I/O
7	IO_L31N_7	IO_L31N_7	N1	I/O
7	IO_L31P_7	IO_L31P_7	N2	I/O
7	IO_L32N_7	IO_L32N_7	P9	I/O
7	IO_L32P_7	IO_L32P_7	P10	I/O
7	IO_L33N_7	IO_L33N_7	P6	I/O
7	IO_L33P_7	IO_L33P_7	P7	I/O
7	IO_L34N_7	IO_L34N_7	P2	I/O
7	IO_L34P_7	IO_L34P_7	P3	I/O
7	IO_L35N_7	IO_L35N_7	R9	I/O
7	IO_L35P_7	IO_L35P_7	R10	I/O
7	IO_L37N_7	IO_L37N_7	R7	I/O
7	IO_L37P_7/VREF_7	IO_L37P_7/VREF_7	R8	VREF
7	IO_L38N_7	IO_L38N_7	R5	I/O
7	IO_L38P_7	IO_L38P_7	R6	I/O
7	IO_L39N_7	IO_L39N_7	R3	I/O
7	IO_L39P_7	IO_L39P_7	R4	I/O
7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	R1	VREF
7	IO_L40P_7	IO_L40P_7	R2	I/O
7	N.C. (◆)	IO_L46N_7	M8	I/O
7	N.C. (◆)	IO_L46P_7	M9	I/O
7	N.C. (◆)	IO_L49N_7	N6	I/O
7	N.C. (◆)	IO_L49P_7	M5	I/O
7	N.C. (◆)	IO_L50N_7	N4	I/O
7	N.C. (◆)	IO_L50P_7	N5	I/O
7	VCCO_7	VCCO_7	E3	VCCO
7	VCCO_7	VCCO_7	J3	VCCO

User I/Os by Bank

Table 108 indicates how the available user-I/O pins are distributed between the eight I/O banks for the XC3S2000 in the FG900 package. Similarly, Table 109 shows how the available user-I/O pins are distributed between the eight I/O banks for the XC3S4000 and XC3S5000 in the FG900 package.

Table 108: **User I/Os Per Bank for XC3S2000 in FG900 Package**

Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	71	62	0	2	5	2
	1	71	62	0	2	5	2
Right	2	69	61	0	2	6	0
	3	71	62	0	2	7	0
Bottom	4	72	57	6	2	5	2
	5	71	55	6	2	6	2
Left	6	69	60	0	2	7	0
	7	71	62	0	2	7	0

Table 109: **User I/Os Per Bank for XC3S4000 and XC3S5000 in FG900 Package**

Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	79	70	0	2	5	2
	1	79	70	0	2	5	2
Right	2	79	71	0	2	6	0
	3	79	70	0	2	7	0
Bottom	4	80	65	6	2	5	2
	5	79	63	6	2	6	2
Left	6	79	70	0	2	7	0
	7	79	70	0	2	7	0

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
0	VCCO_0	VCCO_0	F13	VCCO
0	VCCO_0	VCCO_0	G8	VCCO
0	VCCO_0	VCCO_0	H11	VCCO
0	VCCO_0	VCCO_0	H15	VCCO
0	VCCO_0	VCCO_0	M13	VCCO
0	VCCO_0	VCCO_0	M14	VCCO
0	VCCO_0	VCCO_0	M15	VCCO
0	VCCO_0	VCCO_0	M16	VCCO
1	IO	IO	B26	I/O
1	IO	IO	A18	I/O
1	IO	IO	C23	I/O
1	IO	IO	E21	I/O
1	IO	IO	E25	I/O
1	IO	IO	F18	I/O
1	IO	IO	F27	I/O
1	IO	IO	F29	I/O
1	IO	IO	H23	I/O
1	IO	IO	H26	I/O
1	N.C. (◆)	IO	J26	I/O
1	IO	IO	K19	I/O
1	IO	IO	L19	I/O
1	IO	IO	L20	I/O
1	IO	IO	L21	I/O
1	N.C. (◆)	IO	L23	I/O
1	IO	IO	L24	I/O
1	IO/VREF_1	IO/VREF_1	D30	VREF
1	IO/VREF_1	IO/VREF_1	K21	VREF
1	IO/VREF_1	IO/VREF_1	L18	VREF
1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	A32	DCI
1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	B32	DCI
1	IO_L02N_1	IO_L02N_1	A31	I/O
1	IO_L02P_1	IO_L02P_1	B31	I/O
1	IO_L03N_1	IO_L03N_1	B30	I/O
1	IO_L03P_1	IO_L03P_1	C30	I/O
1	IO_L04N_1	IO_L04N_1	C29	I/O
1	IO_L04P_1	IO_L04P_1	D29	I/O
1	IO_L05N_1	IO_L05N_1	A29	I/O
1	IO_L05P_1	IO_L05P_1	B29	I/O
1	IO_L06N_1/VREF_1	IO_L06N_1/VREF_1	E28	VREF
1	IO_L06P_1	IO_L06P_1	F28	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
1	VCCO_1	VCCO_1	M22	VCCO
2	IO	IO	G33	I/O
2	IO	IO	G34	I/O
2	IO	IO	U25	I/O
2	IO	IO	U26	I/O
2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	C33	DCI
2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	C34	DCI
2	IO_L02N_2	IO_L02N_2	D33	I/O
2	IO_L02P_2	IO_L02P_2	D34	I/O
2	IO_L03N_2/VREF_2	IO_L03N_2/VREF_2	E32	VREF
2	IO_L03P_2	IO_L03P_2	E33	I/O
2	IO_L04N_2	IO_L04N_2	F31	I/O
2	IO_L04P_2	IO_L04P_2	F32	I/O
2	IO_L05N_2	IO_L05N_2	G29	I/O
2	IO_L05P_2	IO_L05P_2	G30	I/O
2	IO_L06N_2	IO_L06N_2	H29	I/O
2	IO_L06P_2	IO_L06P_2	H30	I/O
2	IO_L07N_2	IO_L07N_2	H33	I/O
2	IO_L07P_2	IO_L07P_2	H34	I/O
2	IO_L08N_2	IO_L08N_2	J28	I/O
2	IO_L08P_2	IO_L08P_2	J29	I/O
2	IO_L09N_2/VREF_2	IO_L09N_2/VREF_2	H31	VREF
2	IO_L09P_2	IO_L09P_2	J31	I/O
2	IO_L10N_2	IO_L10N_2	J32	I/O
2	IO_L10P_2	IO_L10P_2	J33	I/O
2	IO_L11N_2	IO_L11N_2	J27	I/O
2	IO_L11P_2	IO_L11P_2	K26	I/O
2	IO_L12N_2	IO_L12N_2	K27	I/O
2	IO_L12P_2	IO_L12P_2	K28	I/O
2	IO_L13N_2	IO_L13N_2	K29	I/O
2	IO_L13P_2/VREF_2	IO_L13P_2/VREF_2	K30	VREF
2	IO_L14N_2	IO_L14N_2	K31	I/O
2	IO_L14P_2	IO_L14P_2	K32	I/O
2	IO_L15N_2	IO_L15N_2	K33	I/O
2	IO_L15P_2	IO_L15P_2	K34	I/O
2	IO_L16N_2	IO_L16N_2	L25	I/O
2	IO_L16P_2	IO_L16P_2	L26	I/O
2	N.C. (◆)	IO_L17N_2	L28	I/O
2	N.C. (◆)	IO_L17P_2/ VREF_2	L29	VREF

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
4	VCCO_4	VCCO_4	AC19	VCCO
4	VCCO_4	VCCO_4	AC20	VCCO
4	VCCO_4	VCCO_4	AC21	VCCO
4	VCCO_4	VCCO_4	AC22	VCCO
4	VCCO_4	VCCO_4	AG20	VCCO
4	VCCO_4	VCCO_4	AG24	VCCO
4	VCCO_4	VCCO_4	AH27	VCCO
4	VCCO_4	VCCO_4	AJ22	VCCO
4	VCCO_4	VCCO_4	AL19	VCCO
4	VCCO_4	VCCO_4	AL24	VCCO
4	VCCO_4	VCCO_4	AM27	VCCO
4	VCCO_4	VCCO_4	AM31	VCCO
4	VCCO_4	VCCO_4	AN22	VCCO
5	IO	IO	AD11	I/O
5	N.C. (◆)	IO	AD12	I/O
5	IO	IO	AD14	I/O
5	IO	IO	AD15	I/O
5	IO	IO	AD16	I/O
5	IO	IO	AD17	I/O
5	IO	IO	AE14	I/O
5	IO	IO	AE16	I/O
5	N.C. (◆)	IO	AF9	I/O
5	IO	IO	AG9	I/O
5	IO	IO	AG12	I/O
5	IO	IO	AJ6	I/O
5	IO	IO	AJ17	I/O
5	IO	IO	AK10	I/O
5	IO	IO	AK14	I/O
5	IO	IO	AM12	I/O
5	IO	IO	AN9	I/O
5	IO/VREF_5	IO/VREF_5	AJ8	VREF
5	IO/VREF_5	IO/VREF_5	AL5	VREF
5	IO/VREF_5	IO/VREF_5	AP17	VREF
5	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	AP3	DUAL
5	IO_L01P_5/CS_B	IO_L01P_5/CS_B	AN3	DUAL
5	IO_L02N_5	IO_L02N_5	AP4	I/O
5	IO_L02P_5	IO_L02P_5	AN4	I/O
5	IO_L03N_5	IO_L03N_5	AN5	I/O
5	IO_L03P_5	IO_L03P_5	AM5	I/O
5	IO_L04N_5	IO_L04N_5	AM6	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
5	IO_L04P_5	IO_L04P_5	AL6	I/O
5	IO_L05N_5	IO_L05N_5	AP6	I/O
5	IO_L05P_5	IO_L05P_5	AN6	I/O
5	IO_L06N_5	IO_L06N_5	AK7	I/O
5	IO_L06P_5	IO_L06P_5	AJ7	I/O
5	IO_L07N_5	IO_L07N_5	AG10	I/O
5	IO_L07P_5	IO_L07P_5	AF10	I/O
5	IO_L08N_5	IO_L08N_5	AJ10	I/O
5	IO_L08P_5	IO_L08P_5	AH10	I/O
5	IO_L09N_5	IO_L09N_5	AM10	I/O
5	IO_L09P_5	IO_L09P_5	AL10	I/O
5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	AP10	DCI
5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	AN10	DCI
5	IO_L11N_5/VREF_5	IO_L11N_5/VREF_5	AP11	VREF
5	IO_L11P_5	IO_L11P_5	AN11	I/O
5	IO_L12N_5	IO_L12N_5	AF12	I/O
5	IO_L12P_5	IO_L12P_5	AE12	I/O
5	IO_L13N_5	IO_L13N_5	AJ12	I/O
5	IO_L13P_5	IO_L13P_5	AH12	I/O
5	IO_L14N_5	IO_L14N_5	AL12	I/O
5	IO_L14P_5	IO_L14P_5	AK12	I/O
5	IO_L15N_5	IO_L15N_5	AP12	I/O
5	IO_L15P_5	IO_L15P_5	AN12	I/O
5	IO_L16N_5	IO_L16N_5	AE13	I/O
5	IO_L16P_5	IO_L16P_5	AD13	I/O
5	IO_L17N_5	IO_L17N_5	AH13	I/O
5	IO_L17P_5	IO_L17P_5	AG13	I/O
5	IO_L18N_5	IO_L18N_5	AM13	I/O
5	IO_L18P_5	IO_L18P_5	AL13	I/O
5	IO_L19N_5	IO_L19N_5	AG14	I/O
5	IO_L19P_5/VREF_5	IO_L19P_5/VREF_5	AF14	VREF
5	IO_L20N_5	IO_L20N_5	AJ14	I/O
5	IO_L20P_5	IO_L20P_5	AH14	I/O
5	IO_L21N_5	IO_L21N_5	AM14	I/O
5	IO_L21P_5	IO_L21P_5	AL14	I/O
5	IO_L22N_5	IO_L22N_5	AP14	I/O
5	IO_L22P_5	IO_L22P_5	AN14	I/O
5	IO_L23N_5	IO_L23N_5	AF15	I/O
5	IO_L23P_5	IO_L23P_5	AE15	I/O
5	IO_L24N_5	IO_L24N_5	AJ15	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
N/A	VCCAUX	VCCAUX	Y5	VCCAUX
N/A	VCCINT	VCCINT	AA13	VCCINT
N/A	VCCINT	VCCINT	AA22	VCCINT
N/A	VCCINT	VCCINT	AB13	VCCINT
N/A	VCCINT	VCCINT	AB14	VCCINT
N/A	VCCINT	VCCINT	AB15	VCCINT
N/A	VCCINT	VCCINT	AB16	VCCINT
N/A	VCCINT	VCCINT	AB19	VCCINT
N/A	VCCINT	VCCINT	AB20	VCCINT
N/A	VCCINT	VCCINT	AB21	VCCINT
N/A	VCCINT	VCCINT	AB22	VCCINT
N/A	VCCINT	VCCINT	AC12	VCCINT
N/A	VCCINT	VCCINT	AC17	VCCINT
N/A	VCCINT	VCCINT	AC18	VCCINT
N/A	VCCINT	VCCINT	AC23	VCCINT
N/A	VCCINT	VCCINT	M12	VCCINT
N/A	VCCINT	VCCINT	M17	VCCINT
N/A	VCCINT	VCCINT	M18	VCCINT
N/A	VCCINT	VCCINT	M23	VCCINT
N/A	VCCINT	VCCINT	N13	VCCINT
N/A	VCCINT	VCCINT	N14	VCCINT
N/A	VCCINT	VCCINT	N15	VCCINT
N/A	VCCINT	VCCINT	N16	VCCINT
N/A	VCCINT	VCCINT	N19	VCCINT
N/A	VCCINT	VCCINT	N20	VCCINT
N/A	VCCINT	VCCINT	N21	VCCINT
N/A	VCCINT	VCCINT	N22	VCCINT
N/A	VCCINT	VCCINT	P13	VCCINT
N/A	VCCINT	VCCINT	P22	VCCINT
N/A	VCCINT	VCCINT	R13	VCCINT
N/A	VCCINT	VCCINT	R22	VCCINT
N/A	VCCINT	VCCINT	T13	VCCINT
N/A	VCCINT	VCCINT	T22	VCCINT
N/A	VCCINT	VCCINT	U12	VCCINT
N/A	VCCINT	VCCINT	U23	VCCINT
N/A	VCCINT	VCCINT	V12	VCCINT
N/A	VCCINT	VCCINT	V23	VCCINT
N/A	VCCINT	VCCINT	W13	VCCINT
N/A	VCCINT	VCCINT	W22	VCCINT
N/A	VCCINT	VCCINT	Y13	VCCINT

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
V	I/O L40P_6 VREF_6	I/O L40N_6	I/O L39P_6	I/O L39N_6	I/O L38P_6	I/O L38N_6	I/O L52P_6	I/O L52N_6	I/O	I/O	I/O L49P_6 ◆	VCCINT	GND	GND	GND	GND	GND
W	GND	I/O L37P_6	I/O L37N_6	VCCO_6	GND	I/O L36P_6	I/O L36N_6	VCCAUX	GND	I/O L35P_6	I/O L49N_6 ◆	VCCO_6	VCCINT	GND	GND	GND	GND
Y	I/O L34P_6	I/O L34N_6 VREF_6	I/O L33P_6	I/O L33N_6	VCCAUX	I/O L48P_6	I/O L48N_6	VCCO_6	I/O L35N_6	I/O L32P_6	I/O L32N_6	VCCO_6	VCCINT	GND	GND	GND	GND
AA	I/O L31P_6	I/O L31N_6	I/O L30P_6	I/O L30N_6	I/O L29P_6	I/O L29N_6	I/O L28P_6	I/O L28N_6	I/O L46P_6 ◆	I/O L46N_6 ◆	I/O L27P_6	VCCO_6	VCCINT	GND	GND	GND	GND
AB	GND	VCCO_6	I/O L26P_6	I/O L26N_6	GND	VCCO_6	I/O L25P_6	I/O L25N_6	GND	I/O L24P_6	I/O L27N_6	VCCO_6	VCCINT	VCCINT	VCCINT	VCCINT	GND
AC	I/O L23P_6	I/O L23N_6	I/O L45P_6	I/O L45N_6	I/O L22P_6	I/O L22N_6	I/O L21P_6	I/O L21N_6	I/O L24N_6 VREF_6	I/O L20P_6	I/O L20N_6	VCCINT	VCCO_5	VCCO_5	VCCO_5	VCCO_5	VCCINT
AD	I/O L19P_6	I/O L19N_6	GND	VCCO_6	VCCAUX	I/O L44P_6 ◆	I/O L44N_6 ◆	VCCO_6	I/O L17P_6 VREF_6	I/O L17N_6	I/O	I/O ◆	I/O L16P_5	I/O	I/O	I/O	I/O
AE	I/O L16P_6	I/O L16N_6	I/O L15P_6	I/O L15N_6	I/O L14P_6	I/O L14N_6	I/O L13P_6 VREF_6	I/O L13N_6	I/O L12P_6	GND	I/O L39P_5 ◆	I/O L12P_5	I/O L16N_5	I/O	I/O L23P_5	I/O	I/O L29P_5 VREF_5
AF	GND	I/O L11P_6	I/O L11N_6	I/O L10P_6	GND	I/O L09P_6	I/O L09N_6 VREF_6	I/O L12N_6	I/O ◆	I/O L07P_5	I/O L39N_5 ◆	I/O L12N_5	GND	I/O L19P_5 VREF_5	I/O L23N_5	GND	I/O L29N_5
AG	I/O L08P_6	I/O L08N_6	VCCO_6	I/O L10N_6	I/O L07P_6	I/O L07N_6	VCCO_6	M2	I/O	I/O L07N_5	VCCO_5	I/O	I/O L17P_5	I/O L19N_5	VCCO_5	VCCAUX	I/O L30P_5
AH	I/O	I/O	I/O L41P_6 ◆	I/O L41N_6 ◆	I/O L06P_6	I/O L06N_6	GND	VCCO_5	I/O L37P_5	I/O L08P_5	I/O L40P_5 ◆	I/O L13P_5	I/O L17N_5	I/O L20P_5	I/O L24P_5	I/O L27P_5	I/O L30N_5
AJ	I/O L05P_6	I/O L05N_6	I/O L04P_6	I/O L04N_6	VCCAUX	I/O	I/O L06P_5	IO VREF_5	I/O L37N_5	I/O L08N_5	I/O L40N_5 ◆	I/O L13N_5	VCCO_5	I/O L20N_5	I/O L24N_5	I/O L27N_5 VREF_5	I/O
AK	GND	I/O L03P_6	I/O L03N_6 VREF_6	M1	GND	VCCAUX	I/O L06N_5	I/O L35P_5	GND	I/O	VCCAUX	I/O L14P_5	GND	I/O	VCCAUX	GND	I/O L31P_5 D5
AL	I/O L02P_6	I/O L02N_6	VCCO_6	M0	IO VREF_5	I/O L04P_5	I/O L33P_5 ◆	I/O L35N_5	I/O L38P_5	I/O L09P_5	VCCO_5	I/O L14N_5	I/O L18P_5	I/O L21P_5	I/O L25P_5	VCCO_5	I/O L31N_5 D4
AM	I/O L01P_6 VRN_6	I/O L01N_6 VRP_6	GND	VCCO_5	I/O L03P_5	I/O L04N_5	I/O L33N_5 ◆	VCCO_5	I/O L38N_5	I/O L09N_5	GND	I/O	I/O L18N_5	I/O L21N_5	I/O L25N_5	I/O L28P_5 D7	I/O L32P_5 GCLK2
AN	GND	GND	I/O L01P_5 CS_B	I/O L02P_5	I/O L03N_5	I/O L05P_5	I/O L34P_5 ◆	I/O L36P_5	I/O	I/O L10P_5 VRN_5	I/O L11P_5	I/O L15P_5	VCCO_5	I/O L22P_5	I/O L26P_5	I/O L28N_5 D6	I/O L32N_5 GCLK3
AP	GND	GND	I/O L01N_5 RDWR_B	I/O L02N_5	GND	I/O L05N_5	I/O L34N_5 ◆	I/O L36N_5	GND	I/O L10N_5 VRP_5	I/O L11N_5 VREF_5	I/O L15N_5	GND	I/O L22N_5	I/O L26N_5	GND	IO VREF_5

Bank 6

Bank 5

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Bottom Left Corner of FG1156 Package (Top View)

Figure 59: FG1156 Package Footprint (Top View) Continued