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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	8320
Number of Logic Elements/Cells	74880
Total RAM Bits	1916928
Number of I/O	633
Number of Gates	500000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	900-BBGA
Supplier Device Package	900-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s5000-4fgg900c

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Table 8: Single-Ended I/O Standards

Signal Standard	V _{cco}	(Volts)	V _{REF} for Inputs	Board Termination
(IOSTANDARD)	For Outputs	For Inputs	(Volts) ⁽¹⁾	Voltage (V _{TT}) in Volts
GTL	Note 2	Note 2	0.8	1.2
GTLP	Note 2	Note 2	1	1.5
HSTL_I	1.5	-	0.75	0.75
HSTL_III	1.5	-	0.9	1.5
HSTL_I_18	1.8	-	0.9	0.9
HSTL_II_18	1.8	-	0.9	0.9
HSTL_III_18	1.8	-	1.1	1.8
LVCMOS12	1.2	1.2	-	-
LVCMOS15	1.5	1.5	-	-
LVCMOS18	1.8	1.8	-	-
LVCMOS25	2.5	2.5	-	-
LVCMOS33	3.3	3.3	-	-
LVTTL	3.3	3.3	-	-
PCI33_3	3.0	3.0	-	-
SSTL18_I	1.8	-	0.9	0.9
SSTL18_II	1.8	-	0.9	0.9
SSTL2_I	2.5	-	1.25	1.25
SSTL2_II	2.5	-	1.25	1.25

Notes:

1. Banks 4 and 5 of any Spartan-3 device in a VQ100 package do not support signal standards using V_{REF}

2. The V_{CCO} level used for the GTL and GTLP standards must be no lower than the termination voltage (V_{TT}), nor can it be lower than the voltage at the I/O pad.

3. See Table 10 for a listing of the single-ended DCI standards.

Differential standards employ a pair of signals, one the opposite polarity of the other. The noise canceling (e.g., Common-Mode Rejection) properties of these standards permit exceptionally high data transfer rates. This section introduces the differential signaling capabilities of Spartan-3 devices.

Each device-package combination designates specific I/O pairs that are specially optimized to support differential standards. A unique "L-number", part of the pin name, identifies the line-pairs associated with each bank (see Figure 40, page 112). For each pair, the letters 'P' and 'N' designate the true and inverted lines, respectively. For example, the pin names IO_L43P_7 and IO_L43N_7 indicate the true and inverted lines comprising the line pair L43 on Bank 7. The V_{CCO} lines provide current to the outputs. The V_{CCAUX} lines supply power to the differential inputs, making them independent of the V_{CCO} voltage for an I/O bank. The V_{REF} lines are not used. Select the V_{CCO} level to suit the desired differential standard according to Table 9.

The product of w and n yields the total block RAM capacity. Equation 1 and Equation 2 show that as the data bus width increases, the number of address lines along with the number of addressable memory locations decreases. Using the permissible DI/DO bus widths as inputs to these equations provides the bus width and memory capacity measures shown in Table 14.

DI/DO Bus Width (w – p Bits)	DIP/DOP Bus Width (p Bits)	Total Data Path Width (w Bits)	ADDR Bus Width (r Bits)	No. of Addressable Locations (n)	Block RAM Capacity (Bits)
1	0	1	14	16,384	16,384
2	0	2	13	8,192	16,384
4	0	4	12	4,096	16,384
8	1	9	11	2,048	18,432
16	2	18	10	1,024	18,432
32	4	36	9	512	18,432

Table 14: Port Aspect Ratios for Port A or B

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Block RAM Data Operations

Writing data to and accessing data from the block RAM are synchronous operations that take place independently on each of the two ports.

The waveforms for the write operation are shown in the top half of the Figure 15, Figure 16, and Figure 17. When the WE and EN signals enable the active edge of CLK, data at the DI input bus is written to the block RAM location addressed by the ADDR lines.

There are a number of different conditions under which data can be accessed at the DO outputs. Basic data access always occurs when the WE input is inactive. Under this condition, data stored in the memory location addressed by the ADDR lines passes through a transparent output latch to the DO outputs. The timing for basic data access is shown in the portions of Figure 15, Figure 16, and Figure 17 during which WE is Low.



Figure 15: Waveforms of Block RAM Data Operations with WRITE_FIRST Selected

Data can also be accessed on the DO outputs when asserting the WE input. This is accomplished using two different attributes:

Choosing the WRITE_FIRST attribute, data is written to the addressed memory location on an enabled active CLK edge and is also passed to the DO outputs. WRITE_FIRST timing is shown in the portion of Figure 15 during which WE is High.

Choosing the READ_FIRST attribute, data already stored in the addressed location pass to the DO outputs before that location is overwritten with new data from the DI inputs on an enabled active CLK edge. READ_FIRST timing is shown in the portion of Figure 16 during which WE is High.



Notes:

1. In the Low Frequency mode, all seven DLL outputs are available. In the High Frequency mode, only the CLK0, CLK180, and CLKDV outputs are available.

Figure 21: Input Clock, Output Clock, and Feedback Connections for the DLL

In the on-chip synchronization case (the [a] and [b] sections of Figure 21), it is possible to connect any of the DLL's seven output clock signals through general routing resources to the FPGA's internal registers. Either a Global Clock Buffer (BUFG) or a BUFGMUX affords access to the global clock network. As shown in the [a] section of Figure 21, the feedback loop is created by routing CLK0 (or CLK2X, in the [b] section) to a global clock net, which in turn drives the CLKFB input.

In the off-chip synchronization case (the [c] and [d] sections of Figure 21), CLK0 (or CLK2X) plus any of the DLL's other output clock signals exit the FPGA using output buffers (OBUF) to drive an external clock network plus registers on the board. As shown in the [c] section of Figure 21, the feedback loop is formed by feeding CLK0 (or CLK2X, in the [d] section) back into the FPGA using an IBUFG, which directly accesses the global clock network, or an IBUF. Then, the global clock net is connected directly to the CLKFB input.

DLL Frequency Modes

The DLL supports two distinct operating modes, High Frequency and Low Frequency, with each specified over a different clock frequency range. The DLL_FREQUENCY_MODE attribute chooses between the two modes. When the attribute is set to LOW, the Low Frequency mode permits all seven DLL clock outputs to operate over a low-to-moderate frequency range. When the attribute is set to HIGH, the High Frequency mode allows the CLK0, CLK180 and CLKDV outputs to operate at the highest possible frequencies. The remaining DLL clock outputs are not available for use in High Frequency mode.

Accommodating High Input Frequencies

If the frequency of the CLKIN signal is high such that it exceeds the maximum permitted, divide it down to an acceptable value using the CLKIN_DIVIDE_BY_2 attribute. When this attribute is set to TRUE, the CLKIN frequency is divided by a factor of two just as it enters the DCM.



Notes:

- There are two ways to use the DONE line. First, one may set the BitGen option DriveDone to "Yes" only for the last FPGA to be configured in the chain shown above (or for the single FPGA as may be the case). This enables the DONE pin to drive High; thus, no pull-up resistor is necessary. DriveDone is set to "No" for the remaining FPGAs in the chain. Second, DriveDone can be set to "No" for all FPGAs. Then all DONE lines are open-drain and require the pull-up resistor shown in grey. In most cases, a value between 3.3KΩ to 4.7KΩ is sufficient. However, when using DONE synchronously with a long chain of FPGAs, cumulative capacitance may necessitate lower resistor values (e.g. down to 330Ω) in order to ensure a rise time within one clock cycle.
- 2. For information on how to program the FPGA using 3.3V signals and power, see 3.3V-Tolerant Configuration Interface.

Figure 26: Connection Diagram for Master and Slave Serial Configuration

Slave Serial mode is selected by applying <111> to the mode pins (M0, M1, and M2). A pull-up on the mode pins makes slave serial the default mode if the pins are left unconnected.

Master Serial Mode

In Master Serial mode, the FPGA drives CCLK pin, which behaves as a bidirectional I/O pin. The FPGA in the center of Figure 26 is set for Master Serial mode and connects to the serial configuration PROM and to the CCLK inputs of any slave FPGAs in a configuration daisy-chain. The master FPGA drives the configuration clock on the CCLK pin to the Xilinx Serial PROM, which, in response, provides bit-serial data to the FPGA's DIN input. The FPGA accepts this data on each rising CCLK edge. After the master FPGA finishes configuring, it passes data on its DOUT pin to the next FPGA device in a daisy-chain. The DOUT data appears after the falling CCLK clock edge.

The Master Serial mode interface is identical to Slave Serial except that an internal oscillator generates the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK, which always starts at a default frequency of 6 MHz. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration.

Slave Parallel Mode (SelectMAP)

The Parallel or SelectMAP modes support the fastest configuration. Byte-wide data is written into the FPGA with a BUSY flag controlling the flow of data. An external source provides 8-bit-wide data, CCLK, an active-Low Chip Select (CS_B) signal and an active-Low Write signal (RDWR_B). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low. Data can also be read using the Slave Parallel mode. If RDWR_B is asserted, configuration data is read out of the FPGA as part of a readback operation.

After configuration, it is possible to use any of the Multipurpose pins (DIN/D0-D7, DOUT/BUSY, INIT_B, CS_B, and RDWR_B) as User I/Os. To do this, simply set the BitGen option *Persist* to *No* and assign the desired signals to multipurpose configuration pins using the Xilinx development software. Alternatively, it is possible to continue using the configuration port

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Additional Configuration Details

Additional details about the Spartan-3 FPGA configuration architecture and command set are available in <u>UG332</u>: *Spartan-3 Generation Configuration User Guide* and in application note <u>XAPP452</u>: *Spartan-3 Advanced Configuration Architecture*.

Powering Spartan-3 FPGAs

Voltage Regulators

Various power supply manufacturers offer complete power solutions for Xilinx FPGAs, including some with integrated multi-rail regulators specifically designed for Spartan-3 FPGAs. The Xilinx Power Corner web page provides links to vendor solution guides as well as Xilinx power estimation and analysis tools.

Power Distribution System (PDS) Design and Bypass/Decoupling Capacitors

Good power distribution system (PDS) design is important for all FPGA designs, especially for high-performance applications. Proper design results in better overall performance, lower clock and DCM jitter, and a generally more robust system. Before designing the printed circuit board (PCB) for the FPGA design, review application note <u>XAPP623</u>: *Power Distribution System (PDS) Design: Using Bypass/Decoupling Capacitors*.

Power-On Behavior

Spartan-3 FPGAs have a built-in Power-On Reset (POR) circuit that monitors the three power rails required to successfully configure the FPGA. At power-up, the POR circuit holds the FPGA in a reset state until the V_{CCINT} , V_{CCAUX} , and V_{CCO} Bank 4 supplies reach their respective input threshold levels (see Table 29, page 59). After all three supplies reach their respective threshold, the POR reset is released and the FPGA begins its configuration process.

Because the three supply inputs must be valid to release the POR reset and can be supplied in any order, there are no specific voltage sequencing requirements. However, applying the FPGA's V_{CCAUX} supply before the V_{CCINT} supply uses the least I_{CCINT} current.

Once all three supplies are valid, the minimum current required to power-on the FPGA is equal to the worst-case quiescent current, as specified in Table 34, page 62. Spartan-3 FPGAs do not require Power-On Surge (POS) current to successfully configure.

Surplus I_{CCINT} if V_{CCINT} Applied before V_{CCAUX}

If the V_{CCINT} supply is applied before the V_{CCAUX} supply, the FPGA may draw a surplus I_{CCINT} current in addition to the I_{CCINT} quiescent current levels specified in Table 34. The momentary additional I_{CCINT} surplus current might be a few hundred milliamperes under nominal conditions, significantly less than the instantaneous current consumed by the bypass capacitors at power-on. However, the surplus current immediately disappears when the V_{CCAUX} supply is applied, and, in response, the FPGA's I_{CCINT} quiescent current demand drops to the levels specified in Table 34. The FPGA does not use nor does it require the surplus current to successfully power-on and configure. If applying V_{CCINT} before V_{CCAUX} , ensure that the regulator does not have a foldback feature that could inadvertently shut down in the presence of the surplus current.

Maximum Allowed V_{CCINT} Ramp Rate on Early Devices, if $V_{\text{VCCINT}} \text{Supply is Last in Sequence}$

All devices with a mask revision code 'E' or later do not have a V_{CCINT} ramp rate requirement. See Mask and Fab Revisions, page 58.

Early Spartan-3 FPGAs were produced at a 200 mm wafer production facility and are identified by a fabrication/process code of "FQ" on the device top marking, as shown in Package Marking, page 5. These "FQ" devices have a maximum V_{CCINT} ramp rate requirement if and only if V_{CCINT} is the last supply to ramp, after the V_{CCAUX} and V_{CCO} Bank 4 supplies. This maximum ramp rate appears as T_{CCINT} in Table 30, page 60.

Minimum Allowed V_{CCO} Ramp Rate on Early Devices

Devices shipped since 2006 essentially have no V_{CCO} ramp rate limits, shown in Table 30, page 60. Similarly, all devices with a mask revision code 'E' or later do not have a V_{CCO} ramp rate limit. See Mask and Fab Revisions, page 58.

Table 42: Setup and Hold Times for the IOB Input Path (Cont'd)

				Speed	Grade	
Symbol	Description	Conditions	Device	-5	-4	Units
				Min	Min	-
Hold Times						
T _{IOICKP}	Time from the active transition at the IFF's	LVCMOS25 ⁽³⁾ ,	XC3S50	-0.55	-0.55	ns
	ICLK input to the point where data must be held at the Input pin. No Input Delay is	IOBDELAY = NONE	XC3S200	-0.29	-0.29	ns
	programmed.		XC3S400	-0.29	-0.29	ns
			XC3S1000	-0.55	-0.55	ns
			XC3S1500	-0.55	-0.55	ns
			XC3S2000	-0.55	-0.55	ns
			XC3S4000	-0.61	-0.61	ns
			XC3S5000	-0.68	-0.68	ns
T _{IOICKPD}	Time from the active transition at the IFF's	LVCMOS25 ⁽³⁾ ,	XC3S50	-2.74	-2.74	ns
	held at the Input pin. The Input Delay is	IOBDELAY = IFD	XC3S200	-3.00	-3.00	ns
	programmed.		XC3S400	-2.90	-2.90	ns
			XC3S1000	-3.24	-3.24	ns
			XC3S1500	-3.55	-3.55	ns
			XC3S2000	-4.57	-4.57	ns
			XC3S4000	-4.96	-4.96	ns
			XC3S5000	-5.09	-5.09	ns
Set/Reset Pulse	Width					
T _{RPW_IOB}	Minimum pulse width to SR control input on IOB		All	0.66	0.76	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32 and Table 35.

2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, add the appropriate Input adjustment from Table 44.

3. These hold times require adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, subtract the appropriate Input adjustment from Table 44. When the hold time is negative, it is possible to change the data before the clock's active edge.

Table 48: Test Methods for Timing Measurement at I/Os (Cont'd)

Signal Standard			Inputs		Out	puts	Inputs and Outputs
(IUSTA	NDARD)	V _{REF} (V)	V _L (V)	V _H (V)	R _T (Ω)	V _T (V)	V _M (V)
HSTL_III_18		1.1	V _{REF} – 0.5	V _{REF} + 0.5	50	1.8	V _{REF}
HSTL_III_DC	CI_18						
LVCMOS12		-	0	1.2	1M	0	0.6
LVCMOS15		-	0	1.5	1M	0	0.75
LVDCI_15							
LVDCI_DV2_	15	-					
HSLVDCI_15	;	-					
LVCMOS18		-	0	1.8	1M	0	0.9
LVDCI_18		-					
LVDCI_DV2_	18	-					
HSLVDCI_18	5						
LVCMOS25		-	0	2.5	1M	0	1.25
LVDCI_25							
LVDCI_DV2_	25						
HSLVDCI_25	i						
LVCMOS33		-	0	3.3	1M	0	1.65
LVDCI_33		-					
LVDCI_DV2_	33	-					
HSLVDCI_33	5	-					
LVTTL		-	0	3.3	1M	0	1.4
PCI33_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
SSTL18_I		0.9	V _{REF} – 0.5	V _{REF} + 0.5	50	0.9	V _{REF}
SSTL18_I_D	CI						
SSTL18_II		0.9	V _{REF} – 0.5	V _{REF} + 0.5	50	0.9	V _{REF}
SSTL2_I		1.25	V _{REF} – 0.75	V _{REF} + 0.75	50	1.25	V _{REF}
SSTL2_I_DC	;						
SSTL2_II		1.25	V _{REF} – 0.75	V _{REF} + 0.75	25	1.25	V _{REF}
SSTL2_II_DO	CI				50	1.25	
Differential							
LDT_25 (ULV	/DS_25)	-	V _{ICM} – 0.125	V _{ICM} + 0.125	60	0.6	V _{ICM}
LVDS_25		-	V _{ICM} – 0.125	V _{ICM} + 0.125	50	1.2	V _{ICM}
LVDS_25_DC	CI				N/A	N/A	
BLVDS_25		-	V _{ICM} – 0.125	V _{ICM} + 0.125	1M	0	V _{ICM}
LVDSEXT_28	5	-	V _{ICM} – 0.125	V _{ICM} + 0.125	50	1.2	V _{ICM}
LVDSEXT_2	5_DCI				N/A	N/A	
LVPECL_25		-	V _{ICM} – 0.3	V _{ICM} + 0.3	1M	0	V _{ICM}
RSDS_25		-	V _{ICM} – 0.1	V _{ICM} + 0.1	50	1.2	V _{ICM}
DIFF_HSTL_	_II_18	-	V _{ICM} – 0.5	V _{ICM} + 0.5	50	1.8	V _{ICM}
DIFF_HSTL_	II_18_DCI						

Digital Clock Manager (DCM) Timing

For specification purposes, the DCM consists of three key components: the Delay-Locked Loop (DLL), the Digital Frequency Synthesizer (DFS), and the Phase Shifter (PS).

Aspects of DLL operation play a role in all DCM applications. All such applications inevitably use the CLKIN and the CLKFB inputs connected to either the CLK0 or the CLK2X feedback, respectively. Thus, specifications in the DLL tables (Table 58 and Table 59) apply to any application that only employs the DLL component. When the DFS and/or the PS components are used together with the DLL, then the specifications listed in the DFS and PS tables (Table 60 through Table 63) supersede any corresponding ones in the DLL tables. DLL specifications that do not change with the addition of DFS or PS functions are presented in Table 58 and Table 59.

Period jitter and cycle-cycle jitter are two (of many) different ways of characterizing clock jitter. Both specifications describe statistical variation from a mean value.

Period jitter is the worst-case deviation from the average clock period of all clock cycles in the collection of clock periods sampled (usually from 100,000 to more than a million samples for specification purposes). In a histogram of period jitter, the mean value is the clock period.

Cycle-cycle jitter is the worst-case difference in clock period between adjacent clock cycles in the collection of clock periods sampled. In a histogram of cycle-cycle jitter, the mean value is zero.

Delay-Locked Loop (DLL)

Table 58: Recommended Operating Conditions for the DLL

Symbol				Speed Grade				
		Description	Frequency Mode/	-5		-4		Units
			CERIN CONSC	Min	Max	Min	Max	
Input Fr	requency Ranges							
F _{CLKIN}	CLKIN_FREQ_DLL_LF	Frequency for the CLKIN input	Low	18 <mark>(2)</mark>	167 <mark>(3)</mark>	18 <mark>(2)</mark>	167 <mark>(3)</mark>	MHz
	CLKIN_FREQ_DLL_HF		High	48	280 ⁽³⁾	48	280 ⁽³⁾⁽⁴⁾	MHz
Input P	ulse Requirements							
CLKIN_	PULSE	CLKIN pulse width as a	$F_{CLKIN} \le 100 \text{ MHz}$	40%	60%	40%	60%	-
		percentage of the CLKIN period	F _{CLKIN} > 100 MHz	45%	55%	45%	55%	-
Input C	lock Jitter Tolerance and	Delay Path Variation ⁽⁵⁾						
CLKIN_	CYC_JITT_DLL_LF	Cycle-to-cycle jitter at the CLKIN	Low	-	±300	-	±300	ps
CLKIN_	CYC_JITT_DLL_HF	input	High	-	±150	-	±150	ps
CLKIN_	PER_JITT_DLL_LF	Period jitter at the CLKIN input	All	-	±1	-	±1	ns
CLKIN_PER_JITT_DLL_HF				-		-		
CLKFB_	DELAY_VAR_EXT	Allowable variation of off-chip feedback delay from the DCM output to the CLKFB input	All	-	±1	-	±1	ns

Notes:

1. DLL specifications apply when any of the DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV) are in use.

2. The DFS, when operating independently of the DLL, supports lower F_{CLKIN} frequencies. See Table 60.

 The CLKIN_DIVIDE_BY_2 attribute can be used to increase the effective input frequency range up to F_{BUFG}. When set to TRUE, CLKIN_DIVIDE_BY_2 divides the incoming clock frequency by two as it enters the DCM.

4. Industrial temperature range devices have additional requirements for continuous clocking, as specified in Table 64.

5. CLKIN input jitter beyond these limits may cause the DCM to lose lock. See UG331 for more details.

PRODUCT NOT RECOMMENDED FOR NEW DESIGNS

Spartan-3 FPGA Family: DC and Switching Characteristics



DS099-3_04_071604

Figure 37: Waveforms for Master and Slave Serial Configuration

Cumhal	Symbol		Slave/	All Spee	d Grades	Unite
Symbol	Descri	iption	Master	Min	Max	Units
Clock-to-O	utput Times					
T _{CCO}	The time from the falling transition on t DOUT pin	The time from the falling transition on the CCLK pin to data appearing at the DOUT pin				ns
Setup Time	95					
T _{DCC}	The time from the setup of data at the CCLK pin	DIN pin to the rising transition at the	Both	10.0	-	ns
Hold Times	5					
T _{CCD}	The time from the rising transition at the last held at the DIN pin	e CCLK pin to the point when data is	Both	0	-	ns
Clock Timi	ng					
Т _{ССН}	CCLK input pin High pulse width		Slave	5.0	~	ns
T _{CCL}	CCLK input pin Low pulse width			5.0	~	ns
F _{CCSER}	Frequency of the clock signal at the	No bitstream compression		0	66 <mark>(2)</mark>	MHz
CCLK input pin		With bitstream compression		0	20	MHz
		During STARTUP phase		0	50	MHz
ΔF_{CCSER}	Variation from the CCLK output freque option	ency set using the ConfigRate BitGen	Master	-50%	+50%	-

Table 66: Timing for the Master and Slave Serial Configuration Modes

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32.

2. For serial configuration with a daisy-chain of multiple FPGAs, the maximum limit is 25 MHz.

Table 86: Spartan-3 FPGA Package Thermal Characteristics (Cont'd)

		lunction-to-	lunction-to-B	Junction-to-	Ambient (θ _J ,) at Differer	nt Air Flows	
Package	Device Case (θ	Case (θ_{JC})	(θ_{JC}) oard (θ_{JB})	Still Air (0 LFM)	250 LFM	500 LFM	750 LFM	Units
FG(G)1156 ⁽¹⁾	XC3S4000	1.9	-	14.7	11.4	10.1	9.0	°C/Watt
	XC3S5000	1.9	8.9	14.5	11.3	10.0	8.9	°C/Watt

Notes:

1. The CP132, CPG132, FG1156, and FGG1156 packages are discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

VQ100: 100-lead Very-Thin Quad Flat Package

The XC3S50 and the XC3S200 devices are available in the 100-lead very-thin quad flat package, VQ100. Both devices share a common footprint for this package as shown in Table 87 and Figure 44.

All the package pins appear in Table 87 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_sheets/s3_pin.zip.

Pinout Table

Table 87: VQ100 Package Pinout

Bank	XC3S50 VQ100 XC3S200 Pin Pin Name Number		Туре
0	IO_L01N_0/VRP_0	P97	DCI
0	IO_L01P_0/VRN_0	P96	DCI
0	IO_L31N_0	P92	I/O
0	IO_L31P_0/VREF_0	P91	VREF
0	IO_L32N_0/GCLK7	P90	GCLK
0	IO_L32P_0/GCLK6	P89	GCLK
0	VCCO_0	P94	VCCO
1	Ю	P81	I/O
1	IO_L01N_1/VRP_1	P80	DCI
1	IO_L01P_1/VRN_1	P79	DCI
1	IO_L31N_1/VREF_1	P86	VREF
1	IO_L31P_1	P85	I/O
1	IO_L32N_1/GCLK5	P88	GCLK
1	IO_L32P_1/GCLK4	P87	GCLK
1	VCCO_1	P83	VCCO
2	IO_L01N_2/VRP_2	P75	DCI
2	IO_L01P_2/VRN_2	P74	DCI
2	IO_L21N_2	P72	I/O
2	IO_L21P_2	P71	I/O
2	IO_L24N_2	P68	I/O
2	IO_L24P_2	P67	I/O

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Table 87: VQ100 Package Pinout (Cont'd)

Bank	XC3S50 XC3S200 Pin Name	VQ100 Pin Number	Туре
VCCAUX	TDO	P76	JTAG
VCCAUX	TMS	P78	JTAG

User I/Os by Bank

Table 88 indicates how the available user-I/O pins are distributed between the eight I/O banks on the VQ100 package.

Paakaga Edga	I/O Bank	Maximum I/O		All Po	ossible I/O Pi	ns by Type	
r uokugo Eugo	1/O Dalik	Maximum 1/0	I/O	DUAL	DCI	VREF	GCLK
Top	0	6	1	0	2	1	2
тор	1	7	2	0	2	1	2
Disht	2	8	5	0	2	1	0
night	3	8	5	0	2	1	0
Bottom	4	10	0	6	2	0	2
Dottom	5	8	0	6	0	0	2
L off	6	8	4	0	2	2	0
Leit	7	8	5	0	2	1	0

Table 88: User I/Os Per Bank in VQ100 Package

Table 93: PQ208 Package Pinout (Cont'd)

Bank	XC3S50 Pin Name	XC3S200, XC3S400 Pin Names	PQ208 Pin Number	Туре
7	IO_L21N_7	IO_L21N_7	P13	I/O
7	IO_L21P_7	IO_L21P_7	P12	I/O
7	IO_L22N_7	IO_L22N_7	P16	I/O
7	IO_L22P_7	IO_L22P_7	P15	I/O
7	IO_L23N_7	IO_L23N_7	P19	I/O
7	IO_L23P_7	IO_L23P_7	P18	I/O
7	IO_L24N_7	IO_L24N_7	P21	I/O
7	IO_L24P_7	IO_L24P_7	P20	I/O
7	N.C. (�)	IO_L39N_7	P24	I/O
7	N.C. (�)	IO_L39P_7	P22	I/O
7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	P27	VREF
7	IO_L40P_7	IO_L40P_7	P26	I/O
7	VCCO_7	VCCO_7	P6	VCCO
7	VCCO_7	VCCO_7	P23	VCCO
N/A	GND	GND	P1	GND
N/A	GND	GND	P186	GND
N/A	GND	GND	P195	GND
N/A	GND	GND	P202	GND
N/A	GND	GND	P163	GND
N/A	GND	GND	P170	GND
N/A	GND	GND	P179	GND
N/A	GND	GND	P134	GND
N/A	GND	GND	P145	GND
N/A	GND	GND	P151	GND
N/A	GND	GND	P157	GND
N/A	GND	GND	P112	GND
N/A	GND	GND	P118	GND
N/A	GND	GND	P129	GND
N/A	GND	GND	P82	GND
N/A	GND	GND	P91	GND
N/A	GND	GND	P99	GND
N/A	GND	GND	P105	GND
N/A	GND	GND	P53	GND
N/A	GND	GND	P59	GND
N/A	GND	GND	P66	GND
N/A	GND	GND	P75	GND
N/A	GND	GND	P30	GND
N/A	GND	GND	P41	GND
N/A	GND	GND	P47	GND
N/A	GND	GND	P8	GND

Table 96: FT256 Package Pinout (Cont'd)

Bank	XC3S200, XC3S400, XC3S1000 Pin Name	FT256 Pin Number	Туре
1	IO_L10N_1/VREF_1	A13	VREF
1	IO_L10P_1	B13	I/O
1	IO_L27N_1	B12	I/O
1	IO_L27P_1	C12	I/O
1	IO_L28N_1	D11	I/O
1	IO_L28P_1	E11	I/O
1	IO_L29N_1	B11	I/O
1	IO_L29P_1	C11	I/O
1	IO_L30N_1	D10	I/O
1	IO_L30P_1	E10	I/O
1	IO_L31N_1/VREF_1	A10	VREF
1	IO_L31P_1	B10	I/O
1	IO_L32N_1/GCLK5	C9	GCLK
1	IO_L32P_1/GCLK4	D9	GCLK
1	VCCO_1	E9	VCCO
1	VCCO_1	F9	VCCO
1	VCCO_1	F10	VCCO
2	IO	G16	I/O
2	IO_L01N_2/VRP_2	B16	DCI
2	IO_L01P_2/VRN_2	C16	DCI
2	IO_L16N_2	C15	I/O
2	IO_L16P_2	D14	I/O
2	IO_L17N_2	D15	I/O
2	IO_L17P_2/VREF_2	D16	VREF
2	IO_L19N_2	E13	I/O
2	IO_L19P_2	E14	I/O
2	IO_L20N_2	E15	I/O
2	IO_L20P_2	E16	I/O
2	IO_L21N_2	F12	I/O
2	IO_L21P_2	F13	I/O
2	IO_L22N_2	F14	I/O
2	IO_L22P_2	F15	I/O
2	IO_L23N_2/VREF_2	G12	VREF
2	IO_L23P_2	G13	I/O
2	IO_L24N_2	G14	I/O
2	IO_L24P_2	G15	I/O
2	IO_L39N_2	H13	I/O
2	IO_L39P_2	H14	I/O
2	IO_L40N_2	H15	I/O
2	IO_L40P_2/VREF_2	H16	VREF

User I/Os by Bank

Table 101 indicates how the available user-I/O pins are distributed between the eight I/O banks for the XC3S400 in the FG456 package. Similarly, Table 102 shows how the available user-I/O pins are distributed between the eight I/O banks for the XC3S1000, XC3S1500, and XC3S2000 in the FG456 package.

Table 101. Usel 1/05 Fel Ballk IOI AC33400 III FG430 Fackag	Table	101:	: User I/Os	Per Bank for	XC3S400 in	FG456 Package
---	-------	------	-------------	--------------	------------	---------------

Edge	I/O	Moximum I/O		All P	ossible I/O Pi	ns by Type	
	Bank		I/O	DUAL	DCI	VREF	GCLK
Top	0	35	27	0	2	4	2
юр	1	35	27	0	2	4	2
Right	2	31	25	0	2	4	0
	3	31	25	0	2	4	0
Bottom	4	35	21	6	2	4	2
	5	35	21	6	2	4	2
Left	6	31	25	0	2	4	0
	7	31	25	0	2	4	0

Table 102: User I/Os Per Bank for XC3S1000, XC3S1500, and XC3S2000 in FG456 Package

Edge	I/O Bonk Movimum I/		All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Тор	0	40	31	0	2	5	2
	1	40	31	0	2	5	2
Right	2	43	37	0	2	4	0
	3	43	37	0	2	4	0
Bottom	4	41	26	6	2	5	2
	5	40	25	6	2	5	2
Left	6	43	37	0	2	4	0
	7	43	37	0	2	4	0

Table 103: FG676 Package Pinout (Cont'd)

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Туре
5	IO_L29P_5/VREF_5	IO_L29P_5/VREF_5	IO_L29P_5/VREF_5	IO_L29P_5/VREF_5	IO_L29P_5/VREF_5	AE12	VREF
5	IO_L30N_5	IO_L30N_5	IO_L30N_5	IO_L30N_5	IO_L30N_5	Y13	I/O
5	IO_L30P_5	IO_L30P_5	IO_L30P_5	IO_L30P_5	IO_L30P_5	W13	I/O
5	IO_L31N_5/D4	IO_L31N_5/D4	IO_L31N_5/D4	IO_L31N_5/D4	IO_L31N_5/D4	AC13	DUAL
5	IO_L31P_5/D5	IO_L31P_5/D5	IO_L31P_5/D5	IO_L31P_5/D5	IO_L31P_5/D5	AB13	DUAL
5	IO_L32N_5/GCLK3	IO_L32N_5/GCLK3	IO_L32N_5/GCLK3	IO_L32N_5/GCLK3	IO_L32N_5/GCLK3	AE13	GCLK
5	IO_L32P_5/GCLK2	IO_L32P_5/GCLK2	IO_L32P_5/GCLK2	IO_L32P_5/GCLK2	IO_L32P_5/GCLK2	AD13	GCLK
5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	AD7	VCCO
5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	AD11	VCCO
5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	U13	VCCO
5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	V11	VCCO
5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	V12	VCCO
5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	V13	VCCO
5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	W9	VCCO
5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	W10	VCCO
6	N.C. (�)	N.C. (■)	IO	IO	Ю	AA5	I/O
6	IO_L01N_6/VRP_6	IO_L01N_6/VRP_6	IO_L01N_6/VRP_6	IO_L01N_6/VRP_6	IO_L01N_6/VRP_6	AD2	DCI
6	IO_L01P_6/VRN_6	IO_L01P_6/VRN_6	IO_L01P_6/VRN_6	IO_L01P_6/VRN_6	IO_L01P_6/VRN_6	AD1	DCI
6	IO_L02N_6	IO_L02N_6	IO_L02N_6	IO_L02N_6	IO_L02N_6	AB4	I/O
6	IO_L02P_6	IO_L02P_6	IO_L02P_6	IO_L02P_6	IO_L02P_6	AB3	I/O
6	IO_L03N_6/VREF_6	IO_L03N_6/VREF_6	IO_L03N_6/VREF_6	IO_L03N_6/VREF_6	IO_L03N_6/VREF_6	AC2	VREF
6	IO_L03P_6	IO_L03P_6	IO_L03P_6	IO_L03P_6	IO_L03P_6	AC1	I/O
6	N.C. (�)	IO_L05N_6	IO_L05N_6	IO_L05N_6	IO_L05N_6	AB2	I/O
6	N.C. (�)	IO_L05P_6	IO_L05P_6	IO_L05P_6	IO_L05P_6	AB1	I/O
6	N.C. (�)	IO_L06N_6	IO_L06N_6	IO_L06N_6	IO_L06N_6	Y7	I/O
6	N.C. (�)	IO_L06P_6	IO_L06P_6	IO_L06P_6	IO_L06P_6	Y6	I/O
6	N.C. (�)	IO_L07N_6	IO_L07N_6	IO_L07N_6	IO_L07N_6	AA4	I/O
6	N.C. (�)	IO_L07P_6	IO_L07P_6	IO_L07P_6	IO_L07P_6	AA3	I/O
6	N.C. (�)	IO_L08N_6	IO_L08N_6	IO_L08N_6	IO_L08N_6	Y5	I/O
6	N.C. (�)	IO_L08P_6	IO_L08P_6	IO_L08P_6	IO_L08P_6	Y4	I/O
6	N.C. (�)	IO L09N 6/VREF 6	AA2	VREF			
6		IO L09P 6	IO L09P 6	IO L09P 6	IO L09P 6	AA1	I/O
6	N.C. (♦)	IO L10N 6	IO L10N 6	IO L10N 6	IO L10N 6	Y2	1/O
6	N.C. (♦)	IO L10P 6	IO L10P 6	IO L10P 6	IO L10P 6	Y1	I/O
6	IO I 14N 6	IO_114N_6	IO_L14N_6	IO_L14N_6	IO 14N 6	W7	1/0
6	IO I 14P 6	IO_114P_6	IO_L14P_6	IO_L14P_6	IO_L14P_6	W6	1/0
6	IO L16N 6	IO L16N 6	IO L16N 6	IO L16N 6	IO L16N 6	V6	
6				IO_L16P_6		W5	1/0
6	IO L17N 6	IO L17N 6	IO L17N 6	IO L17N 6	IO L17N 6	W4	1/0
6	IO L17P 6/VRFF 6	IO L17P 6/VRFF 6	IO L17P 6/VRFF 6	IO L17P 6/VRFF 6	IO L17P 6/VRFF 6	W3	VRFF
6	IO 19N 6	IO 19N 6	IO 19N 6	IO 19N 6	IO 19N 6	W2	1/0
6	IO 19P 6					W1	1/0
	.0_2.101_0		.00	.00	.00		.,0

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Table 107: FG900 Package Pinout (Cont'd)

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Туре
3	N.C. (♠)	IO_L50P_3	V26	I/O
3	VCCO_3	VCCO_3	U20	VCCO
3	VCCO_3	VCCO_3	V20	VCCO
3	VCCO_3	VCCO_3	W20	VCCO
3	VCCO_3	VCCO_3	Y22	VCCO
3	VCCO_3	VCCO_3	V24	VCCO
3	VCCO_3	VCCO_3	AB24	VCCO
3	VCCO_3	VCCO_3	AD26	VCCO
3	VCCO_3	VCCO_3	V28	VCCO
3	VCCO_3	VCCO_3	AB28	VCCO
3	VCCO_3	VCCO_3	AF28	VCCO
4	IO	IO	AA16	I/O
4	IO	IO	AG18	I/O
4	IO	IO	AA18	I/O
4	IO	IO	AE22	I/O
4	IO	IO	AD23	I/O
4	IO	IO	AH27	I/O
4	IO/VREF_4	IO/VREF_4	AF16	VREF
4	IO/VREF_4	IO/VREF_4	AK28	VREF
4	IO_L01N_4/VRP_4	IO_L01N_4/VRP_4	AJ27	DCI
4	IO_L01P_4/VRN_4	IO_L01P_4/VRN_4	AK27	DCI
4	IO_L02N_4	IO_L02N_4	AJ26	I/O
4	IO_L02P_4	IO_L02P_4	AK26	I/O
4	IO_L03N_4	IO_L03N_4	AG26	I/O
4	IO_L03P_4	IO_L03P_4	AF25	I/O
4	IO_L04N_4	IO_L04N_4	AD24	I/O
4	IO_L04P_4	IO_L04P_4	AC23	I/O
4	IO_L05N_4	IO_L05N_4	AE23	I/O
4	IO_L05P_4	IO_L05P_4	AF23	I/O
4	IO_L06N_4/VREF_4	IO_L06N_4/VREF_4	AG23	VREF
4	IO_L06P_4	IO_L06P_4	AH23	I/O
4	IO_L07N_4	IO_L07N_4	AJ23	I/O
4	IO_L07P_4	IO_L07P_4	AK23	I/O
4	IO_L08N_4	IO_L08N_4	AB22	I/O
4	IO_L08P_4	IO_L08P_4	AC22	I/O
4	IO_L09N_4	IO_L09N_4	AF22	I/O
4	IO_L09P_4	IO_L09P_4	AG22	I/O
4	IO_L10N_4	IO_L10N_4	AJ22	I/O
4	IO_L10P_4	IO_L10P_4	AK22	I/O
4	IO_L11N_4	IO_L11N_4	AD21	I/O

Table 107: FG900 Package Pinout (Cont'd)

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Туре
4	IO_L11P_4	IO_L11P_4	AE21	I/O
4	IO_L12N_4	IO_L12N_4	AH21	I/O
4	IO_L12P_4	IO_L12P_4	AJ21	I/O
4	IO_L13N_4	IO_L13N_4	AB21	I/O
4	IO_L13P_4	IO_L13P_4	AA20	I/O
4	IO_L14N_4	IO_L14N_4	AC20	I/O
4	IO_L14P_4	IO_L14P_4	AD20	I/O
4	IO_L15N_4	IO_L15N_4	AE20	I/O
4	IO_L15P_4	IO_L15P_4	AF20	I/O
4	IO_L16N_4	IO_L16N_4	AG20	I/O
4	IO_L16P_4	IO_L16P_4	AH20	I/O
4	IO_L17N_4	IO_L17N_4	AJ20	I/O
4	IO_L17P_4	IO_L17P_4	AK20	I/O
4	IO_L18N_4	IO_L18N_4	AA19	I/O
4	IO_L18P_4	IO_L18P_4	AB19	I/O
4	IO_L19N_4	IO_L19N_4	AC19	I/O
4	IO_L19P_4	IO_L19P_4	AD19	I/O
4	IO_L20N_4	IO_L20N_4	AE19	I/O
4	IO_L20P_4	IO_L20P_4	AF19	I/O
4	IO_L21N_4	IO_L21N_4	AG19	I/O
4	IO_L21P_4	IO_L21P_4	AH19	I/O
4	IO_L22N_4/VREF_4	IO_L22N_4/VREF_4	AJ19	VREF
4	IO_L22P_4	IO_L22P_4	AK19	I/O
4	IO_L23N_4	IO_L23N_4	AB18	I/O
4	IO_L23P_4	IO_L23P_4	AC18	I/O
4	IO_L24N_4	IO_L24N_4	AE18	I/O
4	IO_L24P_4	IO_L24P_4	AF18	I/O
4	IO_L25N_4	IO_L25N_4	AJ18	I/O
4	IO_L25P_4	IO_L25P_4	AK18	I/O
4	IO_L26N_4	IO_L26N_4	AA17	I/O
4	IO_L26P_4/VREF_4	IO_L26P_4/VREF_4	AB17	VREF
4	IO_L27N_4/DIN/D0	IO_L27N_4/DIN/D0	AD17	DUAL
4	IO_L27P_4/D1	IO_L27P_4/D1	AE17	DUAL
4	IO_L28N_4	IO_L28N_4	AH17	I/O
4	IO_L28P_4	IO_L28P_4	AJ17	I/O
4	IO_L29N_4	IO_L29N_4	AB16	I/O
4	IO_L29P_4	IO_L29P_4	AC16	I/O
4	IO_L30N_4/D2	IO_L30N_4/D2	AD16	DUAL
4	IO_L30P_4/D3	IO_L30P_4/D3	AE16	DUAL
4	IO_L31N_4/INIT_B	IO_L31N_4/INIT_B	AG16	DUAL

Table 110: FG1156 Package Pinout (Cont'd)

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Туре
2	IO_L41N_2	IO_L41N_2	F33	I/O
2	IO_L41P_2	IO_L41P_2	F34	I/O
2	N.C. (�)	IO_L42N_2	G31	I/O
2	N.C. (�)	IO_L42P_2	G32	I/O
2	IO_L45N_2	IO_L45N_2	L33	I/O
2	IO_L45P_2	IO_L45P_2	L34	I/O
2	IO_L46N_2	IO_L46N_2	M24	I/O
2	IO_L46P_2	IO_L46P_2	M25	I/O
2	IO_L47N_2	IO_L47N_2	M27	I/O
2	IO_L47P_2	IO_L47P_2	M28	I/O
2	IO_L48N_2	IO_L48N_2	M33	I/O
2	IO_L48P_2	IO_L48P_2	M34	I/O
2	N.C. (�)	IO_L49N_2	P25	I/O
2	N.C. (�)	IO_L49P_2	P26	I/O
2	IO_L50N_2	IO_L50N_2	P27	I/O
2	IO_L50P_2	IO_L50P_2	P28	I/O
2	N.C. (�)	IO_L51N_2	T24	I/O
2	N.C. (�)	IO_L51P_2	U24	I/O
2	VCCO_2	VCCO_2	D32	VCCO
2	VCCO_2	VCCO_2	H28	VCCO
2	VCCO_2	VCCO_2	H32	VCCO
2	VCCO_2	VCCO_2	L27	VCCO
2	VCCO_2	VCCO_2	L31	VCCO
2	VCCO_2	VCCO_2	N23	VCCO
2	VCCO_2	VCCO_2	N29	VCCO
2	VCCO_2	VCCO_2	N33	VCCO
2	VCCO_2	VCCO_2	P23	VCCO
2	VCCO_2	VCCO_2	R23	VCCO
2	VCCO_2	VCCO_2	R27	VCCO
2	VCCO_2	VCCO_2	T23	VCCO
2	VCCO_2	VCCO_2	T31	VCCO
3	Ю	IO	AH33	I/O
3	Ю	IO	AH34	I/O
3	Ю	Ю	V25	I/O
3	Ю	Ю	V26	I/O
3	IO_L01N_3/VRP_3	IO_L01N_3/VRP_3	AM34	DCI
3	IO_L01P_3/VRN_3	IO_L01P_3/VRN_3	AM33	DCI
3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	AL34	VREF
3	IO_L02P_3	IO_L02P_3	AL33	I/O
3	IO_L03N_3	IO_L03N_3	AK33	I/O

Revision History

Date	Version	Description
04/03/03	1.0	Initial Xilinx release.
04/21/03	1.1	Added information on the VQ100 package footprint, including a complete pinout table (Table 87) and footprint diagram (Figure 44). Updated Table 85 with final I/O counts for the VQ100 package. Also added final differential I/O pair counts for the TQ144 package. Added clarifying comments to HSWAP_EN pin description on page 119. Updated the footprint diagram for the FG900 package shown in Figure 55a and Figure 55b. Some thick lines separating I/O banks were incorrect. Made cosmetic changes to Figure 40, Figure 42, and Figure 43. Updated Xilinx hypertext links. Added XC3S200 and XC3S400 to Pin Name column in Table 91.
05/12/03	1.1.1	AM32 pin was missing GND label in FG1156 package diagram (Figure 53).
07/11/03	1.1.2	Corrected misspellings of GCLK in Table 69 and Table 70. Changed CMOS25 to LVCMOS25 in Dual-Purpose Pin I/O Standard During Configuration section. Clarified references to Module 2. For XC3S5000 in FG1156 package, corrected N.C. symbol to a black square in Table 110, key, and package drawing.
07/29/03	1.2	Corrected pin names on FG1156 package. Some package balls incorrectly included LVDS pair names. The affected balls on the FG1156 package include G1, G2, G33, G34, U9, U10, U25, U26, V9, V10, V25, V26, AH1, AH2, AH33, AH34. The number of LVDS pairs is unaffected. Modified affected balls and re-sorted rows in Table 110. Updated affected balls in Figure 53. Also updated ASCII and Excel electronic versions of FG1156 pinout.
08/19/03	1.2.1	Removed 100 MHz ConfigRate option in CCLK: Configuration Clock section and in Table 80. Added note that TDO is a totem-pole output in Table 77.
10/09/03	1.2.2	Some pins had incorrect bank designations and were improperly sorted in Table 93. No pin names or functions changed. Renamed DCI_IN to DCI and added black diamond to N.C. pins in Table 93. In Figure 47, removed some extraneous text from pin 106 and corrected spelling of pins 45, 48, and 81.
12/17/03	1.3	Added FG320 pin tables and pinout diagram (FG320: 320-lead Fine-pitch Ball Grid Array). Made cosmetic changes to the TQ144 footprint (Figure 46), the PQ208 footprint (Figure 47), the FG676 footprint (Figure 53), and the FG900 footprint (Figure 55). Clarified wording in Precautions When Using the JTAG Port in 3.3V Environments section.
02/27/04	1.4	Clarified wording in Using JTAG Port After Configuration section. In Table 81, reduced package height for FG320 and increased maximum I/O values for the FG676, FG900, and FG1156 packages.
07/13/04	1.5	Added information on lead-free (Pb-free) package options to the Package Overview section plus Table 81 and Table 83. Clarified the VRN_# reference resistor requirements for I/O standards that use single termination as described in the DCI Termination Types section and in Figure 42b. Graduated from Advance Product Specification to Product Specification.
08/24/04	1.5.1	Removed XC3S2000 references from FG1156: 1156-lead Fine-pitch Ball Grid Array.
01/17/05	1.6	Added XC3S50 in CP132 package option. Added XC3S2000 in FG456 package option. Added XC3S4000 in FG676 package option. Added Selecting the Right Package Option section. Modified or added Table 81, Table 83, Table 84, Table 85, Table 89, Table 90, Table 100, Table 102, Table 103, Table 106, Figure 45, and Figure 53.
08/19/05	1.7	Removed term "weak" from the description of pull-up and pull-down resistors. Added IDCODE Register values. Added signal integrity precautions to CCLK: Configuration Clock and indicated that CCLK should be treated as an I/O during Master mode in Table 79.
04/03/06	2.0	Added Package Thermal Characteristics. Updated Figure 41 to make it a more obvious example. Added detail about which pins have dedicated pull-up resistors during configuration, regardless of the HSWAP_EN value to Table 70 and to Pin Behavior During Configuration. Updated Precautions When Using the JTAG Port in 3.3V Environments.
04/26/06	2.1	Corrected swapped data row in Table 86. The Theta-JA with zero airflow column was swapped with the Theta-JC column. Made additional notations on CONFIG and JTAG pins that have pull-up resistors during configuration, regardless of the HSWAP_EN input.
05/25/07	2.2	Added link on page 128 to Material Declaration Data Sheets. Corrected units typo in Table 74. Added Note 1 to Table 103 about VREF for XC3S1500 in FG676.

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