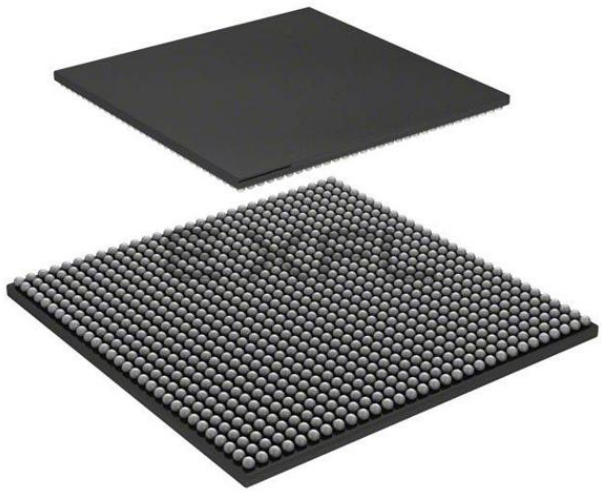
AMD Xilinx - XC3S5000-5FGG900C Datasheet



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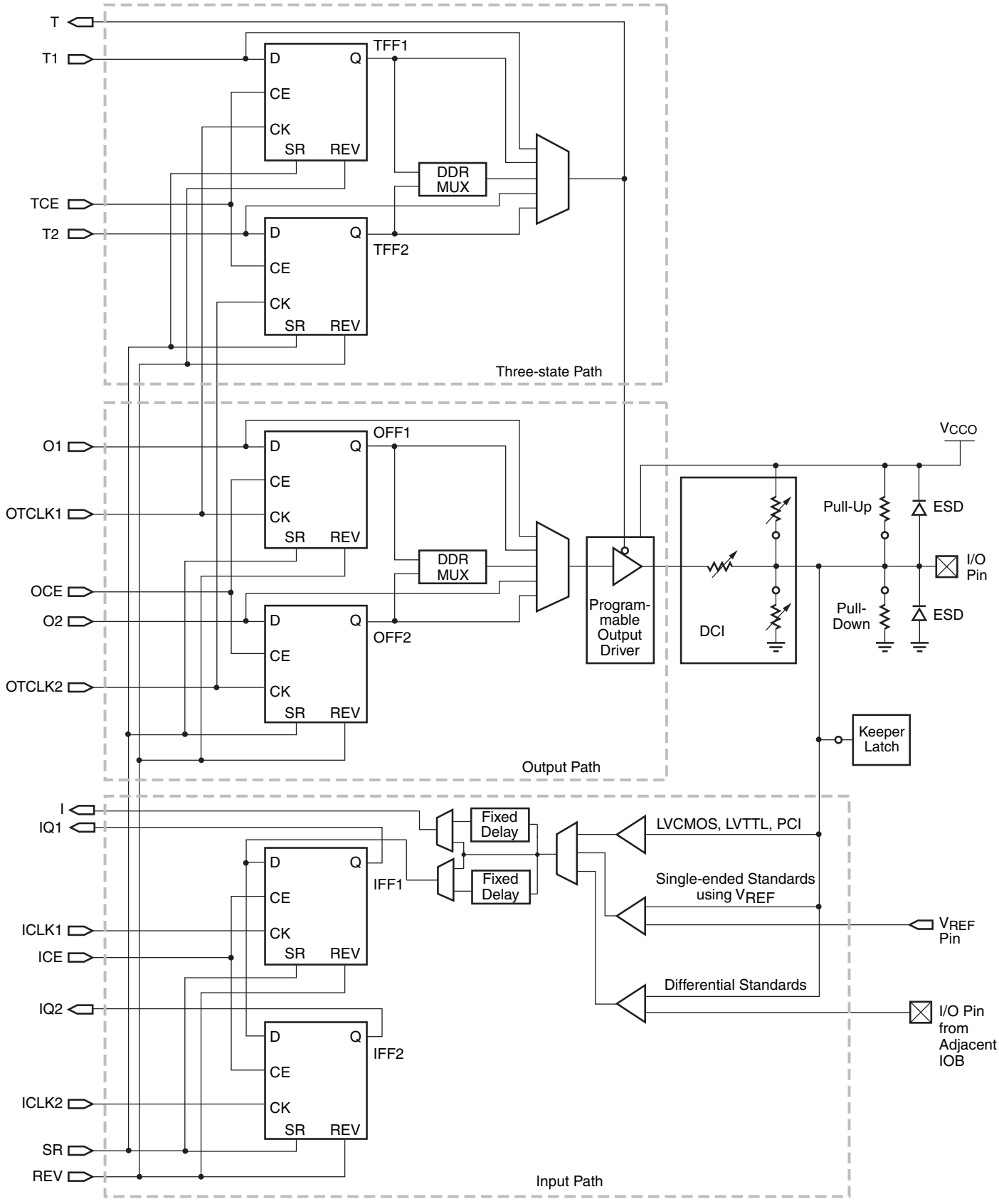
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	8320
Number of Logic Elements/Cells	74880
Total RAM Bits	1916928
Number of I/O	633
Number of Gates	5000000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	900-BBGA
Supplier Device Package	900-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s5000-5fgg900c



Note: All IOB signals originating from the FPGA's internal logic have an optional polarity inverter.

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Figure 7: **Simplified IOB Diagram**

Table 9: **Differential I/O Standards**

Signal Standard (IOSTANDARD)	V_{CCO} (Volts)		V_{REF} for Inputs (Volts)
	For Outputs	For Inputs	
LDT_25 (ULVDS_25)	2.5	–	–
LVDS_25	2.5	–	–
BLVDS_25	2.5	–	–
LVDSEXT_25	2.5	–	–
LVPECL_25	2.5	–	–
RSDS_25	2.5	–	–
DIFF_HSTL_II_18	1.8	–	–
DIFF_SSTL2_II	2.5	–	–

Notes:

1. See Table 10 for a listing of the differential DCI standards.

The need to supply V_{REF} and V_{CCO} imposes constraints on which standards can be used in the same bank. See The Organization of IOBs into Banks section for additional guidelines concerning the use of the V_{CCO} and V_{REF} lines.

Digitally Controlled Impedance (DCI)

When the round-trip delay of an output signal—i.e., from output to input and back again—exceeds rise and fall times, it is common practice to add termination resistors to the line carrying the signal. These resistors effectively match the impedance of a device's I/O to the characteristic impedance of the transmission line, thereby preventing reflections that adversely affect signal integrity. However, with the high I/O counts supported by modern devices, adding resistors requires significantly more components and board area. Furthermore, for some packages—e.g., ball grid arrays—it may not always be possible to place resistors close to pins.

DCI answers these concerns by providing two kinds of on-chip terminations: Parallel terminations make use of an integrated resistor network. Series terminations result from controlling the impedance of output drivers. DCI actively adjusts both parallel and series terminations to accurately match the characteristic impedance of the transmission line. This adjustment process compensates for differences in I/O impedance that can result from normal variation in the ambient temperature, the supply voltage and the manufacturing process. When the output driver turns off, the series termination, by definition, approaches a very high impedance; in contrast, parallel termination resistors remain at the targeted values.

DCI is available only for certain I/O standards, as listed in Table 10. DCI is selected by applying the appropriate I/O standard extensions to symbols or components. There are five basic ways to configure terminations, as shown in Table 11. The DCI I/O standard determines which of these terminations is put into effect.

HSTL_I_DCI-, HSTL_III_DCI-, and SSTL2_I_DCI-type outputs do not require the VRN and VRP reference resistors. Likewise, LVDCI-type inputs do not require the VRN and VRP reference resistors. In a bank without any DCI I/O or a bank containing non-DCI I/O and purely HSTL_I_DCI- or HSTL_III_DCI-type outputs, or SSTL2_I_DCI-type outputs or LVDCI-type inputs, the associated VRN and VRP pins can be used as general-purpose I/O pins.

The HSLVDCI (High-Speed LVDCI) standard is intended for bidirectional use. The driver is identical to LVDCI, while the input is identical to HSTL. By using a V_{REF}-referenced input, HSLVDCI allows greater input sensitivity at the receiver than when using a single-ended LVCMOS-type receiver.

Arrangement of RAM Blocks on Die

The XC3S50 has one column of block RAM. The Spartan-3 devices ranging from the XC3S200 to XC3S2000 have two columns of block RAM. The XC3S4000 and XC3S5000 have four columns. The position of the columns on the die is shown in Figure 1, page 3. For a given device, the total available RAM blocks are distributed equally among the columns. Table 12 shows the number of RAM blocks, the data storage capacity, and the number of columns for each device.

Table 12: **Number of RAM Blocks by Device**

Device	Total Number of RAM Blocks	Total Addressable Locations (Bits)	Number of Columns
XC3S50	4	73,728	1
XC3S200	12	221,184	2
XC3S400	16	294,912	2
XC3S1000	24	442,368	2
XC3S1500	32	589,824	2
XC3S2000	40	737,280	2
XC3S4000	96	1,769,472	4
XC3S5000	104	1,916,928	4

Block RAM and multipliers have interconnects between them that permit simultaneous operation; however, since the multiplier shares inputs with the upper data bits of block RAM, the maximum data path width of the block RAM is 18 bits in this case.

The Internal Structure of the Block RAM

The block RAM has a dual port structure. The two identical data ports called A and B permit independent access to the common RAM block, which has a maximum capacity of 18,432 bits—or 16,384 bits when no parity lines are used. Each port has its own dedicated set of data, control and clock lines for synchronous read and write operations. There are four basic data paths, as shown in Figure 13: (1) write to and read from Port A, (2) write to and read from Port B, (3) data transfer from Port A to Port B, and (4) data transfer from Port B to Port A.

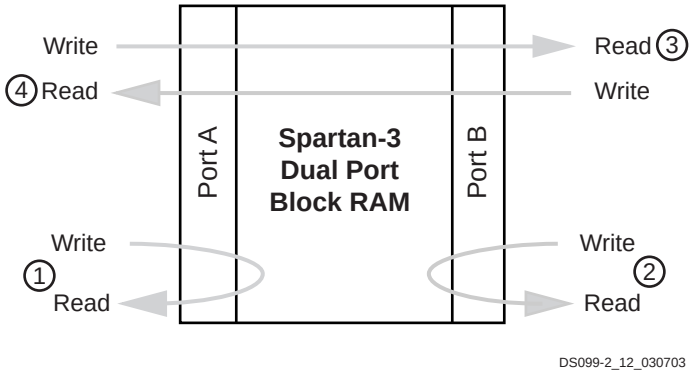
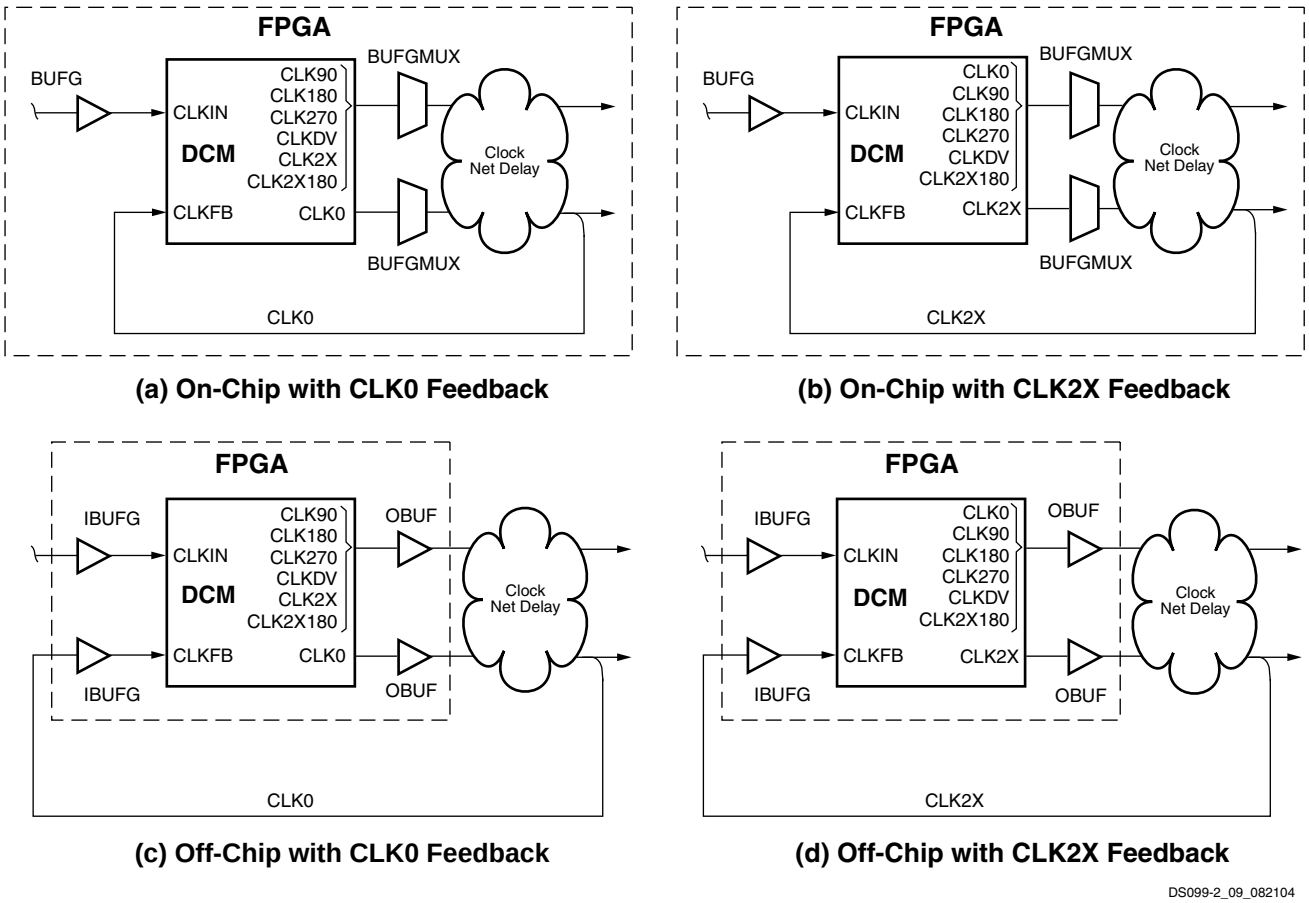


Figure 13: **Block RAM Data Paths**

Block RAM Port Signal Definitions

Representations of the dual-port primitive RAMB16_S[w_A]_S[w_B] and the single-port primitive RAMB16_S[w] with their associated signals are shown in Figure 14. These signals are defined in Table 13.



(a) On-Chip with CLK0 Feedback

(b) On-Chip with CLK2X Feedback

(c) Off-Chip with CLK0 Feedback

(d) Off-Chip with CLK2X Feedback

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Notes:

1. In the Low Frequency mode, all seven DLL outputs are available. In the High Frequency mode, only the CLK0, CLK180, and CLKDV outputs are available.

Figure 21: **Input Clock, Output Clock, and Feedback Connections for the DLL**

In the on-chip synchronization case (the [a] and [b] sections of Figure 21), it is possible to connect any of the DLL's seven output clock signals through general routing resources to the FPGA's internal registers. Either a Global Clock Buffer (BUFG) or a BUFGMUX affords access to the global clock network. As shown in the [a] section of Figure 21, the feedback loop is created by routing CLK0 (or CLK2X, in the [b] section) to a global clock net, which in turn drives the CLKFB input.

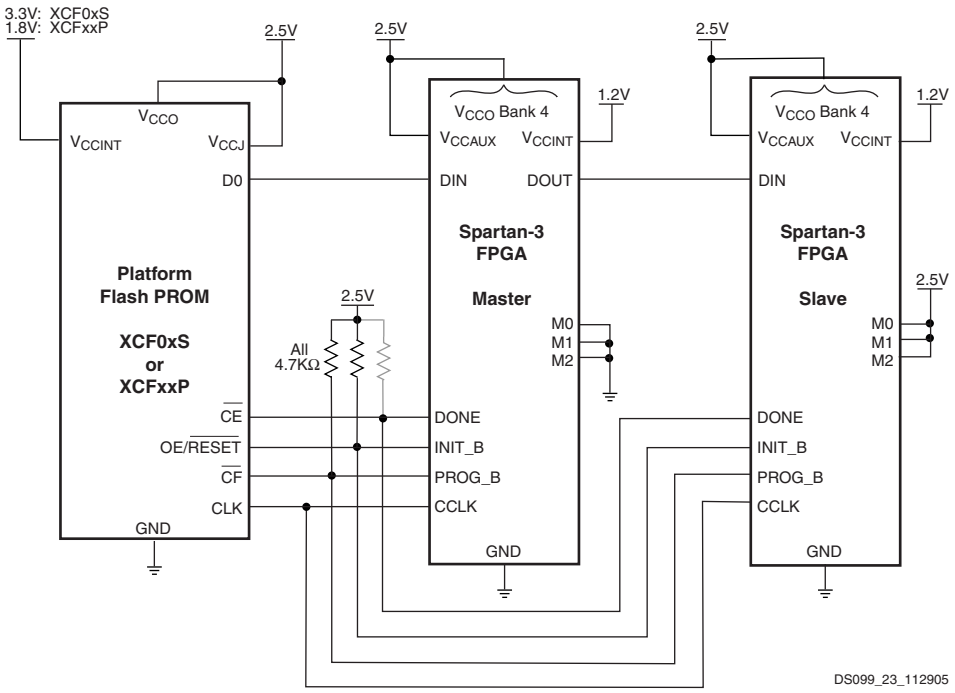
In the off-chip synchronization case (the [c] and [d] sections of Figure 21), CLK0 (or CLK2X) plus any of the DLL's other output clock signals exit the FPGA using output buffers (OBUF) to drive an external clock network plus registers on the board. As shown in the [c] section of Figure 21, the feedback loop is formed by feeding CLK0 (or CLK2X, in the [d] section) back into the FPGA using an IBUFG, which directly accesses the global clock network, or an IBUF. Then, the global clock net is connected directly to the CLKFB input.

DLL Frequency Modes

The DLL supports two distinct operating modes, High Frequency and Low Frequency, with each specified over a different clock frequency range. The DLL_FREQUENCY_MODE attribute chooses between the two modes. When the attribute is set to LOW, the Low Frequency mode permits all seven DLL clock outputs to operate over a low-to-moderate frequency range. When the attribute is set to HIGH, the High Frequency mode allows the CLK0, CLK180 and CLKDV outputs to operate at the highest possible frequencies. The remaining DLL clock outputs are not available for use in High Frequency mode.

Accommodating High Input Frequencies

If the frequency of the CLKIN signal is high such that it exceeds the maximum permitted, divide it down to an acceptable value using the CLKIN_DIVIDE_BY_2 attribute. When this attribute is set to TRUE, the CLKIN frequency is divided by a factor of two just as it enters the DCM.



Notes:

1. There are two ways to use the DONE line. First, one may set the BitGen option DriveDone to "Yes" only for the last FPGA to be configured in the chain shown above (or for the single FPGA as may be the case). This enables the DONE pin to drive High; thus, no pull-up resistor is necessary. DriveDone is set to "No" for the remaining FPGAs in the chain. Second, DriveDone can be set to "No" for all FPGAs. Then all DONE lines are open-drain and require the pull-up resistor shown in grey. In most cases, a value between 3.3KΩ to 4.7KΩ is sufficient. However, when using DONE synchronously with a long chain of FPGAs, cumulative capacitance may necessitate lower resistor values (e.g. down to 330Ω) in order to ensure a rise time within one clock cycle.
2. For information on how to program the FPGA using 3.3V signals and power, see 3.3V-Tolerant Configuration Interface.

Figure 26: **Connection Diagram for Master and Slave Serial Configuration**

Slave Serial mode is selected by applying <111> to the mode pins (M0, M1, and M2). A pull-up on the mode pins makes slave serial the default mode if the pins are left unconnected.

Master Serial Mode

In Master Serial mode, the FPGA drives CCLK pin, which behaves as a bidirectional I/O pin. The FPGA in the center of Figure 26 is set for Master Serial mode and connects to the serial configuration PROM and to the CCLK inputs of any slave FPGAs in a configuration daisy-chain. The master FPGA drives the configuration clock on the CCLK pin to the Xilinx Serial PROM, which, in response, provides bit-serial data to the FPGA's DIN input. The FPGA accepts this data on each rising CCLK edge. After the master FPGA finishes configuring, it passes data on its DOUT pin to the next FPGA device in a daisy-chain. The DOUT data appears after the falling CCLK clock edge.

The Master Serial mode interface is identical to Slave Serial except that an internal oscillator generates the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK, which always starts at a default frequency of 6 MHz. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration.

Slave Parallel Mode (SelectMAP)

The Parallel or SelectMAP modes support the fastest configuration. Byte-wide data is written into the FPGA with a BUSY flag controlling the flow of data. An external source provides 8-bit-wide data, CCLK, an active-Low Chip Select (CS_B) signal and an active-Low Write signal (RDWR_B). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low. Data can also be read using the Slave Parallel mode. If RDWR_B is asserted, configuration data is read out of the FPGA as part of a readback operation.

After configuration, it is possible to use any of the Multipurpose pins (DIN/D0-D7, DOUT/BUSY, INIT_B, CS_B, and RDWR_B) as User I/Os. To do this, simply set the BitGen option *Persist* to *No* and assign the desired signals to multipurpose configuration pins using the Xilinx development software. Alternatively, it is possible to continue using the configuration port

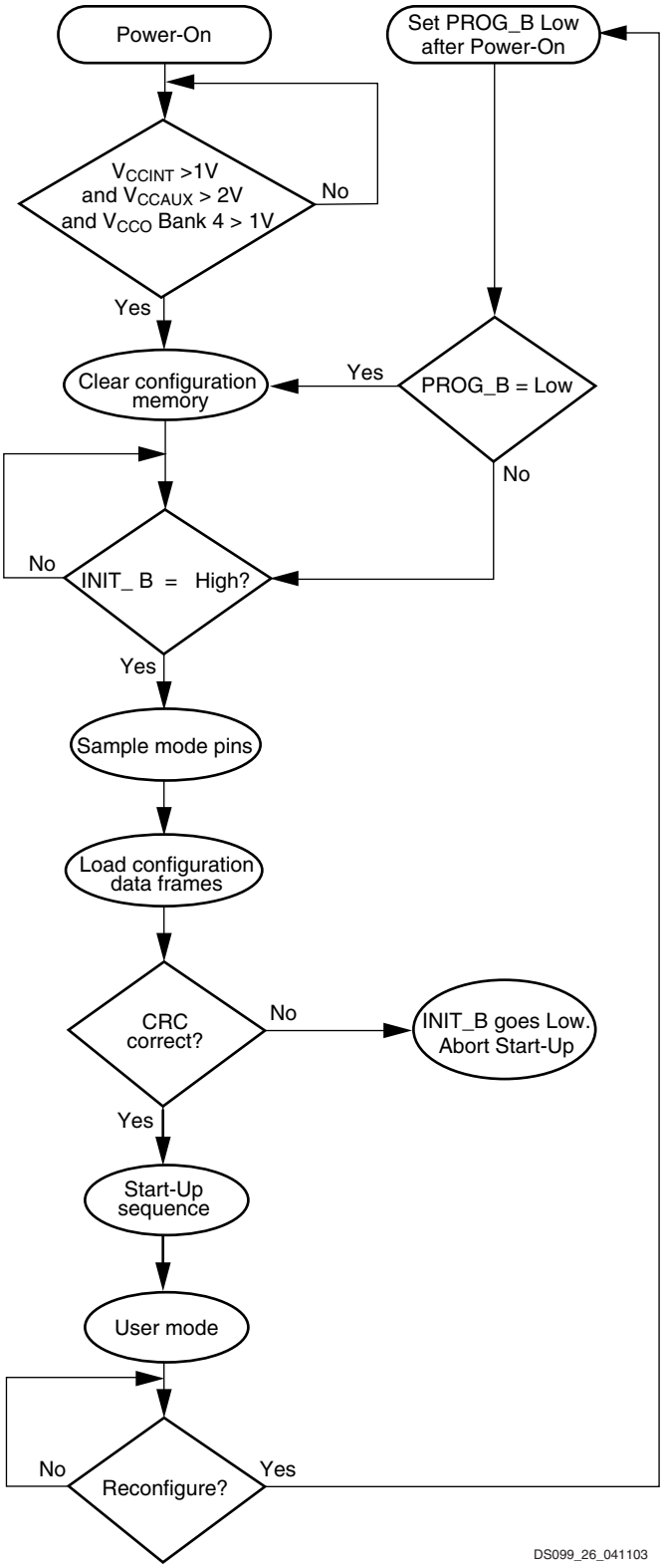


Figure 29: **Configuration Flow Diagram for the Serial and Parallel Modes**

Revision History

Date	Version No.	Description
04/11/03	1.0	Initial Xilinx release
05/19/03	1.1	Added Block RAM column, DCMs, and multipliers to XC3S50 descriptions.
07/11/03	1.2	Explained the configuration port *Persist* option in Slave Parallel Mode (SelectMAP) section. Updated Figure 8 and Double-Data-Rate Transmission section to indicate that DDR clocking for the XC3S50 is the same as that for all other Spartan-3 devices. Updated description of I/O voltage tolerance in ESD Protection section. In Table 10, changed input termination type for DCI version of the LVCMOS standard to *None*. Added additional flexibility for making DLL connections in Figure 21 and accompanying text. In the Configuration section, inserted an explanation of how to choose power supplies for the configuration interface, including guidelines for achieving 3.3V-tolerance.
08/24/04	1.3	Showed inversion of 3-state signal (Figure 7). Clarified description of pull-up and pull-down resistors (Table 6 and page 13). Added information on operating block RAM with multipliers to page 26. Corrected output buffer name in Figure 21. Corrected description of how DOUT is synchronized to CCLK (page 47).
08/19/05	1.4	Corrected description of WRITE_FIRST and READ_FIRST in Table 13. Added note regarding address setup and hold time requirements whenever a block RAM port is enabled (Table 13). Added information in the maximum length of a Configuration daisy-chain. Added reference to XAPP453 in 3.3V-Tolerant Configuration Interface section. Added information on the STATUS[2] DCM output (Table 23). Added information on CCLK behavior and termination recommendations to Configuration. Added Additional Configuration Details section. Added Powering Spartan-3 FPGAs section. Removed GSR from Figure 31 because its timing is not programmable.
04/03/06	2.0	Updated Figure 7. Updated Figure 14. Updated Table 10. Updated Figure 22. Corrected Platform Flash supply voltage name and value in Figure 26 and Figure 28. Added No Internal Charge Pumps or Free-Running Oscillators. Corrected a few minor typographical errors.
04/26/06	2.1	Added more information on the pull-up resistors that are active during configuration to Configuration. Added information to Boundary-Scan (JTAG) Mode about potential interactions when configuring via JTAG if the mode select pins are set for other than JTAG.
05/25/07	2.2	Added Spartan-3 FPGA Design Documentation. Noted SSTL2_I_DCI 25-Ohm driver in Table 10 and Table 11. Added note that pull-down is active during boundary scan tests.
11/30/07	2.3	Updated links to documentation on xilinx.com.
06/25/08	2.4	Added HSLVDCI to Table 10. Updated formatting and links.
12/04/09	2.5	Updated HSLVDCI description in Digitally Controlled Impedance (DCI). Updated the low-voltage differential signaling V_{CCO} values in Table 10. Noted that the CP132 package is being discontinued in The Organization of IOBs into Banks. Updated rule 4 in Rules Concerning Banks. Added software version requirement in The Fixed Phase Mode.
10/29/12	3.0	Added Notice of Disclaimer. Per XCN07022, updated the discontinued FG1156 and FGG1156 package discussion throughout document. Per XCN08011, updated the discontinued CP132 and CPG132 package discussion throughout document. This product is not recommended for new designs.

Table 36: **DC Characteristics of User I/Os Using Single-Ended Standards**

Signal Standard (IOSTANDARD) and Current Drive Attribute (mA)		Test Conditions		Logic Level Characteristics	
		I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
GTL		32	–	0.4	–
GTL_DCI		Note 3	Note 3		
GTLP		36	–	0.6	–
GTLP_DCI		Note 3	Note 3		
HSLVDCI_15		Note 3	Note 3	0.4	V_{CCO} – 0.4
HSLVDCI_18					
HSLVDCI_25					
HSLVDCI_33					
HSTL_I		8	–8	0.4	V_{CCO} – 0.4
HSTL_I_DCI		Note 3	Note 3		
HSTL_III		24	–8	0.4	V_{CCO} – 0.4
HSTL_III_DCI		Note 3	Note 3		
HSTL_I_18		8	–8	0.4	V_{CCO} – 0.4
HSTL_I_DCI_18		Note 3	Note 3		
HSTL_II_18		16	–16	0.4	V_{CCO} – 0.4
HSTL_II_DCI_18		Note 3	Note 3		
HSTL_III_18		24	–8	0.4	V_{CCO} – 0.4
HSTL_III_DCI_18		Note 3	Note 3		
LVCMOS12(4)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
LVCMOS15(4)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
LVDCI_15, LVDCI_DV2_15		Note 3	Note 3		
LVCMOS18(4)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
LVDCI_18, LVDCI_DV2_18		Note 3	Note 3		
LVCMOS25(4,5)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24	24	–24		
LVDCI_25, LVDCI_DV2_25		Note 3	Note 3		

Table 59: **Switching Characteristics for the DLL**

Symbol	Description	Frequency Mode / FCLKIN Range	Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Output Frequency Ranges								
CLKOUT_FREQ_1X_LF	Frequency for the CLK0, CLK90, CLK180, and CLK270 outputs	Low	All	18	167	18	167	MHz
CLKOUT_FREQ_1X_HF	Frequency for the CLK0 and CLK180 outputs	High		48	280	48	280	MHz
CLKOUT_FREQ_2X_LF(3)	Frequency for the CLK2X and CLK2X180 outputs	Low		36	334	36	334	MHz
CLKOUT_FREQ_DV_LF	Frequency for the CLKDV output	Low		1.125	110	1.125	110	MHz
CLKOUT_FREQ_DV_HF		High		3	185	3	185	MHz
Output Clock Jitter(4)								
CLKOUT_PER_JITT_0	Period jitter at the CLK0 output	All	All	–	±100	–	±100	ps
CLKOUT_PER_JITT_90	Period jitter at the CLK90 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_180	Period jitter at the CLK180 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_270	Period jitter at the CLK270 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_2X	Period jitter at the CLK2X and CLK2X180 outputs			–	±200	–	±200	ps
CLKOUT_PER_JITT_DV1	Period jitter at the CLKDV output when performing integer division			–	±150	–	±150	ps
CLKOUT_PER_JITT_DV2	Period jitter at the CLKDV output when performing non-integer division			–	±300	–	±300	ps
Duty Cycle								
CLKOUT_DUTY_CYCLE_DLL(5)	Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs	All	XC3S50	–	±150	–	±150	ps
			XC3S200	–	±150	–	±150	ps
			XC3S400	–	±250	–	±250	ps
			XC3S1000	–	±400	–	±400	ps
			XC3S1500	–	±400	–	±400	ps
			XC3S2000	–	±400	–	±400	ps
			XC3S4000	–	±400	–	±400	ps
			XC3S5000	–	±400	–	±400	ps
Phase Alignment								
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs	All	All	–	±150	–	±150	ps
CLKOUT_PHASE	Phase offset between any two DLL outputs (except CLK2X and CLK0)			–	±140	–	±140	ps
	Phase offset between the CLK2X and CLK0 outputs			–	±250	–	±250	ps

Phase Shifter (PS)

Phase shifter operation is only supported if the DLL is in low-frequency mode, see Table 58. Fixed phase shift requires ISE software version 10.1.03 (or later).

Table 62: **Recommended Operating Conditions for the PS in Variable Phase Mode**

Symbol	Description	Frequency Mode/ F_{CLKIN} Range		Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Operating Frequency Ranges								
PSCLK_FREQ (F_{PSCLK})	Frequency for the PSCLK input	Low		1	167	1	167	MHz
Input Pulse Requirements								
PSCLK_PULSE	PSCLK pulse width as a percentage of the PSCLK period	Low	$F_{CLKIN} \leq 100$ MHz	40%	60%	40%	60%	-
			$F_{CLKIN} > 100$ MHz	45%	55%	45%	55%	-

Table 63: **Switching Characteristics for the PS in Variable or Fixed Phase Shift Mode**

Symbol	Description	Frequency Mode/ F_{CLKIN} Range	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Phase Shifting Range							
FINE_SHIFT_RANGE	Phase shift range	Low	–	10.0	–	10.0	ns
Lock Time							
LOCK_DLL_PS	When using the PS in conjunction with the DLL: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase.	18 MHz $\leq F_{CLKIN} \leq$ 30 MHz	–	3.28	–	3.28	ms
		30 MHz $< F_{CLKIN} \leq$ 40 MHz	–	2.56	–	2.56	ms
		40 MHz $< F_{CLKIN} \leq$ 50 MHz	–	1.60	–	1.60	ms
		50 MHz $< F_{CLKIN} \leq$ 60 MHz	–	1.00	–	1.00	ms
		60 MHz $< F_{CLKIN} \leq$ 165 MHz	–	0.88	–	0.88	ms
LOCK_DLL_PS_FX	When using the PS in conjunction with the DLL and DFS: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase.	Low	–	10.40	–	10.40	ms

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32 and Table 62.
2. The PS specifications in this table apply when the PS attribute CLKOUT_PHASE_SHIFT= VARIABLE or FIXED.

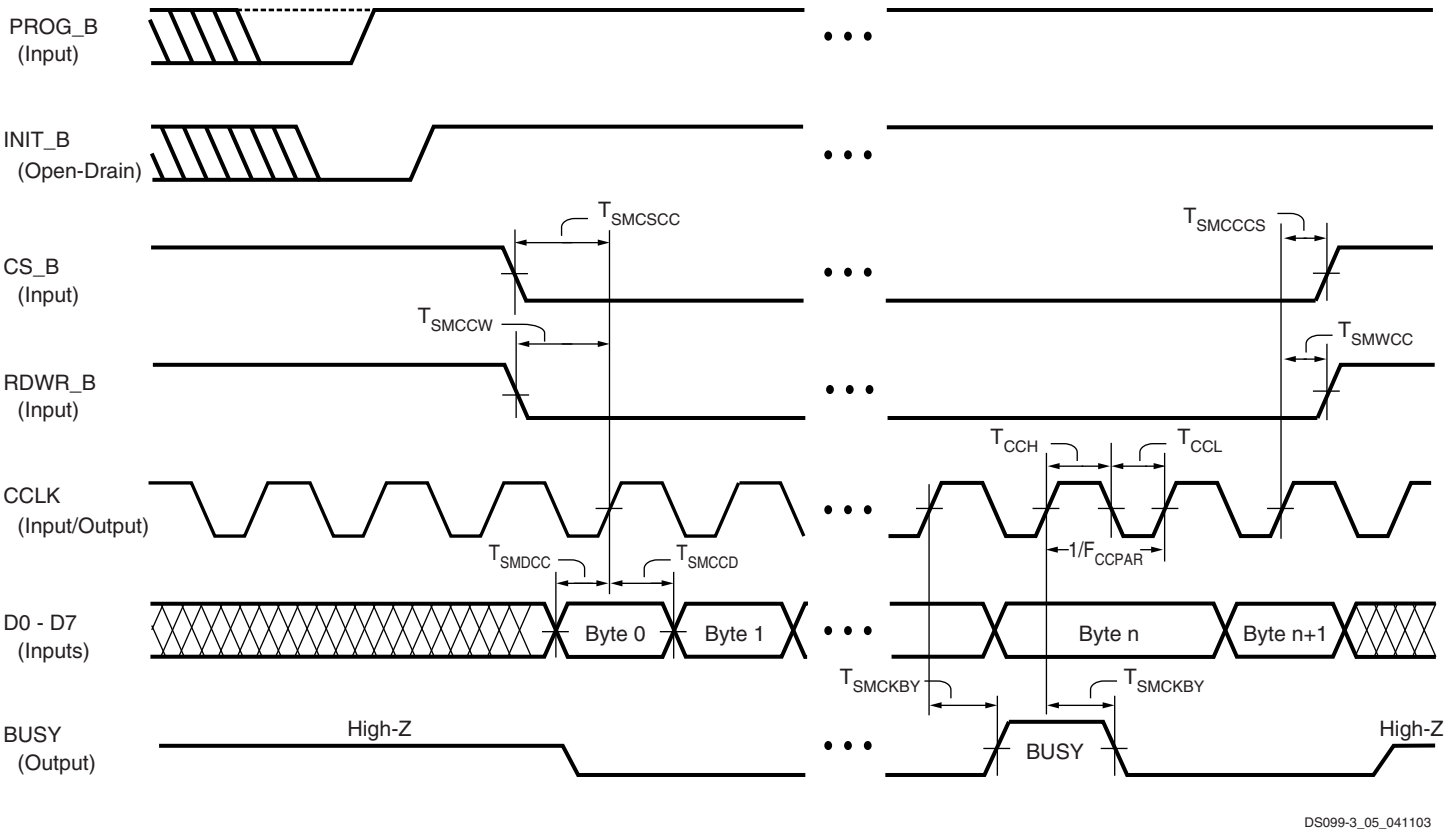


Figure 38: **Waveforms for Master and Slave Parallel Configuration**

Table 67: **Timing for the Master and Slave Parallel Configuration Modes**

Symbol	Description	Slave/ Master	All Speed Grades		Units
			Min	Max	
Clock-to-Output Times					
T_{SMCKBY}	The time from the rising transition on the CCLK pin to a signal transition at the BUSY pin	Slave	–	12.0	ns
Setup Times					
T_{SMDCC}	The time from the setup of data at the D0-D7 pins to the rising transition at the CCLK pin	Both	10.0	–	ns
T_{SMCSCC}	The time from the setup of a logic level at the CS_B pin to the rising transition at the CCLK pin		10.0	–	ns
T_{SMCCW}(3)	The time from the setup of a logic level at the RDWR_B pin to the rising transition at the CCLK pin		10.0	–	ns
Hold Times					
T_{SMCCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the D0-D7 pins	Both	0	–	ns
T_{SMCCCS}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the CS_B pin		0	–	ns
T_{SMWCC}(3)	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the RDWR_B pin		0	–	ns

Table 70: **Spartan-3 FPGA Pin Definitions *(Cont'd)***

Pin Name	Direction	Description
TDI	Input	**JTAG Test Data Input:** TDI is the serial data input for all JTAG instruction and data registers. This pin has an internal pull-up resistor to VCCAUX during configuration.
TMS	Input	**JTAG Test Mode Select:** The serial TMS input controls the operation of the JTAG port. This pin has an internal pull-up resistor to VCCAUX during configuration.
TDO	Output	**JTAG Test Data Output:** TDO is the serial data output for all JTAG instruction and data registers. This pin has an internal pull-up resistor to VCCAUX during configuration.
VCCO: I/O bank output voltage supply pins		
VCCO_#	Supply	**Power Supply for Output Buffer Drivers (per bank):** These pins power the output drivers within a specific I/O bank.
VCCAUX: Auxiliary voltage supply pins		
VCCAUX	Supply	**Power Supply for Auxiliary Circuits:** +2.5V power pins for auxiliary circuits, including the Digital Clock Managers (DCMs), the dedicated configuration pins (CONFIG), and the dedicated JTAG pins. All VCCAUX pins must be connected.
VCCINT: Internal core voltage supply pins		
VCCINT	Supply	**Power Supply for Internal Core Logic:** +1.2V power pins for the internal logic. All pins must be connected.
GND: Ground supply pins		
GND	Supply	**Ground:** Ground pins, which are connected to the power supply's return path. All pins must be connected.
N.C.: Unconnected package pins		
N.C.		**Unconnected Package Pin:** These package pins are unconnected.

Notes:

1. All unused inputs and bidirectional pins must be tied either High or Low. For unused enable inputs, apply the level that disables the associated function. One common approach is to activate internal pull-up or pull-down resistors. An alternative approach is to externally connect the pin to either VCCO or GND.
2. All outputs are of the totem-pole type — i.e., they can drive High as well as Low logic levels — except for the cases where "Open Drain" is indicated. The latter can only drive a Low logic level and require a pull-up resistor to produce a High logic level.

Detailed, Functional Pin Descriptions

I/O Type: Unrestricted, General-purpose I/O Pins

After configuration, I/O-type pins are inputs, outputs, bidirectional I/O, three-state outputs, open-drain outputs, or open-source outputs, as defined in the application

Pins labeled "IO" support all SelectIO™ interface signal standards except differential standards. A given device at most only has a few of these pins.

A majority of the general-purpose I/O pins are labeled in the format "IO_Lxxy_#". These pins support all SelectIO signal standards, including the differential standards such as LVDS, ULVDS, BLVDS, RSDS, or LDT.

For additional information, see IOBs, page 10

Table 93: **PQ208 Package Pinout *(Cont'd)***

Bank	XC3S50 Pin Name	XC3S200, XC3S400 Pin Names	PQ208 Pin Number	Type
3	IO_L20P_3	IO_L20P_3	P114	I/O
3	IO_L21N_3	IO_L21N_3	P117	I/O
3	IO_L21P_3	IO_L21P_3	P116	I/O
3	IO_L22N_3	IO_L22N_3	P120	I/O
3	IO_L22P_3	IO_L22P_3	P119	I/O
3	IO_L23N_3	IO_L23N_3	P123	I/O
3	IO_L23P_3/VREF_3	IO_L23P_3/VREF_3	P122	VREF
3	IO_L24N_3	IO_L24N_3	P125	I/O
3	IO_L24P_3	IO_L24P_3	P124	I/O
3	N.C. (◆)	IO_L39N_3	P128	I/O
3	N.C. (◆)	IO_L39P_3	P126	I/O
3	IO_L40N_3/VREF_3	IO_L40N_3/VREF_3	P131	VREF
3	IO_L40P_3	IO_L40P_3	P130	I/O
3	VCCO_3	VCCO_3	P110	VCCO
3	VCCO_3	VCCO_3	P127	VCCO
4	IO	IO	P93	I/O
4	N.C. (◆)	IO	P97	I/O
4	IO/VREF_4	IO/VREF_4	P85	VREF
4	N.C. (◆)	IO/VREF_4	P96	VREF
4	IO/VREF_4	IO/VREF_4	P102	VREF
4	IO_L01N_4/VRP_4	IO_L01N_4/VRP_4	P101	DCI
4	IO_L01P_4/VRN_4	IO_L01P_4/VRN_4	P100	DCI
4	IO_L25N_4	IO_L25N_4	P95	I/O
4	IO_L25P_4	IO_L25P_4	P94	I/O
4	IO_L27N_4/DIN/D0	IO_L27N_4/DIN/D0	P92	DUAL
4	IO_L27P_4/D1	IO_L27P_4/D1	P90	DUAL
4	IO_L30N_4/D2	IO_L30N_4/D2	P87	DUAL
4	IO_L30P_4/D3	IO_L30P_4/D3	P86	DUAL
4	IO_L31N_4/INIT_B	IO_L31N_4/INIT_B	P83	DUAL
4	IO_L31P_4/DOUT/BUSY	IO_L31P_4/DOUT/BUSY	P81	DUAL
4	IO_L32N_4/GCLK1	IO_L32N_4/GCLK1	P80	GCLK
4	IO_L32P_4/GCLK0	IO_L32P_4/GCLK0	P79	GCLK
4	VCCO_4	VCCO_4	P84	VCCO
4	VCCO_4	VCCO_4	P98	VCCO
5	IO	IO	P63	I/O
5	IO	IO	P71	I/O
5	IO/VREF_5	IO/VREF_5	P78	VREF
5	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	P58	DUAL
5	IO_L01P_5/CS_B	IO_L01P_5/CS_B	P57	DUAL
5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	P62	DCI

Table 93: **PQ208 Package Pinout *(Cont'd)***

Bank	XC3S50 Pin Name	XC3S200, XC3S400 Pin Names	PQ208 Pin Number	Type
7	IO_L21N_7	IO_L21N_7	P13	I/O
7	IO_L21P_7	IO_L21P_7	P12	I/O
7	IO_L22N_7	IO_L22N_7	P16	I/O
7	IO_L22P_7	IO_L22P_7	P15	I/O
7	IO_L23N_7	IO_L23N_7	P19	I/O
7	IO_L23P_7	IO_L23P_7	P18	I/O
7	IO_L24N_7	IO_L24N_7	P21	I/O
7	IO_L24P_7	IO_L24P_7	P20	I/O
7	N.C. (◆)	IO_L39N_7	P24	I/O
7	N.C. (◆)	IO_L39P_7	P22	I/O
7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	P27	VREF
7	IO_L40P_7	IO_L40P_7	P26	I/O
7	VCCO_7	VCCO_7	P6	VCCO
7	VCCO_7	VCCO_7	P23	VCCO
N/A	GND	GND	P1	GND
N/A	GND	GND	P186	GND
N/A	GND	GND	P195	GND
N/A	GND	GND	P202	GND
N/A	GND	GND	P163	GND
N/A	GND	GND	P170	GND
N/A	GND	GND	P179	GND
N/A	GND	GND	P134	GND
N/A	GND	GND	P145	GND
N/A	GND	GND	P151	GND
N/A	GND	GND	P157	GND
N/A	GND	GND	P112	GND
N/A	GND	GND	P118	GND
N/A	GND	GND	P129	GND
N/A	GND	GND	P82	GND
N/A	GND	GND	P91	GND
N/A	GND	GND	P99	GND
N/A	GND	GND	P105	GND
N/A	GND	GND	P53	GND
N/A	GND	GND	P59	GND
N/A	GND	GND	P66	GND
N/A	GND	GND	P75	GND
N/A	GND	GND	P30	GND
N/A	GND	GND	P41	GND
N/A	GND	GND	P47	GND
N/A	GND	GND	P8	GND

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
N/A	GND	GND	B21	GND
N/A	GND	GND	C9	GND
N/A	GND	GND	C14	GND
N/A	GND	GND	J3	GND
N/A	GND	GND	J9	GND
N/A	GND	GND	J10	GND
N/A	GND	GND	J11	GND
N/A	GND	GND	J12	GND
N/A	GND	GND	J13	GND
N/A	GND	GND	J14	GND
N/A	GND	GND	J20	GND
N/A	GND	GND	K9	GND
N/A	GND	GND	K10	GND
N/A	GND	GND	K11	GND
N/A	GND	GND	K12	GND
N/A	GND	GND	K13	GND
N/A	GND	GND	K14	GND
N/A	GND	GND	L9	GND
N/A	GND	GND	L10	GND
N/A	GND	GND	L11	GND
N/A	GND	GND	L12	GND
N/A	GND	GND	L13	GND
N/A	GND	GND	L14	GND
N/A	GND	GND	M9	GND
N/A	GND	GND	M10	GND
N/A	GND	GND	M11	GND
N/A	GND	GND	M12	GND
N/A	GND	GND	M13	GND
N/A	GND	GND	M14	GND
N/A	GND	GND	N9	GND
N/A	GND	GND	N10	GND
N/A	GND	GND	N11	GND
N/A	GND	GND	N12	GND
N/A	GND	GND	N13	GND
N/A	GND	GND	N14	GND
N/A	GND	GND	P3	GND
N/A	GND	GND	P9	GND
N/A	GND	GND	P10	GND
N/A	GND	GND	P11	GND
N/A	GND	GND	P12	GND

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
0	IO_L09N_0	IO_L09N_0	IO_L09N_0	IO_L09N_0	IO_L09N_0	E7	I/O
0	IO_L09P_0	IO_L09P_0	IO_L09P_0	IO_L09P_0	IO_L09P_0	D7	I/O
0	IO_L10N_0	IO_L10N_0	IO_L10N_0	IO_L10N_0	IO_L10N_0	B7	I/O
0	IO_L10P_0	IO_L10P_0	IO_L10P_0	IO_L10P_0	IO_L10P_0	A7	I/O
0	N.C. (◆)	IO_L11N_0	IO_L11N_0	IO_L11N_0	IO_L11N_0	G8	I/O
0	N.C. (◆)	IO_L11P_0	IO_L11P_0	IO_L11P_0	IO_L11P_0	F8	I/O
0	N.C. (◆)	IO_L12N_0	IO_L12N_0	IO_L12N_0	IO(3)	E8	I/O
0	N.C. (◆)	IO_L12P_0	IO_L12P_0	IO_L12P_0	IO(3)	D8	I/O
0	IO_L15N_0	IO_L15N_0	IO_L15N_0	IO_L15N_0	IO_L13P_0(3)	B8	I/O
0	IO_L15P_0	IO_L15P_0	IO_L15P_0	IO_L15P_0	IO(3)	A8	I/O
0	IO_L16N_0	IO_L16N_0	IO_L16N_0	IO_L16N_0	IO_L16N_0	G9	I/O
0	IO_L16P_0	IO_L16P_0	IO_L16P_0	IO_L16P_0	IO_L16P_0	F9	I/O
0	N.C. (◆)	IO_L17N_0	IO_L17N_0	IO_L17N_0	IO_L17N_0	E9	I/O
0	N.C. (◆)	IO_L17P_0	IO_L17P_0	IO_L17P_0	IO_L17P_0	D9	I/O
0	N.C. (◆)	IO_L18N_0	IO_L18N_0	IO_L18N_0	IO_L18N_0	C9	I/O
0	N.C. (◆)	IO_L18P_0	IO_L18P_0	IO_L18P_0	IO_L18P_0	B9	I/O
0	IO_L19N_0	IO_L19N_0	IO_L19N_0	IO_L19N_0	IO_L19N_0	F10	I/O
0	IO_L19P_0	IO_L19P_0	IO_L19P_0	IO_L19P_0	IO_L19P_0	E10	I/O
0	IO_L22N_0	IO_L22N_0	IO_L22N_0	IO_L22N_0	IO_L22N_0	D10	I/O
0	IO_L22P_0	IO_L22P_0	IO_L22P_0	IO_L22P_0	IO_L22P_0	C10	I/O
0	N.C. (◆)	IO_L23N_0	IO_L23N_0	IO_L23N_0	IO_L23N_0	B10	I/O
0	N.C. (◆)	IO_L23P_0	IO_L23P_0	IO_L23P_0	IO_L23P_0	A10	I/O
0	IO_L24N_0	IO_L24N_0	IO_L24N_0	IO_L24N_0	IO_L24N_0	G11	I/O
0	IO_L24P_0	IO_L24P_0	IO_L24P_0	IO_L24P_0	IO_L24P_0	F11	I/O
0	IO_L25N_0	IO_L25N_0	IO_L25N_0	IO_L25N_0	IO_L25N_0	E11	I/O
0	IO_L25P_0	IO_L25P_0	IO_L25P_0	IO_L25P_0	IO_L25P_0	D11	I/O
0	N.C. (◆)	IO_L26N_0	IO_L26N_0	IO_L26N_0	IO_L26N_0	B11	I/O
0	N.C. (◆)	IO_L26P_0/VREF_0	IO_L26P_0/VREF_0	IO_L26P_0/VREF_0	IO_L26P_0/VREF_0	A11	VREF
0	IO_L27N_0	IO_L27N_0	IO_L27N_0	IO_L27N_0	IO_L27N_0	G12	I/O
0	IO_L27P_0	IO_L27P_0	IO_L27P_0	IO_L27P_0	IO_L27P_0	H13	I/O
0	IO_L28N_0	IO_L28N_0	IO_L28N_0	IO_L28N_0	IO_L28N_0	F12	I/O
0	IO_L28P_0	IO_L28P_0	IO_L28P_0	IO_L28P_0	IO_L28P_0	E12	I/O
0	IO_L29N_0	IO_L29N_0	IO_L29N_0	IO_L29N_0	IO_L29N_0	B12	I/O
0	IO_L29P_0	IO_L29P_0	IO_L29P_0	IO_L29P_0	IO_L29P_0	A12	I/O
0	IO_L30N_0	IO_L30N_0	IO_L30N_0	IO_L30N_0	IO_L30N_0	G13	I/O
0	IO_L30P_0	IO_L30P_0	IO_L30P_0	IO_L30P_0	IO_L30P_0	F13	I/O
0	IO_L31N_0	IO_L31N_0	IO_L31N_0	IO_L31N_0	IO_L31N_0	D13	I/O
0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	C13	VREF
0	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	B13	GCLK
0	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	A13	GCLK
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	C7	VCCO
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	C11	VCCO

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	U17	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	U18	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	V9	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	V10	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	V17	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	V18	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	W8	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	W19	VCCINT
VCC AUX	CCLK	CCLK	CCLK	CCLK	CCLK	AD26	CONFIG
VCC AUX	DONE	DONE	DONE	DONE	DONE	AC24	CONFIG
VCC AUX	HSWAP_EN	HSWAP_EN	HSWAP_EN	HSWAP_EN	HSWAP_EN	C2	CONFIG
VCC AUX	M0	M0	M0	M0	M0	AE3	CONFIG
VCC AUX	M1	M1	M1	M1	M1	AC3	CONFIG
VCC AUX	M2	M2	M2	M2	M2	AF3	CONFIG
VCC AUX	PROG_B	PROG_B	PROG_B	PROG_B	PROG_B	D3	CONFIG
VCC AUX	TCK	TCK	TCK	TCK	TCK	B24	JTAG
VCC AUX	TDI	TDI	TDI	TDI	TDI	C1	JTAG
VCC AUX	TDO	TDO	TDO	TDO	TDO	D24	JTAG
VCC AUX	TMS	TMS	TMS	TMS	TMS	A24	JTAG

Notes:
1. XC3S1500 balls D25 and F25 are not VREF pins although they are designated as such. If a design uses an IOSTANDARD requiring VREF in bank 2 then apply the workaround in Answer Record 20519.
2. XC3S4000 is pin compatible with XC3S2000 but uses alternate differential pair labeling on six package balls (H20, H21, H22, H23, H24, J21).
3. XC3S5000 is pin compatible with XC3S4000 but uses alternate differential pair functionality on fifteen package balls (A3, A8, B8, B18, C4, C8, C18, D8, D18, E8, E18, H23, H24, AB9, and AC9).

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
2	IO_L04N_2	IO_L04N_2	E29	I/O
2	IO_L04P_2	IO_L04P_2	E30	I/O
2	IO_L05N_2	IO_L05N_2	F28	I/O
2	IO_L05P_2	IO_L05P_2	F29	I/O
2	IO_L06N_2	IO_L06N_2	G27	I/O
2	IO_L06P_2	IO_L06P_2	G28	I/O
2	IO_L07N_2	IO_L07N_2	G29	I/O
2	IO_L07P_2	IO_L07P_2	G30	I/O
2	IO_L08N_2	IO_L08N_2	G25	I/O
2	IO_L08P_2	IO_L08P_2	H24	I/O
2	IO_L09N_2/VREF_2	IO_L09N_2/VREF_2	H25	VREF
2	IO_L09P_2	IO_L09P_2	H26	I/O
2	IO_L10N_2	IO_L10N_2	H27	I/O
2	IO_L10P_2	IO_L10P_2	H28	I/O
2	IO_L12N_2	IO_L12N_2	H29	I/O
2	IO_L12P_2	IO_L12P_2	H30	I/O
2	IO_L13N_2	IO_L13N_2	J26	I/O
2	IO_L13P_2/VREF_2	IO_L13P_2/VREF_2	J27	VREF
2	IO_L14N_2	IO_L14N_2	J29	I/O
2	IO_L14P_2	IO_L14P_2	J30	I/O
2	IO_L15N_2	IO_L15N_2	J23	I/O
2	IO_L15P_2	IO_L15P_2	K22	I/O
2	IO_L16N_2	IO_L16N_2	K24	I/O
2	IO_L16P_2	IO_L16P_2	K25	I/O
2	IO_L19N_2	IO_L19N_2	L25	I/O
2	IO_L19P_2	IO_L19P_2	L26	I/O
2	IO_L20N_2	IO_L20N_2	L27	I/O
2	IO_L20P_2	IO_L20P_2	L28	I/O
2	IO_L21N_2	IO_L21N_2	L29	I/O
2	IO_L21P_2	IO_L21P_2	L30	I/O
2	IO_L22N_2	IO_L22N_2	M22	I/O
2	IO_L22P_2	IO_L22P_2	M23	I/O
2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	M24	VREF
2	IO_L23P_2	IO_L23P_2	M25	I/O
2	IO_L24N_2	IO_L24N_2	M27	I/O
2	IO_L24P_2	IO_L24P_2	M28	I/O
2	IO_L26N_2	IO_L26N_2	M21	I/O
2	IO_L26P_2	IO_L26P_2	N21	I/O
2	IO_L27N_2	IO_L27N_2	N22	I/O
2	IO_L27P_2	IO_L27P_2	N23	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
0	IO_L23P_0	IO_L23P_0	J15	I/O
0	IO_L24N_0	IO_L24N_0	G15	I/O
0	IO_L24P_0	IO_L24P_0	F15	I/O
0	IO_L25N_0	IO_L25N_0	D15	I/O
0	IO_L25P_0	IO_L25P_0	C15	I/O
0	IO_L26N_0	IO_L26N_0	B15	I/O
0	IO_L26P_0/VREF_0	IO_L26P_0/VREF_0	A15	VREF
0	IO_L27N_0	IO_L27N_0	G16	I/O
0	IO_L27P_0	IO_L27P_0	F16	I/O
0	IO_L28N_0	IO_L28N_0	C16	I/O
0	IO_L28P_0	IO_L28P_0	B16	I/O
0	IO_L29N_0	IO_L29N_0	J17	I/O
0	IO_L29P_0	IO_L29P_0	H17	I/O
0	IO_L30N_0	IO_L30N_0	G17	I/O
0	IO_L30P_0	IO_L30P_0	F17	I/O
0	IO_L31N_0	IO_L31N_0	D17	I/O
0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	C17	VREF
0	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	B17	GCLK
0	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	A17	GCLK
0	N.C. (◆)	IO_L33N_0	D7	I/O
0	N.C. (◆)	IO_L33P_0	C7	I/O
0	N.C. (◆)	IO_L34N_0	B7	I/O
0	N.C. (◆)	IO_L34P_0	A7	I/O
0	IO_L35N_0	IO_L35N_0	E8	I/O
0	IO_L35P_0	IO_L35P_0	D8	I/O
0	IO_L36N_0	IO_L36N_0	B8	I/O
0	IO_L36P_0	IO_L36P_0	A8	I/O
0	IO_L37N_0	IO_L37N_0	D10	I/O
0	IO_L37P_0	IO_L37P_0	C10	I/O
0	IO_L38N_0	IO_L38N_0	B10	I/O
0	IO_L38P_0	IO_L38P_0	A10	I/O
0	N.C. (◆)	IO_L39N_0	G11	I/O
0	N.C. (◆)	IO_L39P_0	F11	I/O
0	N.C. (◆)	IO_L40N_0	B11	I/O
0	N.C. (◆)	IO_L40P_0	A11	I/O
0	VCCO_0	VCCO_0	B13	VCCO
0	VCCO_0	VCCO_0	C4	VCCO
0	VCCO_0	VCCO_0	C8	VCCO
0	VCCO_0	VCCO_0	D11	VCCO
0	VCCO_0	VCCO_0	D16	VCCO

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
0	VCCO_0	VCCO_0	F13	VCCO
0	VCCO_0	VCCO_0	G8	VCCO
0	VCCO_0	VCCO_0	H11	VCCO
0	VCCO_0	VCCO_0	H15	VCCO
0	VCCO_0	VCCO_0	M13	VCCO
0	VCCO_0	VCCO_0	M14	VCCO
0	VCCO_0	VCCO_0	M15	VCCO
0	VCCO_0	VCCO_0	M16	VCCO
1	IO	IO	B26	I/O
1	IO	IO	A18	I/O
1	IO	IO	C23	I/O
1	IO	IO	E21	I/O
1	IO	IO	E25	I/O
1	IO	IO	F18	I/O
1	IO	IO	F27	I/O
1	IO	IO	F29	I/O
1	IO	IO	H23	I/O
1	IO	IO	H26	I/O
1	N.C. (◆)	IO	J26	I/O
1	IO	IO	K19	I/O
1	IO	IO	L19	I/O
1	IO	IO	L20	I/O
1	IO	IO	L21	I/O
1	N.C. (◆)	IO	L23	I/O
1	IO	IO	L24	I/O
1	IO/VREF_1	IO/VREF_1	D30	VREF
1	IO/VREF_1	IO/VREF_1	K21	VREF
1	IO/VREF_1	IO/VREF_1	L18	VREF
1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	A32	DCI
1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	B32	DCI
1	IO_L02N_1	IO_L02N_1	A31	I/O
1	IO_L02P_1	IO_L02P_1	B31	I/O
1	IO_L03N_1	IO_L03N_1	B30	I/O
1	IO_L03P_1	IO_L03P_1	C30	I/O
1	IO_L04N_1	IO_L04N_1	C29	I/O
1	IO_L04P_1	IO_L04P_1	D29	I/O
1	IO_L05N_1	IO_L05N_1	A29	I/O
1	IO_L05P_1	IO_L05P_1	B29	I/O
1	IO_L06N_1/VREF_1	IO_L06N_1/VREF_1	E28	VREF
1	IO_L06P_1	IO_L06P_1	F28	I/O