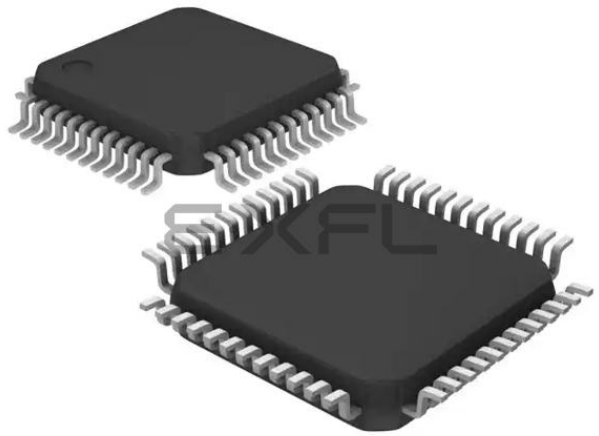

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, PWM, WDT
Number of I/O	35
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 2x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkv30f128vlf10p

- Implements Field Orient Control (FOC) using Back EMF to improve motor efficiency
- Utilizes SpinTAC control theory that improves overall system performance and reliability

Ordering Information

Part Number	Memory		Number of GPIOs
	Flash (KB)	SRAM (KB)	
MKV30F128VLH10	128	16	46
MKV30F128VLF10	128	16	35
MKV30F128VFM10	128	16	26
MKV30F64VLH10	64	16	46
MKV30F64VLF10	64	16	35
MKV30F64VFM10	64	16	26
MKV30F128VLF10P	120	16	35
MKV30F64VLH10P[1]	56	16	46
MKV30F64VLF10P[1]	56	16	35

1. This part number is subject to removal

Related Resources

Type	Description	Resource
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Product Selector
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	KV30FKV31FPB
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KV30P64M100SFARM
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	This document.
KMS User Guide	The KMS User Guide provides a comprehensive description of the features and functions of the Kinetis Motor Suite solution.	Kinetis Motor Suite User's Guide (KMS100UG)[1]
KMS API Reference Manual	The KMS API reference manual provides a comprehensive description of the API of the Kinetis Motor Suite function blocks.	Kinetis Motor Suite API Reference Manual (KMS100RM)[1]
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	Kinetis_V_0N36M
Package drawing	Package dimensions are provided by the part number: • MKV30F64VLF10P • MKV30F64VLH10P • MKV30F128VLH10 • MKV30F128VLF10 • MKV30F128VFM10 • MKV30F128VLF10P	• 98ASH00962A • 98ASS23234W • 98ASS23234W • 98ASH00962A • 98ARE10566D • 98ASH00962A

1. To find the associated resource, go to freescale.com and perform a search using Document ID

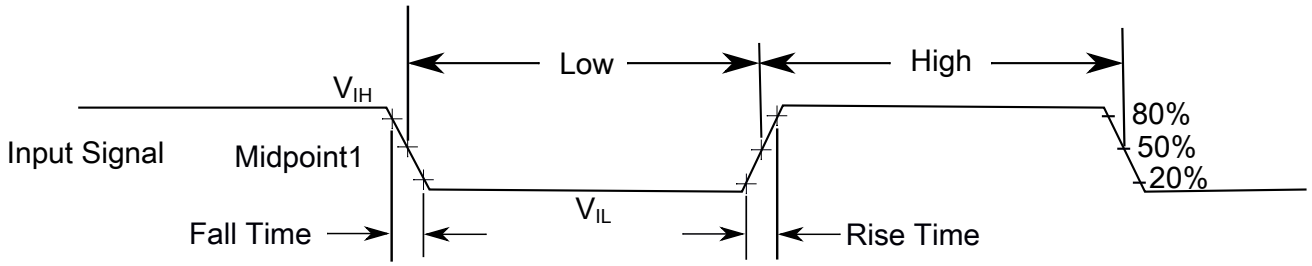
Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	145	mA
V_{DIO}	Digital input voltage	–0.3	V_{DD} + 0.3	V
V_{AIO}	Analog[1]	–0.3	V_{DD} + 0.3	V
I_D	Maximum current single pin limit (applies to all digital pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is V_{IL} + (V_{IH} - V_{IL}) / 2

Figure 2. Input signal measurement reference

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	

Table continues on the next page...

Table 1. Voltage and current operating requirements (continued)

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	0.7 × V_{DD} 0.75 × V_{DD}	— —	V V	
V_{IL}	Input low voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	— —	0.35 × V_{DD} 0.3 × V_{DD}	V V	
V_{HYS}	Input hysteresis	0.06 × V_{DD}	—	V	
I_{ICIO}	Analog and I/O pin DC injection current — single pin • V_{IN} < V_{SS}-0.3V (Negative current injection)	-3	—	mA	1
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins • Negative current injection	-25	—	mA	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	2
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	

1. All analog and I/O pins are internally clamped to V_{SS} through ESD protection diodes. If V_{IN} is less than V_{IO_MIN} or greater than V_{IO_MAX}, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{IO\_MIN}-V_{IN})/|I_{ICIO}|$.
2. Open drain outputs must be pulled to VDD.

2.2.2 LVD and POR operating requirements

Table 2. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	

Table continues on the next page...

Table 4. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• VLLS3 → RUN	—	—	75	µs	
	• VLPS → RUN	—	—	5.7	µs	
	• STOP → RUN	—	—	5.7	µs	

1. Normal boot (FTFA_OPT[LPBOOT]=1)

2.2.5 Power consumption operating behaviors

The current parameters in the table below are derived from code executing a while(1) loop from flash, unless otherwise noted.

The IDD typical values represent the statistical mean at 25°C, and the IDD maximum values for RUN, WAIT, VLPR, and VLPW represent data collected at 125°C junction temperature unless otherwise noted. The maximum values represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

Table 5. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_HSRUN}	High Speed Run mode current - all peripheral clocks disabled, CoreMark benchmark code executing from flash					
	@ 1.8V	—	18.70	19.37	mA	2, 3, 4
	@ 3.0V	—	18.71	19.38	mA	
I_{DD_HSRUN}	High Speed Run mode current - all peripheral clocks disabled, code executing from flash					
	@ 1.8V	—	18.13	18.80	mA	4
	@ 3.0V	—	18.19	18.86	mA	
I_{DD_HSRUN}	High Speed Run mode current — all peripheral clocks enabled, code executing from flash					
	@ 1.8V	—	22.2	22.87	mA	5
	@ 3.0V	—	22.4	23.07	mA	
I_{DD_RUN}	Run mode current in Compute operation — CoreMark benchmark code executing from flash					
	@ 1.8V	—	12.74	13.41	mA	2, 3, 6
	@ 3.0V	—	12.82	13.49	mA	

Table continues on the next page...

Table 5. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	@ 105°C	—	6.9	8.25	µA	

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. Cache on and prefetch on, low compiler optimization
3. CoreMark benchmark compiled using IAR 7.2 with optimization level low
4. 100 MHz core and system clock, 50 MHz bus clock, and 25 MHz flash clock. MCG configured for FEE mode. All peripheral clocks disabled.
5. 100 MHz core and system clock, 50 MHz bus clock, and 25 MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled.
6. 72 MHz core and system clock, 36 MHz bus clock and 24 MHz flash clock. MCG configured for FEE mode. All peripheral clocks disabled. Compute operation.
7. 72 MHz core and system clock, 36 MHz bus clock, and 24 MHz flash clock. MCG configured for FEI mode. All peripheral clocks disabled.
8. 72 MHz core and system clock, 36 MHz bus clock, and 24 MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled.
9. 72MHz core and system clock, 36MHz bus clock, and 24MHz flash clock. MCG configured for FEI mode. Compute operation.
10. 25 MHz core and system clock, 25 MHz bus clock, and 25 MHz flash clock. MCG configured for FEI mode.
11. 4 MHz core, system, and bus clock, and 1 MHz flash clock. MCG configured for BLPE mode. Compute operation. Code executing from flash.
12. 4 MHz core, system, and bus clock, and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
13. 4 MHz core, system, and bus clock, and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled, but peripherals are not in active operation. Code executing from flash.
14. 4 MHz core, system, and bus clock, and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.

Table 6. Low power mode peripheral adders—typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
$I_{IREFSTEN4MHz}$	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	56	µA
$I_{IREFSTEN32KHz}$	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	52	µA
$I_{EREFSTEN4MHz}$	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	228	237	245	251	258	uA
$I_{EREFSTEN32KHz}$	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.							
	VLLS1	440	490	540	560	570	580	nA
	VLLS3	440	490	540	560	570	580	
	LLS	490	490	540	560	570	680	

Table continues on the next page...

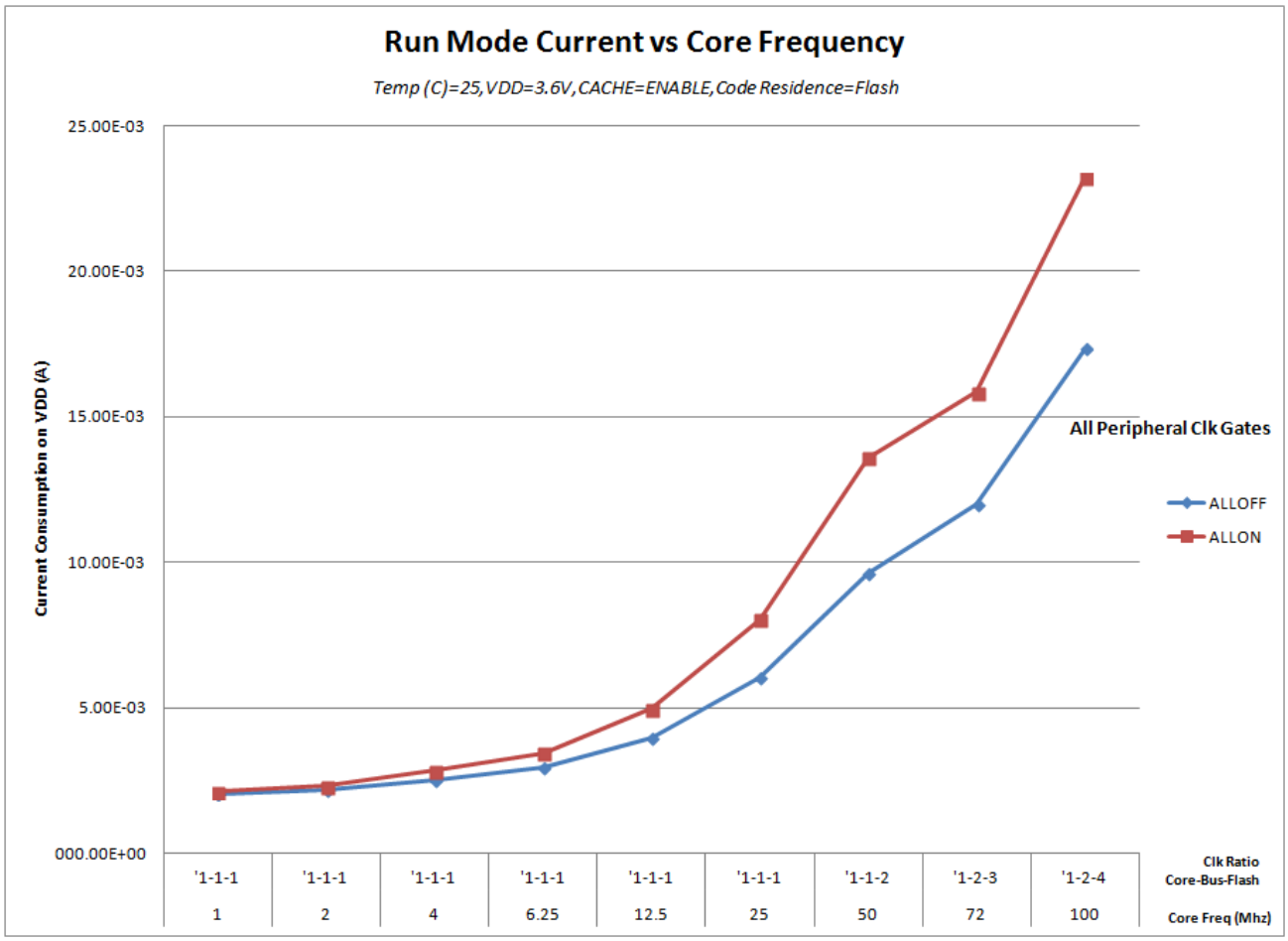


Figure 3. Run mode supply current vs. core frequency

2.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_J	Die junction temperature	–40	125	°C	
T_A	Ambient temperature	–40	105	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed maximum T_J. The simplest method to determine T_J is: $T_J = T_A + R_{\Theta JA} \times$ chip power dissipation.

2.4.2 Thermal attributes

Board type	Symbol	Description	64 LQFP	48 LQFP	32 QFN	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	66	79	97	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	48	55	33	°C/W	1
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	54	67	81	°C/W	1
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	41	49	28	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	30	33	13	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	17	23	2.0	°C/W	3

Table continues on the next page...

3.3.1 MCG specifications

Table 15. MCG specifications

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C		—	32.768	—	kHz	
Δf_{ints_t}	Total deviation of internal reference frequency (slow clock) over voltage and temperature		—	+0.5/-0.7	± 2	%	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed		31.25	—	39.0625	kHz	
$\Delta_{fdco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM		—	± 0.3	± 0.6	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature		—	+0.5/-0.7	± 2	$\%f_{dco}$	1, 2
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C		—	± 0.3	± 1.5	$\%f_{dco}$	1
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C		—	4	—	MHz	
Δf_{intf_ft}	Frequency deviation of internal reference clock (fast clock) over temperature and voltage — factory trimmed at nominal VDD and 25 °C		—	+1/-2	± 5	$\%f_{intf\_ft}$	
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C		3	—	5	MHz	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco}	DCO output frequency range	Low range (DRS=00) 640 × f_{fll_ref}	20	20.97	25	MHz	3, 4
		Mid range (DRS=01) 1280 × f_{fll_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f_{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f_{fll_ref}	80	83.89	100	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS=00) 732 × f_{fll_ref}	—	23.99	—	MHz	5, 6
		Mid range (DRS=01) 1464 × f_{fll_ref}	—	47.97	—	MHz	
		Mid-high range (DRS=10)	—	71.99	—	MHz	

Table continues on the next page...

Table 15. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
		$2197 \times f_{fll\_ref}$					
		High range (DRS=11) $2929 \times f_{fll\_ref}$	—	95.98	—	MHz	
J_{cyc_fll}	FLL period jitter • f_{VCO} = 48 MHz • f_{VCO} = 98 MHz		— —	— 180 150	— —	ps	
$t_{fll\_acquire}$	FLL target frequency acquisition time		—	—	1	ms	7

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. 2.0 V <= VDD <= 3.6 V.
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
4. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3.3.2 IRC48M specifications

Table 16. IRC48M specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DD48M}	Supply current	—	400	500	µA	
f_{irc48m}	Internal reference frequency	—	48	—	MHz	
Δf_{irc48m_hv}	Total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over full temperature	—	± 0.5	± 1.5	$\%f_{irc48m}$	
Δf_{irc48m_hv}	Total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over -40°C to 85°C	—	± 0.5	± 1.0	$\%f_{irc48m}$	
Δf_{irc48m_lv}	Total deviation of IRC48M frequency at low voltage (VDD=1.71V-1.89V) over full temperature	—	± 0.5	± 2.0	$\%f_{irc48m}$	
J_{cyc_irc48m}	Period Jitter (RMS)	—	35	150	ps	
$t_{irc48mst}$	Startup time	—	2	3	µs	1

1. IRC48M startup time is defined as the time between clock enablement and clock availability for system use. Enable the clock by one of the following settings:
   - MCG operating in an external clocking mode and MCG_C7[OSCSEL]=10 or MCG_C5[PLLCLKEN0]=1, or
   - SIM_SOPT2[PLLFLLSEL]=11

Table 17. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{pp}[5]	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x and C_y can be provided by using either integrated capacitors or external components.
4. When low-power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other device.

3.3.3.2 Oscillator frequency specifications

Table 18. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc\_hi\_1}$	Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	50	MHz	1, 2
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL

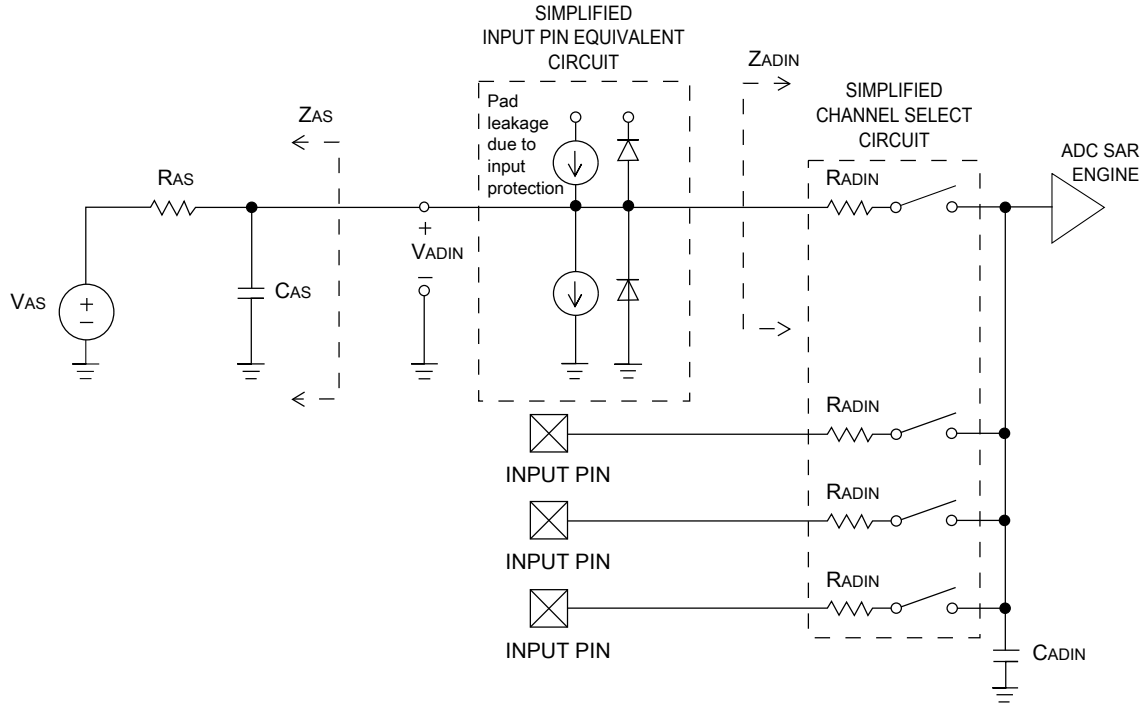


Figure 11. ADC input impedance equivalency diagram

3.6.1.2 16-bit ADC electrical characteristics

Table 24. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0	1.2	2.4	3.9	MHz	t_{ADACK} = 1/ f_{ADACK}
		• ADLPC = 1, ADHSC = 1	2.4	4.0	6.1	MHz	
		• ADLPC = 0, ADHSC = 0	3.0	5.2	7.3	MHz	
		• ADLPC = 0, ADHSC = 1	4.4	6.2	9.5	MHz	
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes	—	±4	±6.8	LSB[4]	5
		• <12-bit modes	—	±1.4	±2.1		
DNL	Differential non-linearity	• 12-bit modes	—	±0.7	–1.1 to +1.9	LSB[4]	5
		• <12-bit modes	—	±0.2	–0.3 to 0.5		
INL	Integral non-linearity	• 12-bit modes	—	±1.0	–2.7 to +1.9	LSB[4]	5

Table continues on the next page...

Table 24. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
		• <12-bit modes	—	±0.5	–0.7 to +0.5		
E_{FS}	Full-scale error	• 12-bit modes • <12-bit modes	— —	–4 –1.4	–5.4 –1.8	LSB[4]	V_{ADIN} = V_{DDA}[5]
E_Q	Quantization error	• 16-bit modes • ≤13-bit modes	— —	–1 to 0 —	— ±0.5	LSB[4]	
ENOB	Effective number of bits	16-bit differential mode • Avg = 32 • Avg = 4 16-bit single-ended mode • Avg = 32 • Avg = 4	 12.8 11.9 12.2 11.4	 14.5 13.8 13.9 13.1	 — — — —	 bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	 — —	 -94 -85	 — —	dB dB	7
SFDR	Spurious free dynamic range	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	 82 78	 95 90	 — —	dB dB	7
E_{IL}	Input leakage error		I_{In} × R_{AS}			mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

1. All accuracy numbers assume the ADC is calibrated with V_{REFH} = V_{DDA}
2. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.

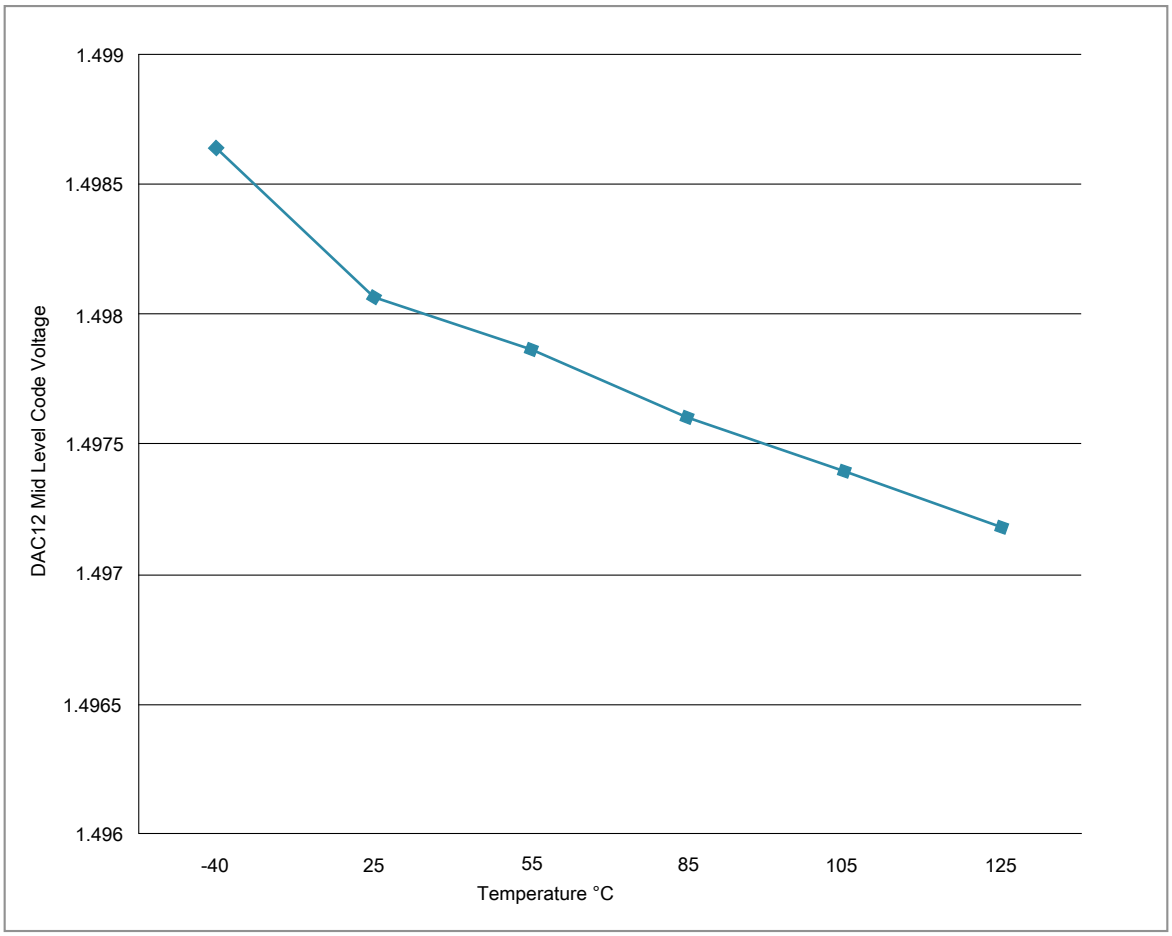


Figure 17. Offset at half scale vs. temperature

3.6.4 Voltage reference electrical specifications

Table 28. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
T_A	Temperature	Operating temperature range of the device		°C	
C_L	Output load capacitance	100		nF	1, 2

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

Table 29. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim at nominal V_{DDA} and temperature=25°C	1.1920	1.1950	1.1980	V	1
V_{out}	Voltage reference output with user trim at nominal V_{DDA} and temperature=25°C	1.1945	1.1950	1.1955	V	1
V_{step}	Voltage reference trim step	—	0.5	—	mV	1
V_{tdrift}	Temperature drift (Vmax -Vmin across the full temperature range)	—	—	15	mV	1
I_{bg}	Bandgap only current	—	—	80	µA	
I_{lp}	Low-power buffer current	—	—	360	uA	1
I_{hp}	High-power buffer current	—	—	1	mA	1
ΔV_{LOAD}	Load regulation • current = ± 1.0 mA	— 	200 	— 	µV 	1, 2
T_{stup}	Buffer startup time	—	—	100	µs	
$T_{chop\_osc\_startup}$	Internal bandgap start-up delay with chop oscillator enabled	—	—	35	ms	
V_{vdrift}	Voltage drift (Vmax -Vmin across the full voltage range)	—	2	—	mV	1

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

Table 30. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_A	Temperature	0	70	°C	

Table 31. VREF limited-range operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{tdrift}	Temperature drift (V_{max} -V_{min} across the limited temperature range)	—	10	mV	

3.7 Timers

See General switching specifications.

3.8 Communication interfaces

3.8.1 DSPI switching specifications (limited voltage range)

The Deserial Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the SPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 32. Master mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	25	MHz	
DS1	DSPI_SCK output cycle time	2 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) – 2	—	ns	1
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) – 2	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	16.2	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

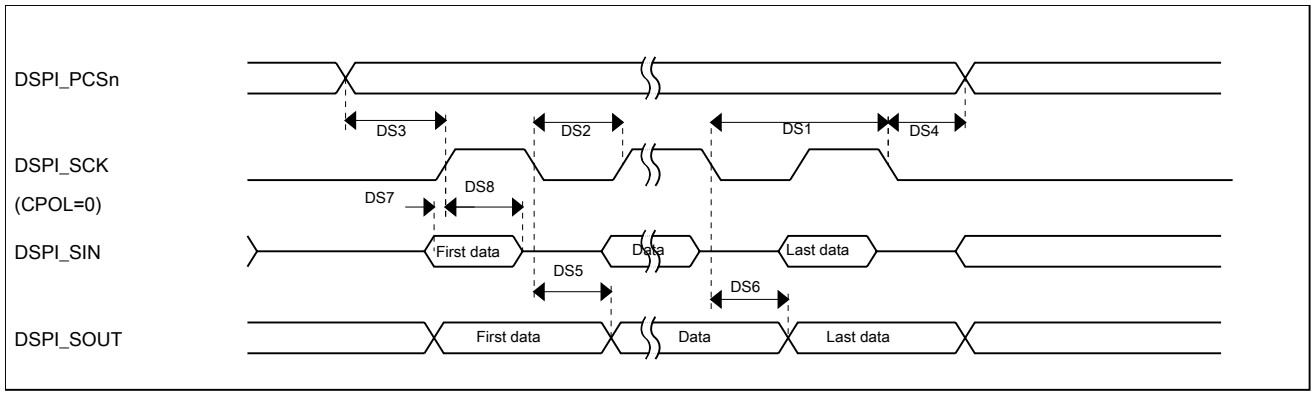


Figure 18. DSPI classic SPI timing — master mode

Table 33. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	12.5	MHz	1
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns	
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns	
DS11	DSPI_SCK to DSPI_SOUT valid	—	21.4	ns	
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns	
DS13	DSPI_SIN to DSPI_SCK input setup	2.6	—	ns	
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns	
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	17	ns	
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	17	ns	

1. The maximum operating frequency is measured with noncontinuous CS and SCK. When DSPI is configured with continuous CS and SCK, the SPI clock must not be greater than 1/6 of the bus clock. For example, when the bus clock is 60 MHz, the SPI clock must not be greater than 10 MHz.

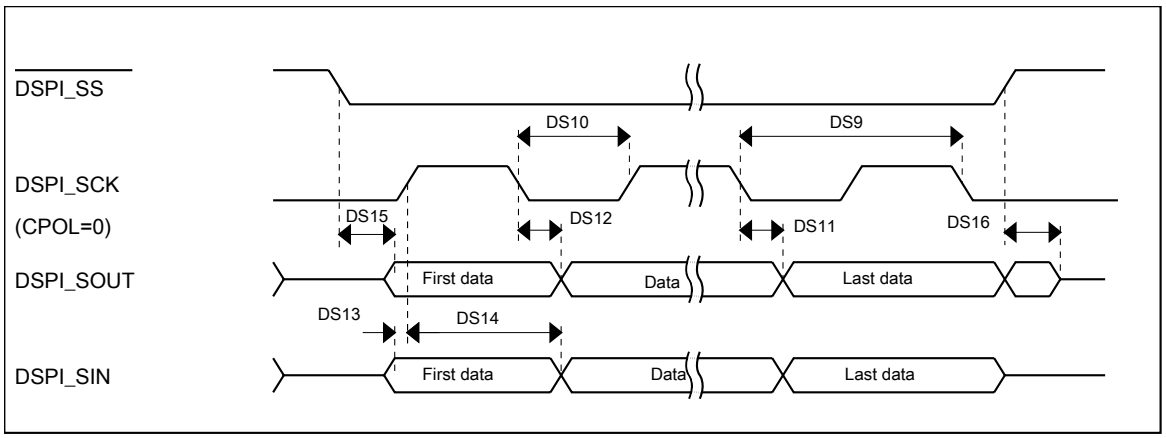


Figure 19. DSPI classic SPI timing — slave mode

3.8.2 DSPI switching specifications (full voltage range)

The Deserial Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the SPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 34. Master mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	12.5	MHz	
DS1	DSPI_SCK output cycle time	4 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) - 4	($t_{SCK/2)}$ + 4	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) – 4	—	ns	2
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) – 4	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-4.5	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	24.6	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

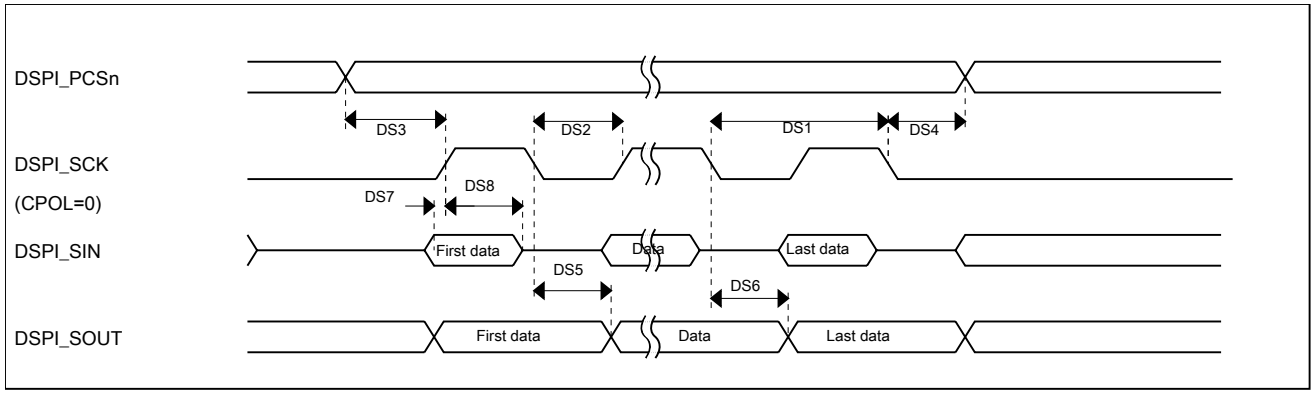


Figure 20. DSPI classic SPI timing — master mode

Table 36. I²C timing (continued)

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
Data hold time for I²C bus devices	t_{HD}; DAT	0[2]	3.45[3]	0[4]	0.9[2]	µs
Data set-up time	t_{SU}; DAT	250[5]	—	100[3, 6]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[7]	300	ns
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b[6]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can only be achieved when using the High drive pins across the full voltage range and when using the Normal drive pins and VDD ≥ 2.7 V.
2. The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
3. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
4. Input signal Slew = 10 ns and Output Load = 50 pF
5. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
6. A Fast mode I²C bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU;\ DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT} = 1000 + 250 = 1250$ ns (according to the Standard mode I²C bus specification) before the SCL line is released.
7. C_b = total capacitance of the one bus line in pF.

Table 37. I²C 1 Mbps timing

Characteristic	Symbol	Minimum	Maximum	Unit
SCL Clock Frequency	f_{SCL}	0	1[1]	MHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	0.26	—	µs
LOW period of the SCL clock	t_{LOW}	0.5	—	µs
HIGH period of the SCL clock	t_{HIGH}	0.26	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	0.26	—	µs
Data hold time for I_2C bus devices	t_{HD}; DAT	0	—	µs
Data set-up time	t_{SU}; DAT	50	—	ns
Rise time of SDA and SCL signals	t_r	20 +0.1C_b,[2]	120	ns
Fall time of SDA and SCL signals	t_f	20 +0.1C_b[2]	120	ns
Set-up time for STOP condition	t_{SU}; STO	0.26	—	µs
Bus free time between STOP and START condition	t_{BUF}	0.5	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	0	50	ns

1. The maximum SCL clock frequency of 1 Mbps can support maximum bus loading when using the High drive pins across the full voltage range.
2. C_b = total capacitance of the one bus line in pF.

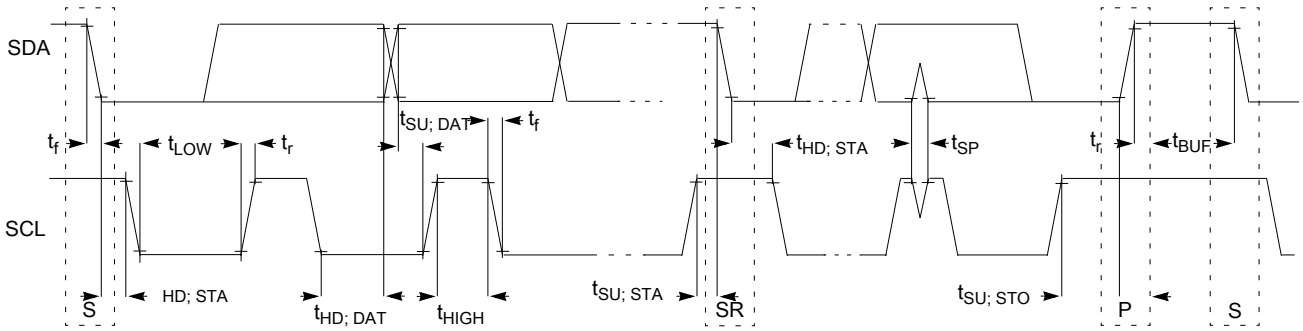


Figure 22. Timing definition for devices on the I²C bus

3.8.4 UART switching specifications

See General switching specifications.

3.9 Kinetis Motor Suite

Kinetis Motor Suite is a bundled software solution that enables the rapid configuration of motor drive systems, and accelerates development of the final motor drive application.

Several members of the KV3x family are enabled with Kinetis motor suite. The enabled devices can be identified within the orderable part numbers in this table. For more information refer to Kinetis Motor Suite User's Guide (KMS100UG) and Kinetis Motor Suite API Reference Manual (KMS100RM).

NOTE

To find the associated resource, go to freescale.com and perform a search using Document ID.

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

Table 39. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• In "Slave mode DSPI timing (limited voltage range)" table, added footnote regarding maximum frequency of operation • Added new section, "Recommended connections for unused analog and digital pins" • Added Terminology and Guidelines section • Updated Thermal Attributes value for 48LQFP • Added KMS related information in front matter • Added Kinetis Motor Suite section • Added "S" in Format and Part Identification table • Updated the Part Number Example • Deleted Package Your Way footnote attached to 48 LQFP

3	4/2015	• Throughout: Modified notes related to 48-pin LQFP to say, "The 48-pin LQFP package for this product is not yet available; however, it is included in a Package Your Way program for Kinetis MCUs. Please visit www.Freescale.com/KPYW for more details."
		• On page 1:
		  • Under "Clocks," corrected second and third bullets—moved "with FLL" from "internal oscillators" to "multipurpose clock generator" bullet
		  • Under "Communication interfaces," updated I^2C bullet to indicate support for up to 1 Mbps operation
		  • Under "Operating characteristics," specified that voltage range includes flash writes
		• In "Voltage and current operating requirements" table:
		  • Removed content related to positive injection
		  • Updated footnote 1 to say that all analog and I/O pins are internally clamped to V_{SS} only (not V_{SS} and V_{DD})through ESD protection diodes.
		• In "Power mode transition operating behaviors" table, removed rows for LLS2 and LLS3
		• In "Power consumption operating behaviors" table:
		  • Provided additional temperature data
		  • Added Max IDD values based on characterization results equivalent to mean + 3 sigma
		  • Removed rows for LLS2 and LLS3
		• Updated "EMC radiated emissions operating behaviors" table
		• In "Thermal operating requirements" table, added the following footnote for ambient temperature: "Maximum T_A can be exceeded only if the user ensures that T_J does not exceed maximum T_J. The simplest method to determine T_J is: $T_J = T_A + \Theta_{JA}$ x chip power dissipation"
		• Updated "IRC48M Specifications":
		  • Updated maximum values for $\Delta_{firc48m\_lv}$ and $\Delta_{firc48m\_hv}$ (full temperature)
		  • Added specifications for $\Delta_{firc48m\_hv}$ (-40°C to 85°C)
		• In "I^2C timing" table,
		  • Added the following footnote on maximum Fast mode value for SCL Clock Frequency: "The maximum SCL Clock Frequency in Fast mode with maximum bus loading can only be achieved when using the High drive pins across the full voltage range and when using the Normal drive pins and VDD ≥ 2.7 V."
		  • Updated minimum Fast mode value for LOW period of the SCL clock to 1.25 µ
		• Added "I^2C 1 Mbps timing" table
		• Removed Section 6, "Ordering parts."
		• Added "48-pin LQFP part marking" section
		• Added "32-pin QFN part marking" section

2	8/2014	• On p. 1, under "Memories and memory interfaces," added bullet, "Preprogrammed Kinetis flashloader for one-time, in-system factory programming"

Table continues on the next page...