



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	DMA, PWM, WDT
Number of I/O	26
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 2x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount, Wettable Flank
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-HVQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkv30f64vfm10

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1 Ratings

1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	-55	150	°C	1
T _{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, High Temperature Storage Life.

2. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	_	3	_	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I _{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.

2. Determined according to JEDEC Standard JESD22-C101, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components.

3. Determined according to JEDEC Standard JESD78, IC Latch-Up Test.

1.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V _{DD}	Digital supply voltage	-0.3	3.8	V
I _{DD}	Digital supply current		145	mA
V _{DIO}	Digital input voltage	-0.3	V _{DD} + 0.3	V
V _{AIO}	Analog ¹	-0.3	V _{DD} + 0.3	V
I _D	Maximum current single pin limit (applies to all digital pins)	-25	25	mA
V _{DDA}	Analog supply voltage	V _{DD} – 0.3	V _{DD} + 0.3	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.





2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

 Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V _{DD}	Supply voltage	1.71	3.6	V	

Table continues on the next page...

Symbol	Description	Min.	Max.	Unit	Notes
V _{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	V _{DD} -to-V _{DDA} differential voltage	-0.1	0.1	V	
$V_{SS} - V_{SSA}$	V _{SS} -to-V _{SSA} differential voltage	-0.1	0.1	V	
V _{IH}	Input high voltage	$0.7 \times V_{DD}$	_	V	
	• 2.7 V \leq V _{DD} \leq 3.6 V	$0.75 \times V_{DD}$	—	V	
	• $1.7 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}$				
V _{IL}	Input low voltage		$0.35 \times V_{DD}$	V	
	• 2.7 V \leq V _{DD} \leq 3.6 V	—	$0.3 \times V_{DD}$	V	
	• $1.7 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}$				
V _{HYS}	Input hysteresis	$0.06 \times V_{DD}$		V	
I _{ICIO}	Analog and I/O pin DC injection current — single pin				1
	 V_{IN} < V_{SS}-0.3V (Negative current injection) 	-3	—	mA	
I _{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins	-25	_	mA	
	Negative current injection				
V _{ODPU}	Open drain pullup voltage level	V _{DD}	V _{DD}	V	2
V _{RAM}	V _{DD} voltage required to retain RAM	1.2	—	V	

Table 1. Voltage and current operating requirements (continued)

 All analog and I/O pins are internally clamped to V_{SS} through ESD protection diodes. If V_{IN} is less than V_{IO_MIN} or greater than V_{IO_MAX}, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R=(V_{IO_MIN}-V_{IN})/II_{ICIO}I.

2. Open drain outputs must be pulled to VDD.

2.2.2 LVD and POR operating requirements

Table 2. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V _{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V _{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V _{LVW1H}	Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V _{LVW2H}	Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V _{LVW3H}	 Level 3 falling (LVWV=10) 	2.82	2.90	2.98	V	
V _{LVW4H}	Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	

Table continues on the next page ...

7

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
	$2.7 \text{ V} \le \text{V}_{\text{DD}} \le 3.6 \text{ V}, \text{ I}_{\text{OL}} = 3 \text{ mA}$	—	_	0.5	V	
	$1.71 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}, \text{ I}_{\text{OL}} = 1.5 \text{ mA}$	_	—	0.5	V	
I _{OLT}	Output low current total for all ports	—	—	100	mA	
I _{IN}	Input leakage current (per pin) for full temperature range					
	All pins other than high drive port pins	_	0.002	0.5	μA	1, 2
	High drive port pins	_	0.004	0.5	μA	
I _{IN}	Input leakage current (total all pins) for full temperature range		_	1.0	μA	2
R _{PU}	Internal pullup resistors	20	—	50	kΩ	3
R _{PD}	Internal pulldown resistors	20	_	50	kΩ	4

Table 3. Voltage and current operating behaviors (continued)

1. PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, and PTD7 I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.

2. Measured at VDD=3.6V

3. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}

4. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{DD}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} , and VLLSx \rightarrow RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 72 MHz
- Bus clock = 36 MHz
- Flash clock = 24 MHz
- MCG mode: FEI

Table 4. Power mode transition operating behaviors

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
t _{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	_	_	300	μs	1
	• VLLS0 \rightarrow RUN	_	_	135	μs	
	• VLLS1 → RUN	_	_	135	μs	
	• VLLS2 → RUN			75	μs	

Table continues on the next page...

9

Table 5.	Power consum	otion operating	behaviors	(continued)
				(••••••••••••••••••••••••••••••••••••••

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	0.76	1.04	mA	13
I _{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	—	0.28	0.56	mA	14
I _{DD_STOP}	Stop mode current at 3.0 V					
	@ -40°C to 25°C	—	0.26	0.33	mA	
	@ 70°C	—	0.30	0.47	mA	
	@ 85°C	—	0.35	0.52	mA	
	@ 105°C	—	0.43	0.60	mA	
I _{DD_VLPS}	Very-low-power stop mode current at 3.0 V					
	@ -40°C to 25°C	—	2.80	8.30	μA	
	@ 70°C	—	13.30	29.90	μA	
	@ 85°C	_	26.90	46.45	μA	
	@ 105°C		56.80	67.05	μA	
I _{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V					
	@ -40°C to 25°C	_	1.3	1.71	μA	
	@ 70°C	_	3.8	5.35	μA	
	@ 85°C	_	7.6	8.50	μA	
	@ 105°C	—	15.1	19.05	μA	
I _{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V					
	@ -40°C to 25°C	_	1.3	1.55	μA	
	@ 70°C	_	3.1	4.05	μΑ	
	@ 85°C	_	7.2	8.60	μA	
	@ 105°C	—	12.0	14.10	μA	
I _{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V					
	@ -40°C to 25°C	_	0.63	0.87	μΑ	
	@ 70°C	_	1.70	2.35	μΑ	
	@ 85°C	_	2.8	3.40	μΑ	
	@ 105°C	—	7.6	8.80	μA	
I _{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled					
	@ -40°C to 25°C	_	0.35	0.46	μA	
	@ 70°C	_	1.38	1.94	μA	
	@ 85°C	_	2.4	2.95	μA	
	@ 105°C		7.3	8.45	μA	
I _{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled					
	@ -40°C to 25°C	—	0.07	0.16	μA	
	@ 70°C	—	1.05	1.78	μA	
	@ 85°C	_	2.1	2.80	μA	

Table continues on the next page ...

General



Figure 4. VLPR mode supply current vs. core frequency

2.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors for 64 LQFP package

Parame ter	Conditions	Clocks	Frequency range	Level (Typ.)	Unit	Notes
V _{EME}	Device configuration, test	FSYS = 100 MHz	150 kHz–50 MHz	11	dBuV	1, 2, 3
	conditions and EM	FBUS = 50 MHz	50 MHz–150 MHz	12		
	61967-2.	External crystal = 10 MHz	150 MHz–500 MHz	11		
	Supply voltage: VDD =		500 MHz–1000 MHz	8		
	3.3 V		IEC level	Ν		4
	Temp = 25°C					

1. Measurements were made per IEC 61967-2 while the device was running typical application code.

- 2. Measurements were performed on the 64LQFP device, MKV30F128VLH10.
- 3. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

Symbol	Description		Max.	Unit	Notes
f _{LPTMR_pin}	LPTMR clock	—	25	MHz	
f _{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz	

Table 9.	Device clock s	pecifications	(continued)
1 4510 01		poolinoutiono	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and timers.

 Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	External RESET and NMI pin interrupt pulse width — Asynchronous path	100	_	ns	3
	GPIO pin interrupt pulse width (digital glitch filter disabled, passive filter disabled) — Asynchronous path	50	_	ns	4
	Port rise and fall time				5
	Slew disabled	—			
	• $1.71 \le V_{DD} \le 2.7V$	—	10	ns	
	• $2.7 \le V_{DD} \le 3.6V$		5	ns	
	Slew enabled	—			
	• $1.71 \le V_{DD} \le 2.7V$	—	30	ns	
	• $2.7 \le V_{DD} \le 3.6V$		16	ns	

- 1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
- 2. The greater of synchronous and asynchronous timing must be met.
- 3. These pins have a passive filter enabled on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
- 4. These pins do not have a passive filter on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
- 5. 25 pF load

2.4 Thermal specifications

Symbol	Description	Min.	Max.	Unit
	Boundary Scan	50	—	ns
	JTAG and CJTAG	25	—	ns
J4	TCLK rise and fall times	_	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	1	—	ns
J7	TCLK low to boundary scan output data valid	_	25	ns
J8	TCLK low to boundary scan output high-Z	_	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	TCLK low to TDO data valid	_	19	ns
J12	TCLK low to TDO high-Z	_	19	ns
J13	TRST assert time	100	—	ns
J14	TRST setup time (negation) to TCLK high	8	—	ns

Table 13. JTAG limited voltage range electricals (continued)

Table 14. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation			MHz
	Boundary Scan	0	10	
	JTAG and CJTAG	0	15	
J2	TCLK cycle period	1/J1	_	ns
J3	TCLK clock pulse width			
	Boundary Scan	50	_	ns
	JTAG and CJTAG	33	_	ns
J4	TCLK rise and fall times	_	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	_	ns
J6	Boundary scan input data hold time after TCLK rise	1.4	—	ns
J7	TCLK low to boundary scan output data valid	_	27	ns
J8	TCLK low to boundary scan output high-Z	_	27	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.4	—	ns
J11	TCLK low to TDO data valid	_	26.2	ns
J12	TCLK low to TDO high-Z		26.2	ns
J13	TRST assert time	100	_	ns
J14	TRST setup time (negation) to TCLK high	8	—	ns

3.3.3 Oscillator electrical specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V _{DD}	Supply voltage	1.71	_	3.6	V	
IDDOSC	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	_	200	_	μA	
	• 8 MHz (RANGE=01)		300	_	μA	
	• 16 MHz	_	950	_	μA	
	• 24 MHz	_	1.2	_	mA	
	• 32 MHz	_	1.5	_	mA	
IDDOSC	Supply current — high-gain mode (HGO=1)					1
	• 32 kHz	—	25	_	μA	
	• 4 MHz	_	400	_	μA	
	• 8 MHz (RANGE=01)	_	500	_	μA	
	• 16 MHz	_	2.5	_	mA	
	• 24 MHz	—	3	_	mA	
	• 32 MHz	—	4	_	mA	
C _x	EXTAL load capacitance					2, 3
Cy	XTAL load capacitance	_	_	—		2, 3
R _F	Feedback resistor — low-frequency, low-power mode (HGO=0)	_	_	_	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	_	10		MΩ	
	Feedback resistor — high-frequency, low- power mode (HGO=0)	_	_		MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	_	1		MΩ	
R _S	Series resistor — low-frequency, low-power mode (HGO=0)		_		kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	_	200		kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)				kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)					
		_	0	_	kΩ	

3.3.3.1 Oscillator DC electrical specifications Table 17. Oscillator DC electrical specifications

Table continues on the next page...

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V _{pp} ⁵	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	_	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	_	V _{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	_	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V _{DD}	_	V	

 Table 17. Oscillator DC electrical specifications (continued)

1. V_{DD} =3.3 V, Temperature =25 °C

2. See crystal or resonator manufacturer's recommendation

3. C_x and C_y can be provided by using either integrated capacitors or external components.

4. When low-power mode is selected, R_F is integrated and must not be attached externally.

5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other device.

3.3.3.2 Oscillator frequency specifications

Table 18. Oscillator frequency specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
f _{osc_lo}	Oscillator crystal or resonator frequency — low- frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
f _{osc_hi_1}	Oscillator crystal or resonator frequency — high- frequency mode (low range) (MCG_C2[RANGE]=01)	3	_	8	MHz	
f _{osc_hi_2}	_2 Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)		_	32	MHz	
f _{ec_extal}	Input clock frequency (external clock mode)	_	_	50	MHz	1, 2
t _{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t _{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	_	750	_	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	_	0.6	_	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	_	1	_	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL

2. Maximum times for erase parameters based on expectations at cycling end-of-life.

3.4.1.3 Flash high voltage current behaviors Table 21. Flash high voltage current behaviors

Symbol	Description	Min.	Тур.	Max.	Unit
I _{DD_PGM}	Average current adder during high voltage flash programming operation		2.5	6.0	mA
I _{DD_ERS}	Average current adder during high voltage flash erase operation		1.5	4.0	mA

3.4.1.4 Reliability specifications Table 22. NVM reliability specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
	Program	n Flash				
t _{nvmretp10k}	Data retention after up to 10 K cycles	5	50	_	years	—
t _{nvmretp1k}	Data retention after up to 1 K cycles	20	100		years	—
n _{nvmcycp}	Cycling endurance	10 K	50 K	_	cycles	2

 Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.

2. Cycling endurance represents number of program/erase cycles at -40 °C \leq T_i \leq 125 °C.

3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

3.6 Analog

3.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 23 and Table 24 are achievable on the differential pins ADCx_DPx, ADCx_DMx.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V _{DDA}	Supply voltage	Absolute	1.71	_	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V _{DD} (V _{DD} – V _{DDA})	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$)	-100	0	+100	mV	2
V _{REFH}	ADC reference voltage high		1.13	V _{DDA}	V _{DDA}	V	
V _{REFL}	ADC reference voltage low		V _{SSA}	V _{SSA}	V _{SSA}	V	
V _{ADIN}	Input voltage	16-bit differential mode	VREFL	_	31/32 * VREFH	V	
		All other modes	VREFL	—	VREFH		
C _{ADIN}	Input	16-bit mode		8	10	pF	
	capacitance	 8-bit / 10-bit / 12-bit modes 	_	4	5		
R _{ADIN}	Input series resistance			2	5	kΩ	
R _{AS}	Analog source resistance (external)	13-bit / 12-bit modes f _{ADCK} < 4 MHz	_	_	5	kΩ	3
f _{ADCK}	ADC conversion clock frequency	≤ 13-bit mode	1.0		24.0	MHz	4
f _{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	_	12.0	MHz	4
C _{rate}	ADC conversion	≤ 13-bit modes					5
	rate	No ADC hardware averaging	20	_	1200	Ksps	
		Continuous conversions enabled, subsequent conversion time					
C _{rate}	ADC conversion	16-bit mode					5
	rate	No ADC hardware averaging	37	—	461	Ksps	
		Continuous conversions enabled, subsequent conversion time					

3.6.1.1 16-bit ADC operating conditions Table 23. 16-bit ADC operating conditions

- 1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
- 2. DC potential difference.
- 3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
- 4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
- 5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.

3.6.3.2 12-bit DAC operating behaviors Table 27. 12-bit DAC operating behaviors

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I _{DDA_DACL}	Supply current — low-power mode	_	—	330	μΑ	
I _{DDA_DACH}	Supply current — high-speed mode	_	—	1200	μΑ	
t _{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	μs	1
tDACHP	Full-scale settling time (0x080 to 0xF7F) — high-power mode	_	15	30	μs	1
t _{CCDACLP}	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	_	0.7	1	μs	1
V _{dacoutl}	DAC output voltage range low — high- speed mode, no load, DAC set to 0x000		—	100	mV	
V _{dacouth}	DAC output voltage range high — high- speed mode, no load, DAC set to 0xFFF	V _{DACR} -100	_	V _{DACR}	mV	
INL	Integral non-linearity error — high speed mode		_	±8	LSB	2
DNL	Differential non-linearity error — V _{DACR} > 2 V		_	±1	LSB	3
DNL	Differential non-linearity error — V _{DACR} = VREF_OUT	_	_	±1	LSB	4
VOFFSET	Offset error	_	±0.4	±0.8	%FSR	5
E _G	Gain error	_	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, $V_{DDA} \ge 2.4 V$	60	—	90	dB	
T _{CO}	Temperature coefficient offset voltage	_	3.7	_	μV/C	6
T _{GE}	Temperature coefficient gain error	_	0.000421		%FSR/C	
Rop	Output resistance (load = $3 \text{ k}\Omega$)	_	—	250	Ω	
SR	Slew rate -80h \rightarrow F7Fh \rightarrow 80h				V/µs	
	 High power (SP_{HP}) 	1.2	1.7	—		
	• Low power (SP _{LP})	0.05	0.12	—		
BW	3dB bandwidth				kHz	
	 High power (SP_{HP}) 	550	_	—		
	 Low power (SP_{LP}) 	40	_	—		

1. Settling within ±1 LSB

2. The INL is measured for 0 + 100 mV to V_{DACR} –100 mV

3. The DNL is measured for 0 + 100 mV to V_{DACR} –100 mV

4. The DNL is measured for 0 + 100 mV to V_{DACR} –100 mV with V_{DDA} > 2.4 V 5. Calculated by a best fit curve from V_{SS} + 100 mV to V_{DACR} – 100 mV

6. V_{DDA} = 3.0 V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_CO:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

38



Figure 16. Typical INL error vs. digital code

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V _{out}	Voltage reference output with factory trim at nominal V _{DDA} and temperature=25°C	1.1920	1.1950	1.1980	V	1
V _{out}	Voltage reference output with user trim at nominal V _{DDA} and temperature=25°C	1.1945	1.1950	1.1955	V	1
V _{step}	Voltage reference trim step	—	0.5	—	mV	1
V _{tdrift}	Temperature drift (Vmax -Vmin across the full temperature range)	_		15	mV	1
I _{bg}	Bandgap only current	—	—	80	μA	
I _{lp}	Low-power buffer current	—	_	360	uA	1
I _{hp}	High-power buffer current	—	—	1	mA	1
ΔV_{LOAD}	Load regulation				μV	1, 2
	• current = ± 1.0 mA	_	200	_		
T _{stup}	Buffer startup time	—	_	100	μs	
T _{chop_osc_st}	chop_osc_st up Internal bandgap start-up delay with chop oscillator enabled		—	35	ms	
V _{vdrift}	Voltage drift (Vmax -Vmin across the full voltage range)	_	2	_	mV	1

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.

2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

Table 30. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T _A	Temperature	0	70	°C	

Table 31. VREF limited-range operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V _{tdrift}	Temperature drift (V _{max} -V _{min} across the limited temperature range)	_	10	mV	

3.7 Timers

See General switching specifications.

3.8 Communication interfaces

3.8.1 DSPI switching specifications (limited voltage range)

The Deserial Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the SPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	25	MHz	
DS1	DSPI_SCK output cycle time	2 x t _{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t _{SCK} /2) – 2	(t _{SCK} /2) + 2	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	(t _{BUS} x 2) – 2	_	ns	1
DS4	DSPI_SCK to DSPI_PCSn invalid delay	(t _{BUS} x 2) – 2	_	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	16.2	_	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	_	ns	

Table 32. Master mode DSPI timing (limited voltage range)

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].

2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].



Figure 18. DSPI classic SPI timing — master mode

3.8.2 DSPI switching specifications (full voltage range)

The Deserial Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the SPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	12.5	MHz	
DS1	DSPI_SCK output cycle time	4 x t _{BUS}	_	ns	
DS2	DSPI_SCK output high/low time	(t _{SCK} /2) - 4	(t _{SCK/2)} + 4	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	(t _{BUS} x 2) – 4	—	ns	2
DS4	DSPI_SCK to DSPI_PCSn invalid delay	(t _{BUS} x 2) – 4	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-4.5	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	24.6	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

Table 34.	Master mode	DSPI timing	(full	voltage	range)
-----------	-------------	--------------------	-------	---------	--------

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.

- 2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
- 3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].



Figure 20. DSPI classic SPI timing — master mode

64 LQFP	48 LQFP	32 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
40	32	-	PTB17	DISABLED		PTB17		UART0_TX	FTM_CLKIN1		EWM_OUT_b	
41	-	_	PTB18	DISABLED		PTB18		FTM2_CH0			FTM2_QD_ PHA	
42	-	-	PTB19	DISABLED		PTB19		FTM2_CH1			FTM2_QD_ PHB	
43	33	_	PTC0	ADC0_SE14	ADC0_SE14	PTC0	SPI0_PCS4	PDB0_ EXTRG		CMP0_OUT	FTM0_FLT1	SPI0_PCS0
44	34	22	PTC1/ LLWU_P6	ADC0_SE15	ADC0_SE15	PTC1/ LLWU_P6	SPI0_PCS3	UART1_RTS_ b	FTM0_CH0	FTM2_CH0		
45	35	23	PTC2	ADC0_SE4b/ CMP1_IN0	ADC0_SE4b/ CMP1_IN0	PTC2	SPI0_PCS2	UART1_CTS_ b	FTM0_CH1	FTM2_CH1		
46	36	24	PTC3/ LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT		
47	_	-	VSS	VSS	VSS							
48	_	-	VDD	VDD	VDD							
49	37	25	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3		CMP1_OUT	
50	38	26	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2			CMP0_OUT	FTM0_CH2
51	39	27	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_ EXTRG		UART0_RX		I2C0_SCL
52	40	28	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN			UART0_TX		I2C0_SDA
53	-	-	PTC8	ADC1_SE4b/ CMP0_IN2	ADC1_SE4b/ CMP0_IN2	PTC8						
54	-	_	PTC9	ADC1_SE5b/ CMP0_IN3	ADC1_SE5b/ CMP0_IN3	PTC9					FTM2_FLT0	
55	_	Ι	PTC10	ADC1_SE6b	ADC1_SE6b	PTC10						
56	_		PTC11/ LLWU_P11	ADC1_SE7b	ADC1_SE7b	PTC11/ LLWU_P11						
57	41	-	PTD0/ LLWU_P12	DISABLED		PTD0/ LLWU_P12	SPI0_PCS0	UART0_RTS_ b	FTM0_CH0	UART1_RX		
58	42	-	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK	UART0_CTS_ b	FTM0_CH1	UART1_TX		
59	43	_	PTD2/ LLWU_P13	DISABLED		PTD2/ LLWU_P13	SPI0_SOUT	UART0_RX	FTM0_CH2			I2C0_SCL
60	44	_	PTD3	DISABLED		PTD3	SPI0_SIN	UART0_TX	FTM0_CH3			I2C0_SDA
61	45	29	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI0_PCS1	UART0_RTS_ b	FTM0_CH4	FTM2_CH0	EWM_IN	
62	46	30	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI0_PCS2	UART0_CTS_ b	FTM0_CH5	FTM2_CH1	EWM_OUT_b	
63	47	31	PTD6/ LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH0	FTM1_CH0	FTM0_FLT0	
64	48	32	PTD7	DISABLED		PTD7		UART0_TX	FTM0_CH1	FTM1_CH1	FTM0_FLT1	

7.2 Examples

Operating rating:

Symbol	Description	Min.	Max.	Unit					
V _{DD}	1.0 V core supply voltage	-0.3	1.2	V					
	-								

Operating requirement:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	0.9	1.1	v

4.

Operating behavior that includes a typical value:

Symbol	Description	Min.	Тур.	Max.	Unit
I _{WP}	Digital I/O weak pullup/pulldown current	10 AM	70	130	μA

7.3 Typical-value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T _A	Ambient temperature	25	Ο°
V _{DD}	Supply voltage	3.3	V

Rev. No.	Date	Substantial Changes
Hev. No.	Date	 On p. 1, added parenthetical element to the following bullet under "Analog modules": Accurate internal voltage reference (not available for 32-pin QFN package) In "Voltage and current operating ratings" section, updated digital supply current maximum value In "Voltage and current operating behaviors" section, updated input leakage information In "Power consumption operating behaviors table": Updated existing typical and maximum power measurements Added new typical power measurements for the following: IDD_HSRUN (High Speed Run mode, all peripheral clocks disabled, current executing CoreMark code) IDD_HSRUN (Hugh Speed Run mode, all peripheral clocks disabled, current executing While(1) loop) IDD_RUN (Run mode current in Compute operation, all peripheral clocks disabled, executing CoreMark code) IDD_RUN (Run mode current in Compute operation, all peripheral clocks disabled, executing While(1) loop) IDD_RUN (Run mode current in Compute operation, all peripheral clocks disabled, executing While(1) loop) IDD_LVLPR (Very Low Power mode current in Compute operation, all peripheral clocks disabled, executing CoreMark code) IDD_VLPR (Very Low Power Run mode current in Compute operation, all peripheral clocks disabled, executing While(1) loop) Updated section, "EMC radiated emissions operating behaviors for 64 LQFP package" In "Thermal attributes" section, added 64-pin LQFP and 32-pin QFN package values Updated "WCG specifications" table Updated "WREF full-range operating behaviors" table
1	3/201/	• In the Part identification section, added Format and Fleids subsections
1	3/2014	

Table 39. Revision History (continued)