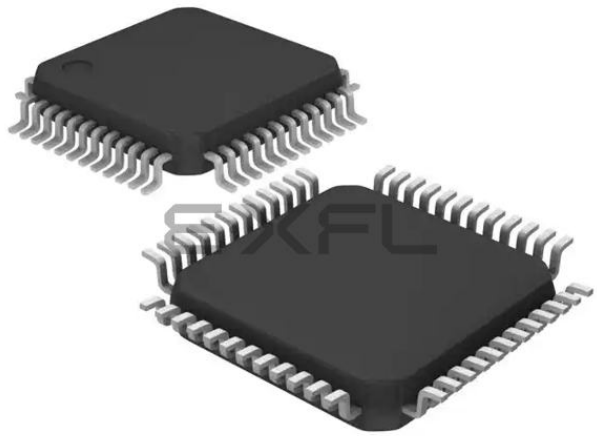


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 100MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | DMA, PWM, WDT |
| Number of I/O | 35 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3.6V |
| Data Converters | A/D 2x16b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mkv30f64vlf10r |

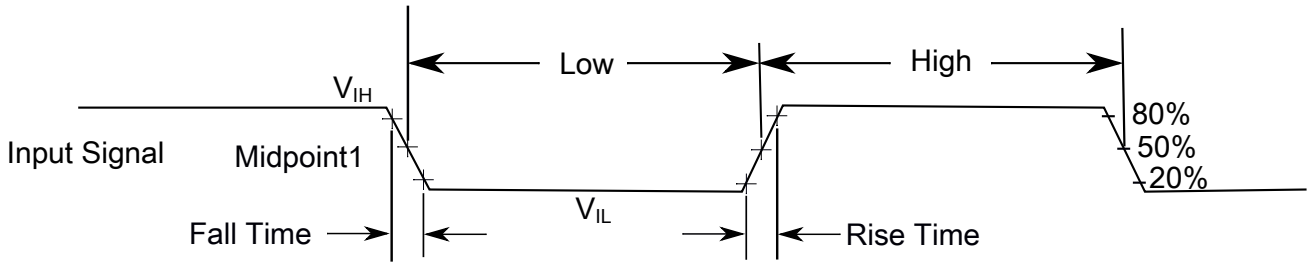
| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Digital supply voltage | –0.3 | 3.8 | V |
| $I_{DD}$ | Digital supply current | — | 145 | mA |
| $V_{DIO}$ | Digital input voltage | –0.3 | $V_{DD}$ + 0.3 | V |
| $V_{AIO}$ | Analog[1] | –0.3 | $V_{DD}$ + 0.3 | V |
| $I_D$ | Maximum current single pin limit (applies to all digital pins) | –25 | 25 | mA |
| $V_{DDA}$ | Analog supply voltage | $V_{DD}$ – 0.3 | $V_{DD}$ + 0.3 | V |

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

# 2 General

## 2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.




The midpoint is $V_{IL}$ + ($V_{IH}$ - $V_{IL}$) / 2

**Figure 2. Input signal measurement reference**

## 2.2 Nonswitching electrical specifications

### 2.2.1 Voltage and current operating requirements

**Table 1. Voltage and current operating requirements**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.71 | 3.6 | V | |

*Table continues on the next page...*

**Table 4. Power mode transition operating behaviors (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | • VLLS3 → RUN | — | — | 75 | µs | |
| | • VLPS → RUN | — | — | 5.7 | µs | |
| | • STOP → RUN | — | — | 5.7 | µs | |

1. Normal boot (FTFA_OPT[LPBOOT]=1)

## 2.2.5 Power consumption operating behaviors

The current parameters in the table below are derived from code executing a while(1) loop from flash, unless otherwise noted.

The IDD typical values represent the statistical mean at 25°C, and the IDD maximum values for RUN, WAIT, VLPR, and VLPW represent data collected at 125°C junction temperature unless otherwise noted. The maximum values represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

**Table 5. Power consumption operating behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DDA}$ | Analog supply current | — | — | See note | mA | 1 |
| $I_{DD\_HSRUN}$ | High Speed Run mode current - all peripheral clocks disabled, CoreMark benchmark code executing from flash | | | | | |
| | @ 1.8V | — | 18.70 | 19.37 | mA | 2, 3, 4 |
| | @ 3.0V | — | 18.71 | 19.38 | mA | |
| $I_{DD\_HSRUN}$ | High Speed Run mode current - all peripheral clocks disabled, code executing from flash | | | | | |
| | @ 1.8V | — | 18.13 | 18.80 | mA | 4 |
| | @ 3.0V | — | 18.19 | 18.86 | mA | |
| $I_{DD\_HSRUN}$ | High Speed Run mode current — all peripheral clocks enabled, code executing from flash | | | | | |
| | @ 1.8V | — | 22.2 | 22.87 | mA | 5 |
| | @ 3.0V | — | 22.4 | 23.07 | mA | |
| $I_{DD\_RUN}$ | Run mode current in Compute operation — CoreMark benchmark code executing from flash | | | | | |
| | @ 1.8V | — | 12.74 | 13.41 | mA | 2, 3, 6 |
| | @ 3.0V | — | 12.82 | 13.49 | mA | |

*Table continues on the next page...*

**Table 6. Low power mode peripheral adders—typical value (continued)**

| Symbol | Description | Temperature (°C) | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | -40 | 25 | 50 | 70 | 85 | 105 | |
| | VLPS | 510 | 560 | 560 | 560 | 610 | 680 | |
| | STOP | 510 | 560 | 560 | 560 | 610 | 680 | |
| $I_{48MIRC}$ | 48 Mhz internal reference clock | 350 | 350 | 350 | 350 | 350 | 350 | µA |
| $I_{CMP}$ | CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption. | 22 | 22 | 22 | 22 | 22 | 22 | µA |
| $I_{UART}$ | UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption. | | | | | | | |
| | MCGIRCLK (4 MHz internal reference clock) | 66 | 66 | 66 | 66 | 66 | 66 | µA |
| | >OSCERCLK (4 MHz external crystal) | 214 | 237 | 246 | 254 | 260 | 268 | |
| $I_{BG}$ | Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode. | 45 | 45 | 45 | 45 | 45 | 45 | µA |
| $I_{ADC}$ | ADC peripheral adder combining the measured values at $V_{DD}$ and $V_{DDA}$ by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions. | 42 | 42 | 42 | 42 | 42 | 42 | µA |

### 2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode for 50 MHz and lower frequencies. MCG in FEE mode at frequencies between 50 MHz and 100MHz.
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

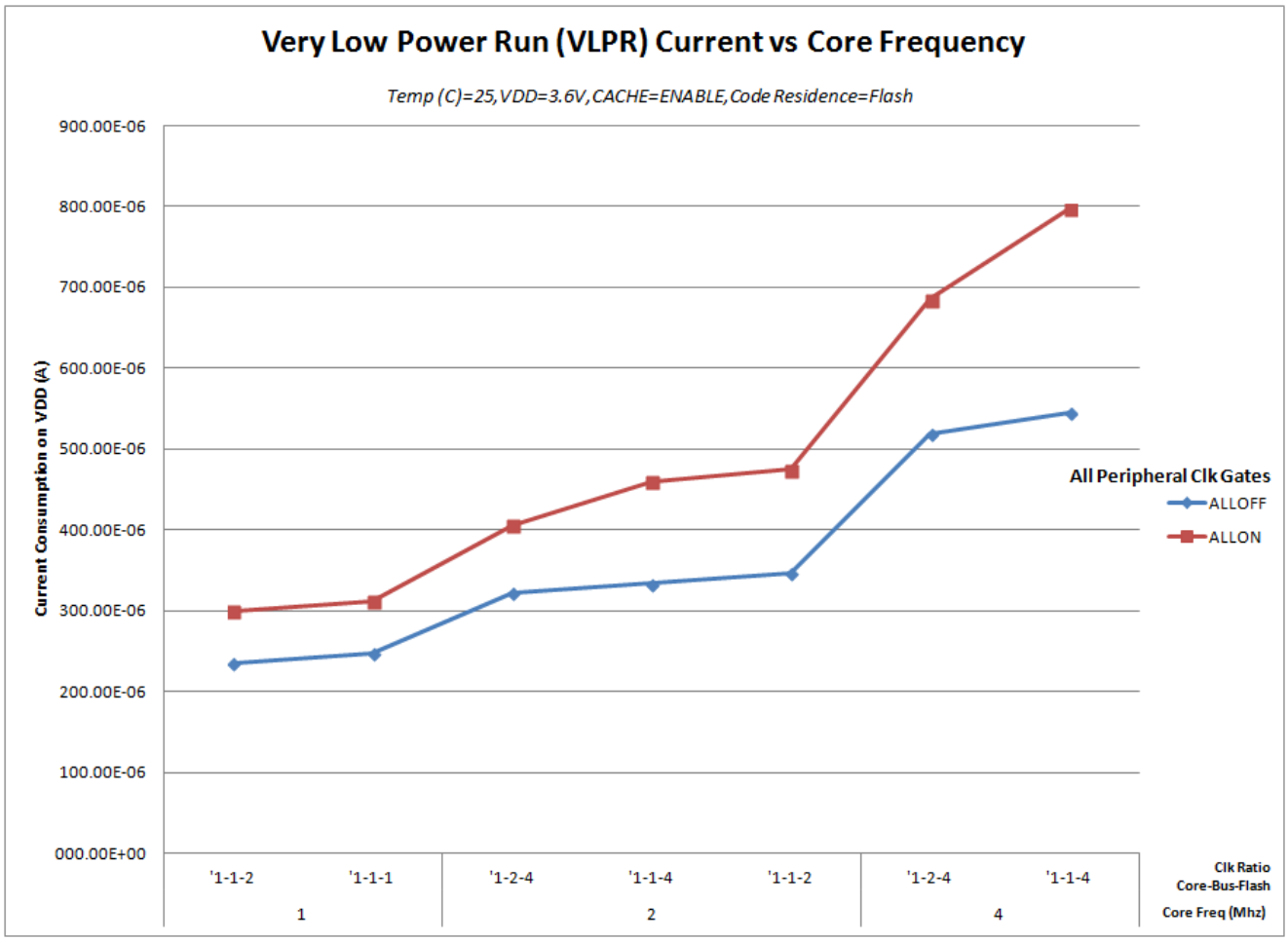



**Figure 4. VLPR mode supply current vs. core frequency**

## 2.2.6 EMC radiated emissions operating behaviors

**Table 7. EMC radiated emissions operating behaviors for 64 LQFP package**

| Parameter | Conditions | Clocks | Frequency range | Level (Typ.) | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{EME}$ | Device configuration, test conditions and EM testing per standard IEC 61967-2.<br>Supply voltage: VDD = 3.3 V<br>Temp = 25°C | FSYS = 100 MHz<br>FBUS = 50 MHz<br>External crystal = 10 MHz | 150 kHz–50 MHz | 11 | dBuV | 1, 2, 3 |
| | | | 50 MHz–150 MHz | 12 | | |
| | | | 150 MHz–500 MHz | 11 | | |
| | | | 500 MHz–1000 MHz | 8 | | |
| | | | IEC level | N | | 4 |

1. Measurements were made per IEC 61967-2 while the device was running typical application code.
2. Measurements were performed on the 64LQFP device, MKV30F128VLH10.
3. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

## 2.4.1 Thermal operating requirements

**Table 11. Thermal operating requirements**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $T_J$ | Die junction temperature | –40 | 125 | °C | |
| $T_A$ | Ambient temperature | –40 | 105 | °C | 1 |

1. Maximum $T_A$ can be exceeded only if the user ensures that $T_J$ does not exceed maximum $T_J$. The simplest method to determine $T_J$ is: $T_J = T_A + R_{\Theta JA} \times$ chip power dissipation.

## 2.4.2 Thermal attributes

| Board type | Symbol | Description | 64 LQFP | 48 LQFP | 32 QFN | Unit | Notes |
|---|---|---|---|---|---|---|---|
| Single-layer (1s) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 66 | 79 | 97 | °C/W | 1 |
| Four-layer (2s2p) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 48 | 55 | 33 | °C/W | 1 |
| Single-layer (1s) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 54 | 67 | 81 | °C/W | 1 |
| Four-layer (2s2p) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 41 | 49 | 28 | °C/W | 1 |
| — | $R_{\theta JB}$ | Thermal resistance, junction to board | 30 | 33 | 13 | °C/W | 2 |
| — | $R_{\theta JC}$ | Thermal resistance, junction to case | 17 | 23 | 2.0 | °C/W | 3 |

*Table continues on the next page...*

| Board type | Symbol | Description | 64 LQFP | 48 LQFP | 32 QFN | Unit | Notes |
|---|---|---|---|---|---|---|---|
| — | $\Psi_{JT}$ | Thermal characterization parameter, junction to package top outside center (natural convection) | 3 | 5 | 6 | °C/W | 4 |

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

# 3 Peripheral operating requirements and behaviors

## 3.1 Core modules

### 3.1.1 SWD electricals

**Table 12. SWD full voltage range electricals**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |
| S1 | SWD_CLK frequency of operation<br>• Serial wire debug | 0 | 33 | MHz |
| S2 | SWD_CLK cycle period | 1/S1 | — | ns |
| S3 | SWD_CLK clock pulse width<br>• Serial wire debug | 15 | — | ns |
| S4 | SWD_CLK rise and fall times | — | 3 | ns |
| S9 | SWD_DIO input data setup time to SWD_CLK rise | 8 | — | ns |
| S10 | SWD_DIO input data hold time after SWD_CLK rise | 1.4 | — | ns |
| S11 | SWD_CLK high to SWD_DIO data valid | — | 25 | ns |
| S12 | SWD_CLK high to SWD_DIO high-Z | 5 | — | ns |

## 3.3.3 Oscillator electrical specifications

### 3.3.3.1 Oscillator DC electrical specifications

**Table 17. Oscillator DC electrical specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.71 | — | 3.6 | V | |
| $I_{DDOSC}$ | Supply current — low-power mode (HGO=0) | | | | | 1 |
| | • 32 kHz | — | 500 | — | nA | |
| | • 4 MHz | — | 200 | — | µA | |
| | • 8 MHz (RANGE=01) | — | 300 | — | µA | |
| | • 16 MHz | — | 950 | — | µA | |
| | • 24 MHz | — | 1.2 | — | mA | |
| | • 32 MHz | — | 1.5 | — | mA | |
| $I_{DDOSC}$ | Supply current — high-gain mode (HGO=1) | | | | | 1 |
| | • 32 kHz | — | 25 | — | µA | |
| | • 4 MHz | — | 400 | — | µA | |
| | • 8 MHz (RANGE=01) | — | 500 | — | µA | |
| | • 16 MHz | — | 2.5 | — | mA | |
| | • 24 MHz | — | 3 | — | mA | |
| | • 32 MHz | — | 4 | — | mA | |
| $C_x$ | EXTAL load capacitance | — | — | — | | 2, 3 |
| $C_y$ | XTAL load capacitance | — | — | — | | 2, 3 |
| $R_F$ | Feedback resistor — low-frequency, low-power mode (HGO=0) | — | — | — | MΩ | 2, 4 |
| | Feedback resistor — low-frequency, high-gain mode (HGO=1) | — | 10 | — | MΩ | |
| | Feedback resistor — high-frequency, low-power mode (HGO=0) | — | — | — | MΩ | |
| | Feedback resistor — high-frequency, high-gain mode (HGO=1) | — | 1 | — | MΩ | |
| $R_S$ | Series resistor — low-frequency, low-power mode (HGO=0) | — | — | — | kΩ | |
| | Series resistor — low-frequency, high-gain mode (HGO=1) | — | 200 | — | kΩ | |
| | Series resistor — high-frequency, low-power mode (HGO=0) | — | — | — | kΩ | |
| | Series resistor — high-frequency, high-gain mode (HGO=1) | — | 0 | — | kΩ | |

*Table continues on the next page...*

4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz

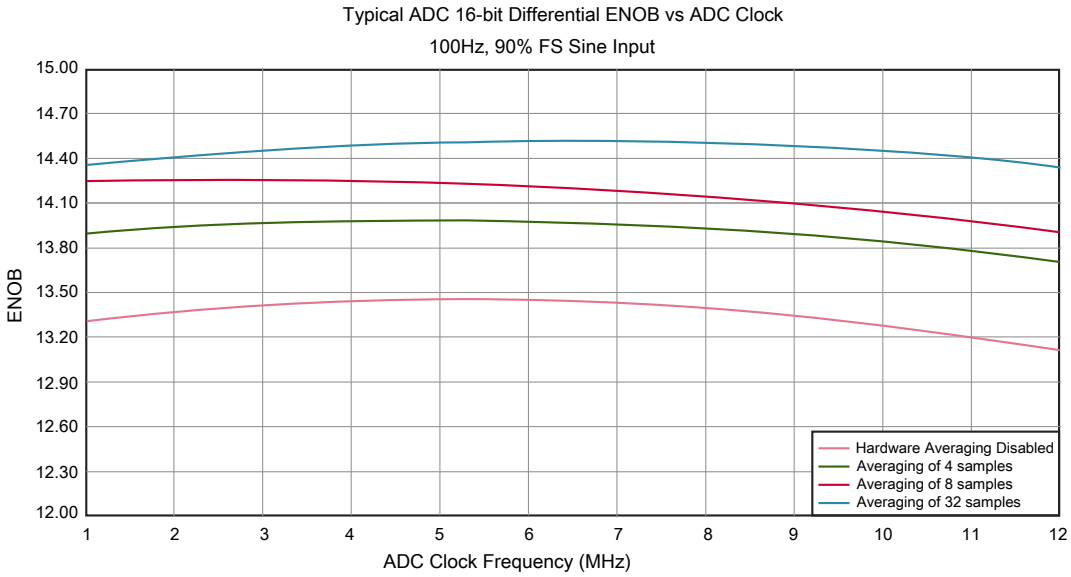



**Figure 12. Typical ENOB vs. ADC_CLK for 16-bit differential mode**

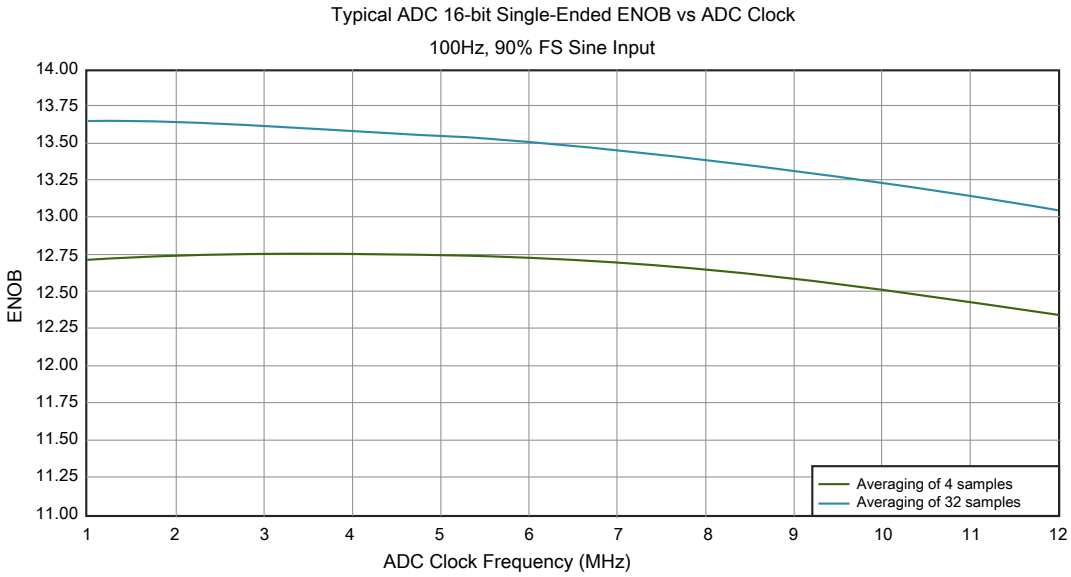



**Figure 13. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode**

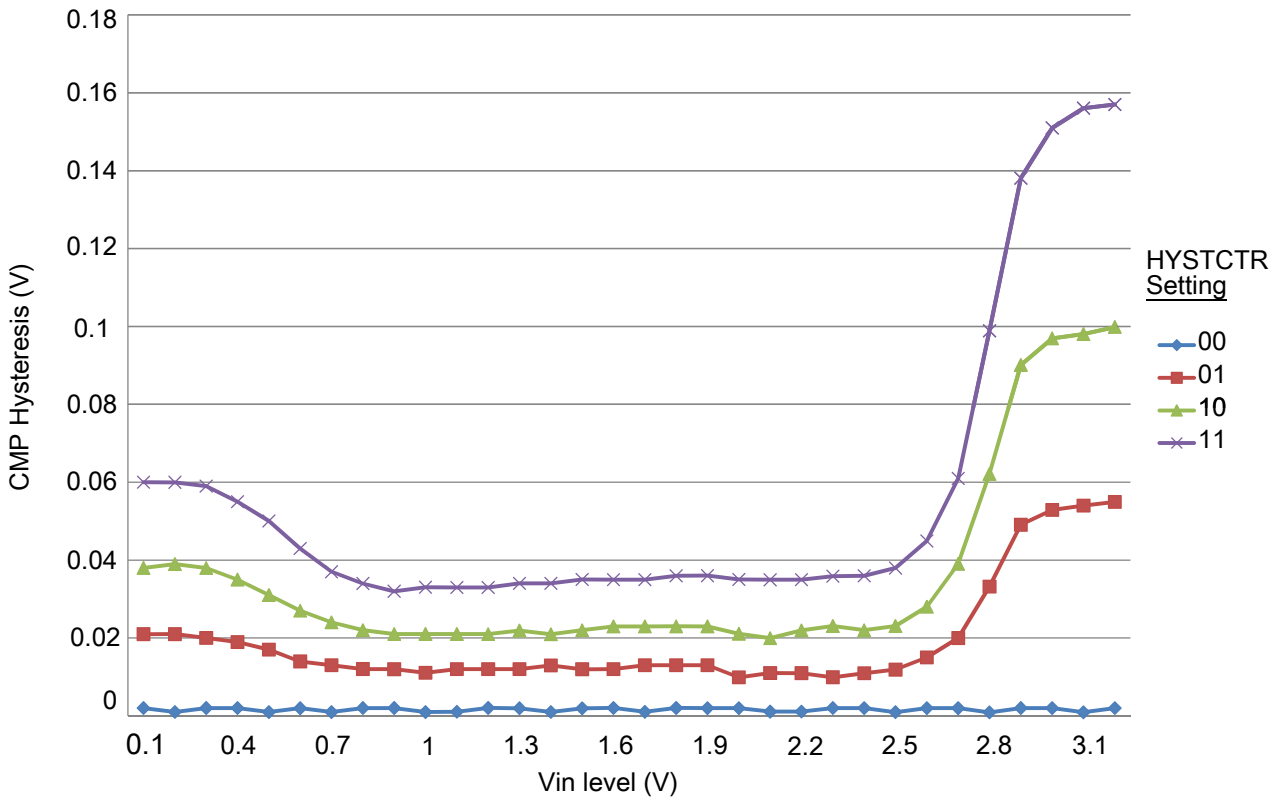



**Figure 15. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)**

## 3.6.3 12-bit DAC electrical characteristics

### 3.6.3.1 12-bit DAC operating requirements

**Table 26. 12-bit DAC operating requirements**

| Symbol | Desciption | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | 1.71 | 3.6 | V | |
| $V_{DACR}$ | Reference voltage | 1.13 | 3.6 | V | 1 |
| $C_L$ | Output load capacitance | — | 100 | pF | 2 |
| $I_L$ | Output load current | — | 1 | mA | |

1. The DAC reference can be selected to be $V_{DDA}$ or $V_{REFH}$.
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

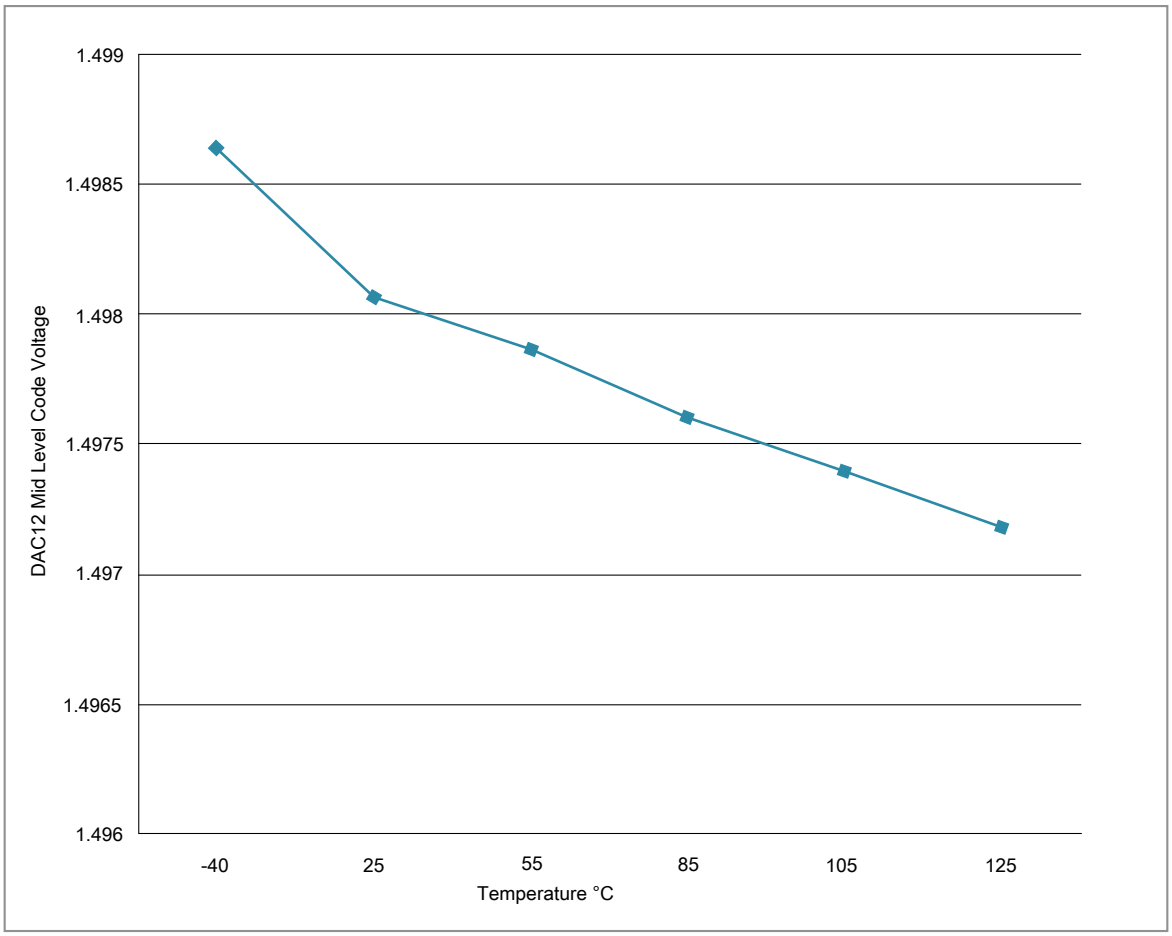



**Figure 17. Offset at half scale vs. temperature**

## 3.6.4 Voltage reference electrical specifications

**Table 28. VREF full-range operating requirements**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | 1.71 | 3.6 | V | |
| $T_A$ | Temperature | Operating temperature range of the device | | °C | |
| $C_L$ | Output load capacitance | 100 | | nF | 1, 2 |

1. $C_L$ must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified $C_L$ value over the operating temperature range of the device.

**Table 29. VREF full-range operating behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{out}$ | Voltage reference output with factory trim at nominal $V_{DDA}$ and temperature=25°C | 1.1920 | 1.1950 | 1.1980 | V | 1 |
| $V_{out}$ | Voltage reference output with user trim at nominal $V_{DDA}$ and temperature=25°C | 1.1945 | 1.1950 | 1.1955 | V | 1 |
| $V_{step}$ | Voltage reference trim step | — | 0.5 | — | mV | 1 |
| $V_{tdrift}$ | Temperature drift (Vmax -Vmin across the full temperature range) | — | — | 15 | mV | 1 |
| $I_{bg}$ | Bandgap only current | — | — | 80 | µA | |
| $I_{lp}$ | Low-power buffer current | — | — | 360 | uA | 1 |
| $I_{hp}$ | High-power buffer current | — | — | 1 | mA | 1 |
| $\Delta V_{LOAD}$ | Load regulation<br>• current = ± 1.0 mA | —<br> | 200<br> | —<br> | µV<br> | 1, 2<br> |
| $T_{stup}$ | Buffer startup time | — | — | 100 | µs | |
| $T_{chop\_osc\_startup}$ | Internal bandgap start-up delay with chop oscillator enabled | — | — | 35 | ms | |
| $V_{vdrift}$ | Voltage drift (Vmax -Vmin across the full voltage range) | — | 2 | — | mV | 1 |

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

**Table 30. VREF limited-range operating requirements**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $T_A$ | Temperature | 0 | 70 | °C | |

**Table 31. VREF limited-range operating behaviors**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{tdrift}$ | Temperature drift ($V_{max}$ -$V_{min}$ across the limited temperature range) | — | 10 | mV | |

## 3.7 Timers

See General switching specifications.

## 3.8 Communication interfaces

## Table 36. I²C timing (continued)

| Characteristic | Symbol | Standard Mode | | Fast Mode | | Unit |
|---|---|---|---|---|---|---|
| | | Minimum | Maximum | Minimum | Maximum | |
| Data hold time for I²C bus devices | $t_{HD}$; DAT | 0[2] | 3.45[3] | 0[4] | 0.9[2] | µs |
| Data set-up time | $t_{SU}$; DAT | 250[5] | — | 100[3, 6] | — | ns |
| Rise time of SDA and SCL signals | $t_r$ | — | 1000 | 20 +0.1$C_b$[7] | 300 | ns |
| Fall time of SDA and SCL signals | $t_f$ | — | 300 | 20 +0.1$C_b$[6] | 300 | ns |
| Set-up time for STOP condition | $t_{SU}$; STO | 4 | — | 0.6 | — | µs |
| Bus free time between STOP and START condition | $t_{BUF}$ | 4.7 | — | 1.3 | — | µs |
| Pulse width of spikes that must be suppressed by the input filter | $t_{SP}$ | N/A | N/A | 0 | 50 | ns |

1. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can only be achieved when using the High drive pins across the full voltage range and when using the Normal drive pins and VDD ≥ 2.7 V.
2. The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
3. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
4. Input signal Slew = 10 ns and Output Load = 50 pF
5. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
6. A Fast mode I²C bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU;\ DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT} = 1000 + 250 = 1250$ ns (according to the Standard mode I²C bus specification) before the SCL line is released.
7. $C_b$ = total capacitance of the one bus line in pF.

## Table 37. I²C 1 Mbps timing

| Characteristic | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|
| SCL Clock Frequency | $f_{SCL}$ | 0 | 1[1] | MHz |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated. | $t_{HD}$; STA | 0.26 | — | µs |
| LOW period of the SCL clock | $t_{LOW}$ | 0.5 | — | µs |
| HIGH period of the SCL clock | $t_{HIGH}$ | 0.26 | — | µs |
| Set-up time for a repeated START condition | $t_{SU}$; STA | 0.26 | — | µs |
| Data hold time for $I_2C$ bus devices | $t_{HD}$; DAT | 0 | — | µs |
| Data set-up time | $t_{SU}$; DAT | 50 | — | ns |
| Rise time of SDA and SCL signals | $t_r$ | 20 +0.1$C_b$,[2] | 120 | ns |
| Fall time of SDA and SCL signals | $t_f$ | 20 +0.1$C_b$[2] | 120 | ns |
| Set-up time for STOP condition | $t_{SU}$; STO | 0.26 | — | µs |
| Bus free time between STOP and START condition | $t_{BUF}$ | 0.5 | — | µs |
| Pulse width of spikes that must be suppressed by the input filter | $t_{SP}$ | 0 | 50 | ns |

1. The maximum SCL clock frequency of 1 Mbps can support maximum bus loading when using the High drive pins across the full voltage range.
2. $C_b$ = total capacitance of the one bus line in pF.

| 64 LQFP | 48 LQFP | 32 QFN | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 14 | 10 | 7 | VREFH | VREFH | VREFH | | | | | | | |
| 15 | 11 | 8 | VREFL | VREFL | VREFL | | | | | | | |
| 16 | 12 | 8 | VSSA | VSSA | VSSA | | | | | | | |
| 17 | 13 | — | VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18 | VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18 | VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18 | | | | | | | |
| 18 | 14 | 9 | DAC0_OUT/ CMP1_IN3/ ADC0_SE23 | DAC0_OUT/ CMP1_IN3/ ADC0_SE23 | DAC0_OUT/ CMP1_IN3/ ADC0_SE23 | | | | | | | |
| 19 | — | — | CMP0_IN4/ ADC1_SE23 | CMP0_IN4/ ADC1_SE23 | CMP0_IN4/ ADC1_SE23 | | | | | | | |
| 20 | 15 | 10 | PTE24 | ADC0_SE17 | ADC0_SE17 | PTE24 | | FTM0_CH0 | | I2C0_SCL | EWM_OUT_b | |
| 21 | 16 | 11 | PTE25 | ADC0_SE18 | ADC0_SE18 | PTE25 | | FTM0_CH1 | | I2C0_SDA | EWM_IN | |
| 22 | 17 | 12 | PTA0 | JTAG_TCLK/ SWD_CLK | | PTA0 | UART0_CTS_ b | FTM0_CH5 | | EWM_IN | | JTAG_TCLK/ SWD_CLK |
| 23 | 18 | 13 | PTA1 | JTAG_TDI | | PTA1 | UART0_RX | FTM2_CH0 | CMP0_OUT | FTM2_QD_ PHA | FTM1_CH1 | JTAG_TDI |
| 24 | 19 | 14 | PTA2 | JTAG_TDO/ TRACE_SWO | | PTA2 | UART0_TX | FTM2_CH1 | CMP1_OUT | FTM2_QD_ PHB | FTM1_CH0 | JTAG_TDO/ TRACE_SWO |
| 25 | 20 | 15 | PTA3 | JTAG_TMS/ SWD_DIO | | PTA3 | UART0_RTS_ b | FTM0_CH0 | FTM2_FLT0 | EWM_OUT_b | | JTAG_TMS/ SWD_DIO |
| 26 | 21 | 16 | PTA4/ LLWU_P3 | NMI_b | | PTA4/ LLWU_P3 | | FTM0_CH1 | | FTM0_FLT3 | | NMI_b |
| 27 | — | — | PTA5 | DISABLED | | PTA5 | | FTM0_CH2 | | | | JTAG_TRST_ b |
| 28 | — | — | PTA12 | DISABLED | | PTA12 | | FTM1_CH0 | | | | FTM1_QD_ PHA |
| 29 | — | — | PTA13/ LLWU_P4 | DISABLED | | PTA13/ LLWU_P4 | | FTM1_CH1 | | | | FTM1_QD_ PHB |
| 30 | 22 | — | VDD | VDD | VDD | | | | | | | |
| 31 | 23 | — | VSS | VSS | VSS | | | | | | | |
| 32 | 24 | 17 | PTA18 | EXTAL0 | EXTAL0 | PTA18 | | FTM0_FLT2 | FTM_CLKIN0 | | | |
| 33 | 25 | 18 | PTA19 | XTAL0 | XTAL0 | PTA19 | FTM0_FLT0 | FTM1_FLT0 | FTM_CLKIN1 | | LPTMR0_ ALT1 | |
| 34 | 26 | 19 | RESET_b | RESET_b | RESET_b | | | | | | | |
| 35 | 27 | 20 | PTB0/ LLWU_P5 | ADC0_SE8/ ADC1_SE8 | ADC0_SE8/ ADC1_SE8 | PTB0/ LLWU_P5 | I2C0_SCL | FTM1_CH0 | | | FTM1_QD_ PHA | UART0_RX |
| 36 | 28 | 21 | PTB1 | ADC0_SE9/ ADC1_SE9 | ADC0_SE9/ ADC1_SE9 | PTB1 | I2C0_SDA | FTM1_CH1 | FTM0_FLT2 | EWM_IN | FTM1_QD_ PHB | UART0_TX |
| 37 | 29 | — | PTB2 | ADC0_SE12 | ADC0_SE12 | PTB2 | I2C0_SCL | UART0_RTS_ b | FTM0_FLT1 | | FTM0_FLT3 | |
| 38 | 30 | — | PTB3 | ADC0_SE13 | ADC0_SE13 | PTB3 | I2C0_SDA | UART0_CTS_ b | | | FTM0_FLT0 | |
| 39 | 31 | — | PTB16 | DISABLED | | PTB16 | | UART0_RX | FTM_CLKIN0 | | EWM_IN | |

## 5.2 Recommended connection for unused analog and digital pins

The following table shows the recommended connections for analog interface pins if those analog interfaces are not used in the customer's application.

**Table 38. Recommended connection for unused analog interfaces**

| Pin Type | | Short recommendation | Detailed recommendation |
|---|---|---|---|
| Analog/non GPIO | PGAx/ADCx | Float | Analog input - Float |
| Analog/non GPIO | ADCx/CMPx | Float | Analog input - Float |
| Analog/non GPIO | VREF_OUT | Float | Analog output - Float |
| Analog/non GPIO | DACx_OUT | Float | Analog output - Float |
| Analog/non GPIO | RTC_WAKEUP_B | Float | Analog output - Float |
| Analog/non GPIO | XTAL32 | Float | Analog output - Float |
| Analog/non GPIO | EXTAL32 | Float | Analog input - Float |
| GPIO/Analog | PTA18/EXTAL0 | Float | Analog input - Float |
| GPIO/Analog | PTA19/XTAL0 | Float | Analog output - Float |
| GPIO/Analog | PTx/ADCx | Float | Float (default is analog input) |
| GPIO/Analog | PTx/CMPx | Float | Float (default is analog input) |
| GPIO/Digital | PTA0/JTAG_TCLK | Float | Float (default is JTAG with pulldown) |
| GPIO/Digital | PTA1/JTAG_TDI | Float | Float (default is JTAG with pullup) |
| GPIO/Digital | PTA2/JTAG_TDO | Float | Float (default is JTAG with pullup) |
| GPIO/Digital | PTA3/JTAG_TMS | Float | Float (default is JTAG with pullup) |
| GPIO/Digital | PTA4/NMI_b | 10kΩ pullup or disable and float | Pull high or disable in PCR & FOPT and float |
| GPIO/Digital | PTx | Float | Float (default is disabled) |
| VDDA | VDDA | Always connect to VDD potential | Always connect to VDD potential |
| VREFH | VREFH | Always connect to VDD potential | Always connect to VDD potential |
| VREFL | VREFL | Always connect to VSS potential | Always connect to VSS potential |
| VSSA | VSSA | Always connect to VSS potential | Always connect to VSS potential |

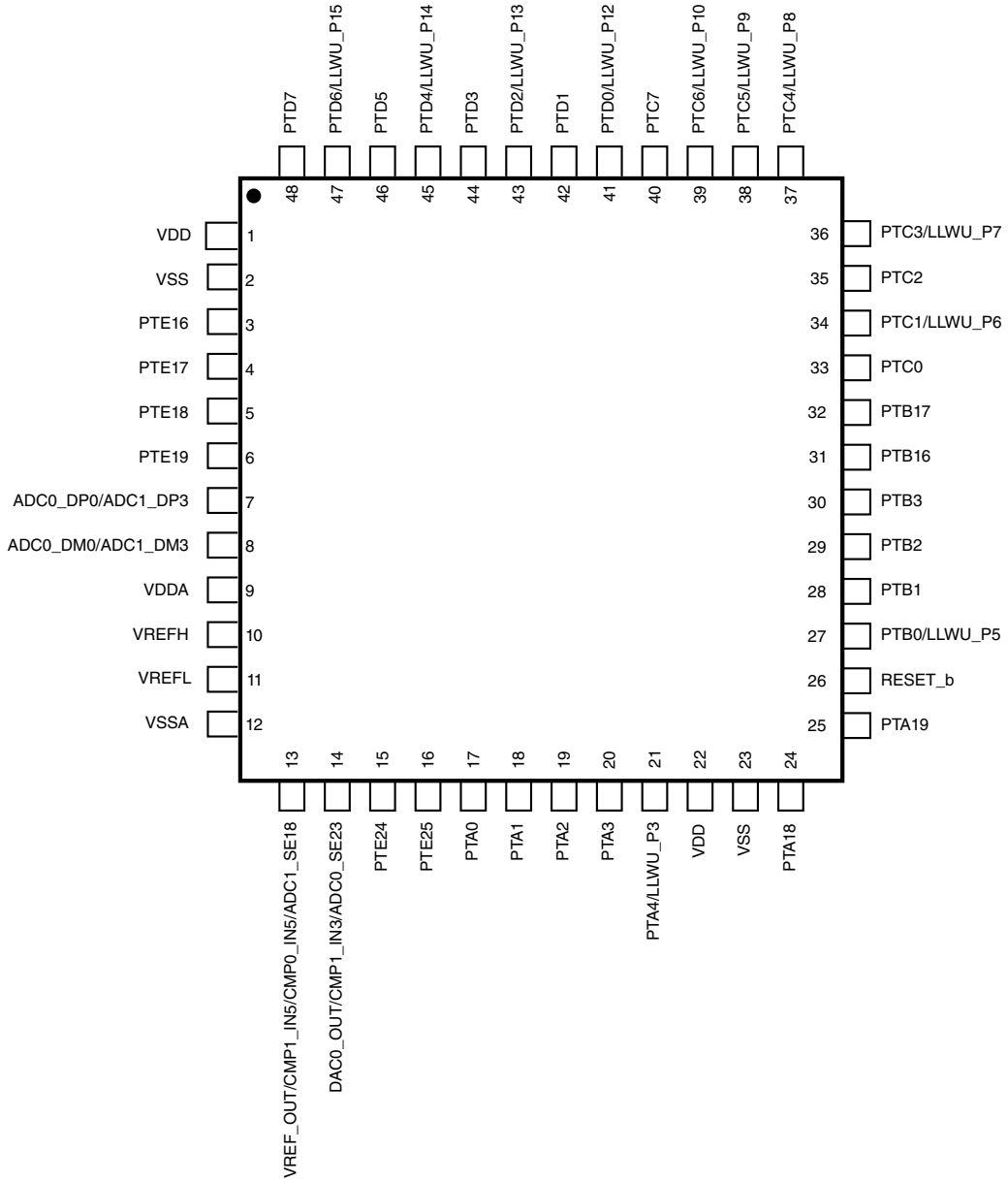



**Figure 24. KV30F 48 LQFP pinout diagram**

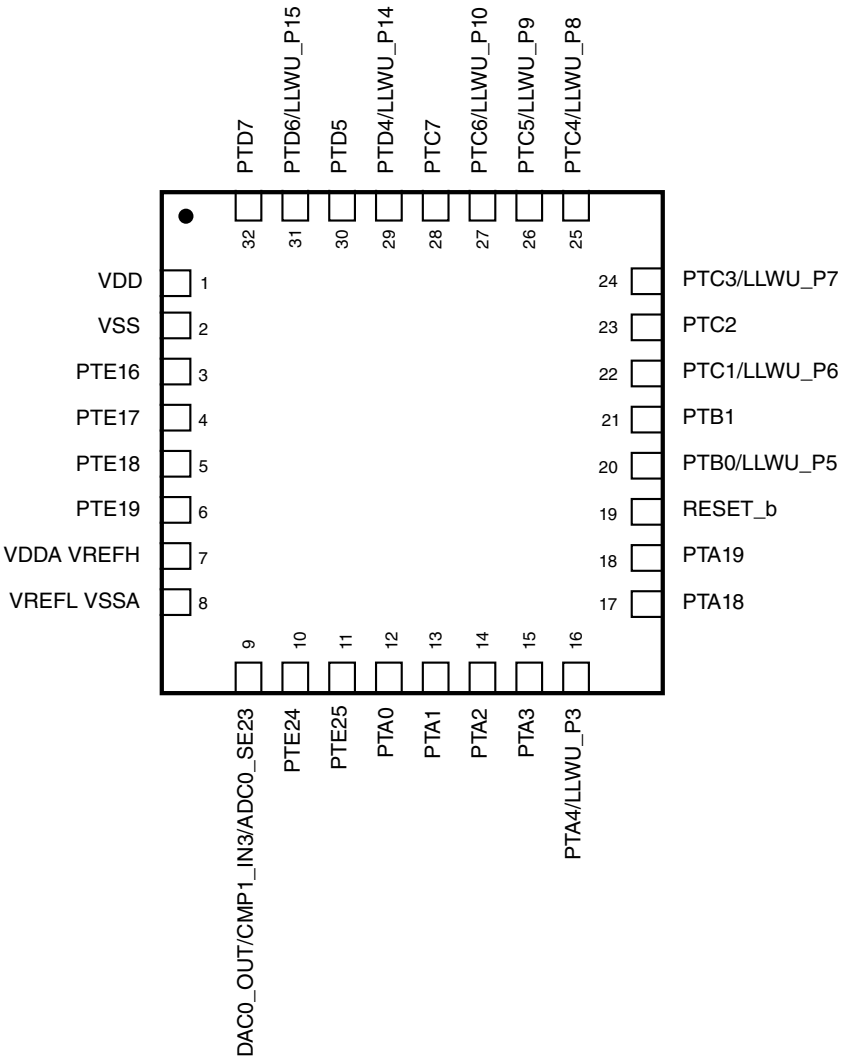



**Figure 25. KV30F 32 QFN pinout diagram (Transparent top view)**

# 6 Part identification

## 6.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

## 6.2 Format

Part numbers for this device have the following format:

Q KV## A FFF R T PP CC S N

## 6.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

| Field | Description | Values |
|---|---|---|
| Q | Qualification status | • M = Fully qualified, general market flow<br>• P = Prequalification |
| KV## | Kinetis V Series | • KV3x: Cortex-M4 based MCU |
| A | Key attribute | • D = Cortex-M4 w/ DSP<br>• F = Cortex-M4 w/ DSP and FPU |
| FFF | Program flash memory size | • 64 = 64 KB<br>• 128 = 128 KB<br>• 256 = 256 KB<br>• 512 = 512 KB |
| R | Silicon revision | • (Blank) = Main<br>• A = Revision after main |
| T | Temperature range (°C) | • V = –40 to 105<br>• C = –40 to 85 |
| PP | Package identifier | • FM = 32 QFN (5 mm x 5 mm)<br>• LF = 48 LQFP (7 mm x 7 mm)<br>• LH = 64 LQFP (10 mm x 10 mm)<br>• LL = 100 LQFP (14 mm x 14 mm)<br>• MC = 121 XFBGA (8 mm x 8 mm)<br>• DC = 121 XFBGA (8 mm x 8 mm x 0.5 mm) |
| CC | Maximum CPU frequency (MHz) | • 10 = 100 MHz<br>• 12 = 120 MHz |
| S | Software type | • P = KMS-PMSM and BLDC<br>• (Blank) = Not software enabled |
| N | Packaging type | • R = Tape and reel<br>• (Blank) = Trays |

## 6.4 Example

This is an example part number:

MKV30F128VLH10P

# 7 Terminology and guidelines

## 7.1 Definitions

Key terms are defined in the following table:

| Term | Definition |
|---|---|
| Rating | A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:<br>• *Operating ratings* apply during operation of the chip.<br>• *Handling ratings* apply when the chip is not powered.<br>**NOTE:** The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings. |
| Operating requirement | A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip |
| Operating behavior | A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions |
| Typical value | A specified value for a technical characteristic that:<br>• Lies within the range of values specified by the operating behavior<br>• Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions<br>**NOTE:** Typical values are provided as design guidelines and are neither tested nor guaranteed. |

## Table 39. Revision History (continued)

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| | | • On p. 1, added parenthetical element to the following bullet under "Analog modules":*Accurate internal voltage reference (not available for 32-pin QFN package)*<br>• In "Voltage and current operating ratings" section, updated digital supply current maximum value<br>• In "Voltage and current operating behaviors" section, updated input leakage information<br>• In "Power consumption operating behaviors table":<br>  • Updated existing typical and maximum power measurements<br>  • Added new typical power measurements for the following:<br>  • IDD_HSRUN (High Speed Run mode, all peripheral clocks disabled, current executing CoreMark code)<br>  • IDD_HSRUN (High Speed Run mode, all peripheral clocks disabled, current executing while(1) loop)<br>  • IDD_RUN (Run mode current in Compute operation, all peripheral clocks disabled, executing CoreMark code)<br>  • IDD_RUN (Run mode current in Compute operation, all peripheral clocks disabled, executing while(1) loop)<br>  • IDD_VLPR (Very Low Power mode current in Compute operation, all peripheral clocks disabled, executing CoreMark code)<br>  • IDD_VLPR (Very Low Power Run mode current in Compute operation, all peripheral clocks disabled, executing while(1) loop)<br>• Updated section, "EMC radiated emissions operating behaviors for 64 LQFP package"<br>• In "Thermal attributes" section, added 64-pin LQFP and 32-pin QFN package values<br>• Updated "MCG specifications" table<br>• Updated "VREF full-range operating behaviors" table<br>• In the "Part identification" section, added "Format" and "Fields" subsections |
| 1 | 3/2014 | Initial public release |

***How to Reach Us:***

**Home Page:**
freescale.com

**Web Support:**
freescale.com/support



Document Number KV30P64M100SFA
Revision 4, 02/2016