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#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	368 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f87-e-p

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

## 4.0 OSCILLATOR CONFIGURATIONS

## 4.1 Oscillator Types

The PIC16F87/88 can be operated in eight different oscillator modes. The user can program three configuration bits (FOSC2:FOSC0) to select one of these eight modes (modes 5-8 are new PIC16 oscillator configurations):

- 1. LP Low-Power Crystal
- 2. XT Crystal/Resonator
- 3. HS High-Speed Crystal/Resonator
- 4. RC External Resistor/Capacitor with Fosc/4 output on RA6
- 5. RCIO External Resistor/Capacitor with I/O on RA6
- 6. INTIO1 Internal Oscillator with Fosc/4 output on RA6 and I/O on RA7
- 7. INTIO2 Internal Oscillator with I/O on RA6 and RA7
- 8. ECIO External Clock with I/O on RA6

## 4.2 Crystal Oscillator/Ceramic Resonators

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1/CLKI and OSC2/CLKO pins to establish oscillation (see Figure 4-1 and Figure 4-2). The PIC16F87/88 oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturer's specifications.





# TABLE 4-1:CAPACITOR SELECTION FOR<br/>CRYSTAL OSCILLATOR (FOR<br/>DESIGN GUIDANCE ONLY)

Osc Type	Crystal	Typical Capacitor Values Tested:				
	Fieq	C1	C2			
LP	32 kHz	33 pF	33 pF			
XT	200 kHz	56 pF	56 pF			
	1 MHz	15 pF	15 pF			
	4 MHz	15 pF	15 pF			
HS	4 MHz	15 pF	15 pF			
	8 MHz	15 pF	15 pF			
	20 MHz	15 pF	15 pF			

#### Capacitor values are for design guidance only.

These capacitors were tested with the crystals listed below for basic start-up and operation. These values were not optimized.

Different capacitor values may be required to produce acceptable oscillator operation. The user should test the performance of the oscillator over the expected VDD and temperature range for the application.

See the notes following this table for additional information.

- Note 1: Higher capacitance increases the stability of oscillator but also increases the start-up time.
  - 2: Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.
  - **3:** Rs may be required in HS mode, as well as XT mode, to avoid overdriving crystals with low drive level specification.
  - **4:** Always verify oscillator performance over the VDD and temperature range that is expected for the application.

## 4.6 Clock Sources and Oscillator Switching

The PIC16F87/88 devices include a feature that allows the system clock source to be switched from the main oscillator to an alternate low-frequency clock source. PIC16F87/88 devices offer three alternate clock sources. When enabled, these give additional options for switching to the various power-managed operating modes.

Essentially, there are three clock sources for these devices:

- Primary oscillators
- Secondary oscillators
- Internal oscillator block (INTRC)

The **primary oscillators** include the External Crystal and Resonator modes, the External RC modes, the External Clock mode and the internal oscillator block. The particular mode is defined on POR by the contents of Configuration Word 1. The details of these modes are covered earlier in this chapter.

The **secondary oscillators** are those external sources not connected to the OSC1 or OSC2 pins. These sources may continue to operate even after the controller is placed in a power-managed mode.

PIC16F87/88 devices offer the Timer1 oscillator as a secondary oscillator. This oscillator continues to run when a SLEEP instruction is executed and is often the time base for functions such as a real-time clock.

Most often, a 32.768 kHz watch crystal is connected between the RB6/T1OSO and RB7/T1OSI pins. Like the LP mode oscillator circuit, loading capacitors are also connected from each pin to ground. The Timer1 oscillator is discussed in greater detail in **Section 7.6 "Timer1 Oscillator"**.

In addition to being a primary clock source, the **internal oscillator block** is available as a power-managed mode clock source. The 31.25 kHz INTRC source is also used as the clock source for several special features, such as the WDT, Fail-Safe Clock Monitor, Power-up Timer and Two-Speed Start-up.

The clock sources for the PIC16F87/88 devices are shown in Figure 4-6. See **Section 7.0 "Timer1 Module"** for further details of the Timer1 oscillator. See **Section 15.1 "Configuration Bits"** for Configuration register details.

## 4.6.1 OSCCON REGISTER

The OSCCON register (Register 4-2) controls several aspects of the system clock's operation, both in full power operation and in power-managed modes.

The System Clock Select bits, SCS1:SCS0, select the clock source that is used when the device is operating in power-managed modes. When the bits are cleared (SCS<1:0> = 00), the system clock source comes from the main oscillator that is selected by the

FOSC2:FOSC0 configuration bits in Configuration Word 1 register. When the bits are set in any other manner, the system clock source is provided by the Timer1 oscillator (SCS1:SCS0 = 01) or from the internal oscillator block (SCS1:SCS0 = 10). After a Reset, SCS<1:0> are always set to '00'.

Note:	The instruction to immediately follow the
	modification of SCS<1:0> will have an
	instruction time (TCY) based on the previ-
	ous clock source. This should be taken
	into consideration when developing time
	dependant code.

The Internal Oscillator Select bits, IRCF2:IRCF0, select the frequency output of the internal oscillator block that is used to drive the system clock. The choices are the INTRC source (31.25 kHz), the INTOSC source (8 MHz) or one of the six frequencies derived from the INTOSC postscaler (125 kHz to 4 MHz). Changing the configuration of these bits has an immediate change on the multiplexor's frequency output.

The OSTS and IOFS bits indicate the status of the primary oscillator and INTOSC source; these bits are set when their respective oscillators are stable. In particular, OSTS indicates that the Oscillator Start-up Timer has timed out.

## 4.6.2 CLOCK SWITCHING

Clock switching will occur for the following reasons:

- The FCMEN (CONFIG2<0>) bit is set, the device is running from the primary oscillator and the primary oscillator fails. The clock source will be the internal RC oscillator.
- The FCMEN bit is set, the device is running from the T1OSC and T1OSC fails. The clock source will be the internal RC oscillator.
- Following a wake-up due to a Reset or a POR, when the device is configured for Two-Speed Start-up mode, switching will occur between the INTRC and the system clock defined by the FOSC<2:0> bits.
- A wake-up from Sleep occurs due to an interrupt or WDT wake-up and Two-Speed Start-up is enabled. If the primary clock is XT, HS or LP, the clock will switch between the INTRC and the primary system clock after 1024 clocks (OST) and 8 clocks of the primary oscillator. This is conditional upon the SCS bits being set equal to '00'.
- SCS bits are modified from their original value.
- IRCF bits are modified from their original value.
- Note: Because the SCS bits are cleared on any Reset, no clock switching will occur on a Reset unless the Two-Speed Start-up is enabled and the primary clock is XT, HS or LP. The device will wait for the primary clock to become stable before execution begins (Two-Speed Start-up disabled).

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#### 4.6.3 CLOCK TRANSITION AND WDT

When clock switching is performed, the Watchdog Timer is disabled because the Watchdog ripple counter is used as the Oscillator Start-up Timer.

Once the clock transition is complete (i.e., new oscillator selection switch has occurred), the Watchdog counter is re-enabled with the counter reset. This allows the user to synchronize the Watchdog Timer to the start of execution at the new clock frequency.

Note:	The OST is only used when switching to
	XT, HS and LP Oscillator modes.

## REGISTER 4-2: OSCCON: OSCILLATOR CONTROL REGISTER (ADDRESS 8Fh)

U-0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0
—	IRCF2	IRCF1	IRCF0	OSTS <sup>(1)</sup>	IOFS	SCS1	SCS0
bit 7							bit 0

- bit 7 Unimplemented: Read as '0'
- bit 6-4 IRCF<2:0>: Internal RC Oscillator Frequency Select bits
  - 000 = 31.25 kHz
  - 001 = 125 kHz
  - 010 = 250 kHz
  - 011 = 500 kHz
  - 100 = 1 MHz
  - 101 = 2 MHz
  - 110 = 4 MHz
  - 111 = 8 MHz

#### bit 3 **OSTS:** Oscillator Start-up Time-out Status bit<sup>(1)</sup>

- 1 = Device is running from the primary system clock
- 0 = Device is running from T1OSC or INTRC as a secondary system clock
  - Note 1: Bit resets to '0' with Two-Speed Start-up mode and LP, XT or HS selected as the oscillator mode.
- bit 2 **IOFS:** INTOSC Frequency Stable bit
  - 1 = Frequency is stable
  - 0 = Frequency is not stable
- bit 1-0 SCS<1:0>: Oscillator Mode Select bits
  - 00 = Oscillator mode defined by FOSC<2:0>
  - 01 = T1OSC is used for system clock
  - 10 = Internal RC is used for system clock
  - 11 = Reserved

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

## 4.7.3.2 Returning to Primary Oscillator with a Reset

A Reset will clear SCS<1:0> back to '00'. The sequence for starting the primary oscillator following a Reset is the same for all forms of Reset, including POR. There is no transition sequence from the alternate system clock to the primary system clock on a Reset condition. Instead, the device will reset the state of the OSCCON register and default to the primary system clock. The sequence of events that takes place after this will depend upon the value of the FOSC bits in the Configuration register. If the external oscillator is configured as a crystal (HS, XT or LP), the CPU will be held in the Q1 state until 1024 clock cycles have transpired on the primary clock. This is necessary because the crystal oscillator has been powered down until the time of the transition.

During the oscillator start-up time, instruction execution and/or peripheral operation is suspended.

Note:	If Two-Speed Clock Start	up mode is							
	enabled, the INTRC will act as the syster								
	clock until the OST timer ha	s timed out.							

If the primary system clock is either RC, EC or INTRC, the CPU will begin operating on the first Q1 cycle following the wake-up event. This means that there is no oscillator start-up time required because the primary clock is already stable; however, there is a delay between the wake-up event and the following Q2. An internal delay timer of 5-10  $\mu$ s will suspend operation after the Reset to allow the CPU to become ready for code execution. The CPU and peripheral clock will be held in the first Q1.

The sequence of events is as follows:

- 1. A device Reset is asserted from one of many sources (WDT, BOR, MCLR, etc.).
- 2. The device resets and the CPU start-up timer is enabled if in Sleep mode. The device is held in Reset until the CPU start-up time-out is complete.
- 3. If the primary system clock is configured as an external oscillator (HS, XT, LP), then the OST will be active waiting for 1024 clocks of the primary system clock. While waiting for the OST, the device will be held in Reset. The OST and CPU start-up timers run in parallel.
- After both the CPU start-up and OST timers have timed out, the device will wait for one additional clock cycle and instruction execution will begin.



FIGURE 4-10: PRIMARY SYSTEM CLOCK AFTER RESET (HS, XT, LP)

## 5.2 PORTB and the TRISB Register

PORTB is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISB. Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., put the contents of the output latch on the selected pin).

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit RBPU (OPTION\_REG<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

Four of PORTB's pins, RB7:RB4, have an interrupt-onchange feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB4 pin configured as an output is excluded from the interrupton-change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR'ed together to generate the RB Port Change Interrupt with Flag bit RBIF (INTCON<0>).

This interrupt can wake the device from Sleep. The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

- a) Any read or write of PORTB. This will end the mismatch condition.
- b) Clear flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared.

The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt-on-change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.

RB0/INT is an external interrupt input pin and is configured using the INTEDG bit (OPTION\_REG<6>).

PORTB is multiplexed with several peripheral functions (see Table 5-3). PORTB pins have Schmitt Trigger input buffers.

When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTB pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. Since the TRIS bit override is in effect while the peripheral is enabled, read-modifywrite instructions (BSF, BCF, XORWF) with TRISB as the destination should be avoided. The user should refer to the corresponding peripheral section for the correct TRIS bit settings.



r			
RTCinit	BANKSEL	TMR1H	
	MOVLW	0x80	; Preload TMR1 register pair
	MOVWF	TMR1H	; for 1 second overflow
	CLRF	TMR1L	
	MOVLW	b'00001111'	; Configure for external clock,
	MOVWF	T1CON	; Asynchronous operation, external oscillator
	CLRF	secs	; Initialize timekeeping registers
	CLRF	mins	
	MOVLW	.12	
	MOVWF	hours	
	BANKSEL	PIE1	
	BSF	PIE1, TMR1IE	; Enable Timer1 interrupt
	RETURN		
RTCisr	BANKSEL	TMR1H	
	BSF	TMR1H, 7	; Preload for 1 sec overflow
	BCF	PIR1, TMR1IF	; Clear interrupt flag
	INCF	secs, F	; Increment seconds
	MOVF	secs, w	
	SUBLW	.60	
	BTFSS	STATUS, Z	; 60 seconds elapsed?
	RETURN		; No, done
	CLRF	seconds	; Clear seconds
	INCF	mins, f	; Increment minutes
	MOVF	mins, w	
	SUBLW	.60	
	BTFSS	STATUS, Z	; 60 seconds elapsed?
	RETURN		; No, done
	CLRF	mins	; Clear minutes
	INCF	hours, f	; Increment hours
	MOVF	hours, w	
	SUBLW	.24	
	BTFSS	STATUS, Z	; 24 hours elapsed?
	RETURN		; No, done
	CLRF	hours	; Clear hours
	RETURN		; Done

## EXAMPLE 7-3: IMPLEMENTING A REAL-TIME CLOCK USING A TIMER1 INTERRUPT SERVICE

## TABLE 7-2: REGISTERS ASSOCIATED WITH TIMER1 AS A TIMER/COUNTER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Valu POR,	e on BOR	Valu all c Res	e on other sets
0Bh, 8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INTOIF	RBIF	0000	000x	0000	000u
0Ch	PIR1		ADIF <sup>(1)</sup>	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	-000	0000	-000	0000
8Ch	PIE1		ADIE <sup>(1)</sup>	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	-000	0000	-000	0000
0Eh	TMR1L	Holding	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register							xxxx	xxxx	uuuu	uuuu
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register							er	xxxx	xxxx	uuuu	uuuu
10h	T1CON	—	T1RUN	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	-000	0000	-uuu	uuuu

Legend:x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.Note1:This bit is only implemented on the PIC16F88. The bit will read '0' on the PIC16F87.

## 9.3 PWM Mode

In Pulse-Width Modulation (PWM) mode, the CCP1 pin produces up to a 10-bit resolution PWM output. Since the CCP1 pin is multiplexed with the PORTB data latch, the TRISB<x> bit must be cleared to make the CCP1 pin an output.

Note:	Clearing the CCP1CON register will force
	the CCP1 PWM output latch to the default
	low level. This is not the PORTB I/O data
	latch.

Figure 9-3 shows a simplified block diagram of the CCP module in PWM mode.

For a step-by-step procedure on how to set up the CCP module for PWM operation, see **Section 9.3.3 "Setup for PWM Operation"**.

#### FIGURE 9-3: SIMPLIFIED PWM BLOCK DIAGRAM



A PWM output (Figure 9-4) has a time base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is the inverse of the period (1/period).





## 9.3.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula.

#### **EQUATION 9-1:**

PWM Period = [(PR2) + 1] • 4 • Tosc • (TMR2 Prescale Value)

PWM frequency is defined as 1/[PWM period].

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set (exception: if PWM duty cycle = 0%, the CCP1 pin will not be set)
- The PWM duty cycle is latched from CCPR1L into CCPR1H

Note:	The Timer2 postscaler (see Section 8.0
	"Timer2 Module") is not used in the deter-
	mination of the PWM frequency. The post-
	scaler could be used to have a servo
	update rate at a different frequency than
	the PWM output.

## 9.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the CCPR1L register and to the CCP1CON<5:4> bits. Up to 10-bit resolution is available. The CCPR1L contains the eight MSbs and the CCP1CON<5:4> bits contain the two LSbs. This 10-bit value is represented by CCPR1L:CCP1CON<5:4>. The following equation is used to calculate the PWM duty cycle in time.

## **EQUATION 9-2:**

CCPR1L and CCP1CON<5:4> can be written to at any time, but the duty cycle value is not latched into CCPR1H until after a match between PR2 and TMR2 occurs (i.e., the period is complete). In PWM mode, CCPR1H is a read-only register.

The CCPR1H register and a 2-bit internal latch are used to double-buffer the PWM duty cycle. This double-buffering is essential for glitchless PWM operation.

When the CCPR1H and 2-bit latch match TMR2, concatenated with an internal 2-bit Q clock or 2 bits of the TMR2 prescaler, the CCP1 pin is cleared.

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REGISTER 10-1:	REGISTER 10-1: SSPSTAT: SYNCHRONOUS SERIAL PORT STATUS REGISTER (ADDRESS 94h)								
	R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0	
	SMP	CKE	D/A	P <sup>(1)</sup>	S <sup>(1)</sup>	R/W	UA	BF	
	bit 7							bit 0	
bit 7	SMP: SPI [	Data Input S	ample Phas	e bit					
	SPI Master	mode:							
	1 = Input d	ata sampled	at end of da	ata output tin f data output	1e time (Micro	wira)			
	SPI Slave r	node:				,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,			
	This bit mu	st be cleare	d when SPI	is used in SI	ave mode.				
	I <sup>2</sup> C mode:								
	This bit mu	st be mainta	ained clear.						
bit 6	CKE: SPI (	Clock Edge	Select bit	ana antina ta	امالم ماممار م	4.04.0			
	1 = Transm0 = Transm	nit occurs on	transition fr	om Idle to ad	tive clock s	tate			
	Note:	Polarity of o	clock state is	s set by the C	CKP bit (SS	PCON<4>).			
bit 5	D/A: Data/	Address bit	(I <sup>2</sup> C mode o	nly)					
	In I <sup>2</sup> C Slave mode:								
	1 = Indicate	es that the la	ast byte rece	ived was da	dress				
bit 4	<b>P:</b> Stop bit <sup>(1)</sup> ( $ ^{2}$ C mode only)								
	1 = Indicat 0 = Stop b	es that a Stories tha	op bit has be etected last	en detected	last				
bit 3	S: Start bit	1) (I <sup>2</sup> C mode	e only)						
	1 = Indicat 0 = Start b	es that a Statit it was not de	art bit has be etected last	en detected	last (this bi	t is '0' on Re	eset)		
bit 2	R/W: Read	/Write Inform	nation bit (I <sup>2</sup>	C mode only	<i>'</i> )				
	Holds the F match to th	Holds the $R/W$ bit information following the last address match and is only valid from address match to the next Start bit. Stop bit or $\overline{ACK}$ bit.							
	1 = Read								
	0 = Write								
bit 1	UA: Update	e Address b	it (10-bit I <sup>2</sup> C	mode only)					
	1 = Indicat 0 = Addres	tes that the uses does not	user needs to need to be u	o update the Ipdated	address in	the SSPADI	D register		
bit 0	BF: Buffer	Full Status b	bit						
	Receive (S	PI and I <sup>2</sup> C r	<u>nodes):</u>						
	1 = Receive	e complete, e pot comple	SSPBUF is	full F is empty					
	0 = Receive	n I <sup>2</sup> C mode	only).	is empty					
	1 = Transmit in progress, SSPBUF is full (8 bits)								
	0 = Transm	nit complete,	SSPBUF is	empty					
	Note 1:	This bit is cl	eared when	the SSP mod	lule is disabl	ed (i.e., the S	SSPEN bit is	cleared).	
	Legend:								
	R = Reada	ble bit	W = W	/ritable bit	U = Unin	plemented	bit, read as	0'	

'1' = Bit is set

-n = Value at POR

x = Bit is unknown

'0' = Bit is cleared

BAUD	Fosc = 8 MHz			Fosc = 4 M	Hz	Fosc = 2 MHz Fosc = 1 MHz			IHz			
RATE (K)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
0.3	NA	_	_	0.300	0	207	0.300	0	103	0.300	0	51
1.2	1.202	+0.16	103	1.202	+0.16	51	1.202	+0.16	25	1.202	+0.16	12
2.4	2.404	+0.16	51	2.404	+0.16	25	2.404	+0.16	12	2.232	-6.99	6
9.6	9.615	+0.16	12	8.929	-6.99	6	10.417	+8.51	2	NA	_	_
19.2	17.857	-6.99	6	20.833	+8.51	2	NA	_	_	NA	_	_
28.8	31.250	+8.51	3	31.250	+8.51	1	31.250	+8.51	0	NA	_	_
38.4	41.667	+8.51	2	NA	_	_	NA	_	_	NA	_	_
57.6	62.500	+8.51	1	62.500	8.51	0	NA	_	_	NA	_	_

## TABLE 11-5: INTRC BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 0)

## TABLE 11-6:INTRC BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 1)

BAUD	Fosc = 8 MHz				Fosc = 4 M	Hz		Fosc = 2 N	lHz	Fosc = 1 MHz		
RATE (K)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
0.3	NA	_	_	NA	_	_	NA	_	_	0.300	0	207
1.2	NA	—	_	1.202	+0.16	207	1.202	+0.16	103	1.202	+0.16	51
2.4	2.404	+0.16	207	2.404	+0.16	103	2.404	+0.16	51	2.404	+0.16	25
9.6	9.615	+0.16	51	9.615	+0.16	25	9.615	+0.16	12	8.929	-6.99	6
19.2	19.231	+0.16	25	19.231	+0.16	12	17.857	-6.99	6	20.833	+8.51	2
28.8	29.412	+2.12	16	27.778	-3.55	8	31.250	+8.51	3	31.250	+8.51	1
38.4	38.462	+0.16	12	35.714	-6.99	6	41.667	+8.51	2	NA	_	_
57.6	55.556	-3.55	8	62.500	+8.51	3	62.500	+8.51	1	62.500	+8.51	0

## 11.2 AUSART Asynchronous Mode

In this mode, the AUSART uses standard Non-Returnto-Zero (NRZ) format (one Start bit, eight or nine data bits and one Stop bit). The most common data format is 8 bits. An on-chip, dedicated, 8-bit Baud Rate Generator can be used to derive standard baud rate frequencies from the oscillator. The AUSART transmits and receives the LSb first. The transmitter and receiver are functionally independent, but use the same data format and baud rate. The Baud Rate Generator produces a clock, either x16 or x64 of the bit shift rate, depending on bit BRGH (TXSTA<2>). Parity is not supported by the hardware, but can be implemented in software (and stored as the ninth data bit). Asynchronous mode is stopped during Sleep.

Asynchronous mode is selected by clearing bit SYNC (TXSTA<4>).

The AUSART Asynchronous module consists of the following important elements:

- Baud Rate Generator
- · Sampling Circuit
- Asynchronous Transmitter
- Asynchronous Receiver

### 11.2.1 AUSART ASYNCHRONOUS TRANSMITTER

The AUSART transmitter block diagram is shown in Figure 11-1. The heart of the transmitter is the Transmit (Serial) Shift Register (TSR). The Shift register obtains its data from the Read/Write Transmit Buffer register, TXREG. The TXREG register is loaded with data in software. The TSR register is not loaded until the Stop bit has been transmitted from the previous load. As soon as the Stop bit is transmitted, the TSR is loaded with new data from the TXREG register (if available). Once the TXREG register transfers the data to the TSR register (occurs in one TcY), the TXREG register is empty and flag bit, TXIF (PIR1<4>), is set. This interrupt can be enabled/disabled by setting/clearing enable bit, TXIE (PIE1<4>). Flag bit TXIF will be set, regardless of the state of enable bit TXIE and cannot be cleared in software. It will reset only when new data is loaded into the TXREG register. While flag bit TXIF indicates the status of the TXREG register, another bit, TRMT (TXSTA<1>), shows the status of the TSR register. Status bit TRMT is a read-only bit which is set when the TSR register is empty. No interrupt logic is tied to this bit, so the user has to poll this bit in order to determine if the TSR register is empty.

Note 1:	The TSR register is not mapped in data memory, so it is not available to the user.
2:	Flag bit TXIF is set when enable bit TXEN is set. TXIF is cleared by loading TXREG.

Transmission is enabled by setting enable bit TXEN (TXSTA<5>). The actual transmission will not occur until the TXREG register has been loaded with data and the Baud Rate Generator (BRG) has produced a shift clock (Figure 11-2). The transmission can also be started by first loading the TXREG register and then setting enable bit TXEN. Normally, when transmission is first started, the TSR register is empty. At that point, transfer to the TXREG register will result in an immediate transfer to TSR, resulting in an empty TXREG. A back-to-back transfer is thus possible (Figure 11-3). Clearing enable bit TXEN during a transmission will cause the transmission to be aborted and will reset the transmitter. As a result, the RB5/SS/TX/CK pin will revert to high-impedance.

In order to select 9-bit transmission, transmit bit, TX9 (TXSTA<6>), should be set and the ninth bit should be written to TX9D (TXSTA<0>). The ninth bit must be written before writing the 8-bit data to the TXREG register. This is because a data write to the TXREG register can result in an immediate transfer of the data to the TSR register (if the TSR is empty). In such a case, an incorrect ninth data bit may be loaded in the TSR register.



## FIGURE 11-1: AUSART TRANSMIT BLOCK DIAGRAM

## 12.1 A/D Acquisition Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 12-2. The source impedance (Rs) and the internal sampling switch (Rss) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (Rss) impedance varies over the device voltage (VDD), see Figure 12-2. The maximum recommended impedance for analog sources is 10 k $\Omega$ . As the impedance is decreased, the

# acquisition time may be decreased. After the analog input channel is selected (changed), this acquisition must be done before the conversion can be started.

To calculate the minimum acquisition time, Equation 12-1 may be used. This equation assumes that 1/2 LSb error is used (1024 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

To calculate the minimum acquisition time, TACQ, see the "*PIC*<sup>®</sup> *Mid-Range MCU Family Reference Manual*" (DS33023).

## EQUATION 12-1: ACQUISITION TIME

TACQ	= Amplifier Settling Time + Hold Capacitor Charging Time + Temperature Coefficient
Tc Tacq	= TAMP + TC + TCOFF = $2 \mu s + TC + [(Temperature -25^{\circ}C)(0.05 \mu s/^{\circ}C)]$ = CHOLD (RIC + RSS + RS) In(1/2047) = -120 pF (1 k $\Omega$ + 7 k $\Omega$ + 10 k $\Omega$ ) In(0.0004885) = 16.47 $\mu s$ = $2 \mu s + 16.47 \mu s + [(50^{\circ}C - 25^{\circ}C)(0.05 \mu s/^{\circ}C)]$ = 19.72 $\mu s$

Note 1: The reference voltage (VREF) has no effect on the equation, since it cancels itself out.

- **2:** The charge holding capacitor (CHOLD) is not discharged after each conversion.
- **3:** The maximum recommended impedance for analog sources is 10 k $\Omega$ . This is required to meet the pin leakage specification.
- **4:** After a conversion has completed, a 2.0 TAD delay must complete before acquisition can begin again. During this time, the holding capacitor is not connected to the selected A/D input channel.





## 15.3 MCLR

PIC16F87/88 devices have a noise filter in the MCLR Reset path. The filter will detect and ignore small pulses.

It should be noted that a WDT Reset does not drive MCLR pin low.

The behavior of the ESD protection on the MCLR pin has been altered from previous devices of this family. Voltages applied to the pin that exceed its specification can result in both MCLR and excessive current beyond the device specification during the ESD event. The circuit, as shown in Figure 15-2, is suggested.

Note:	For this reason, Microchip recommends
	that the MCLR pin no longer be tied
	directly to VDD.

The RA5/MCLR/VPP pin can be configured for MCLR (default), or as an I/O pin (RA5). This is configured through the MCLRE bit in Configuration Word 1.





only if the VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.

- 2:  $R < 40 \text{ k}\Omega$  is recommended to make sure that the voltage drop across R does not violate the device's electrical specification.
- 3:  $R1 = 1 \ k\Omega \ to \ 10 \ k\Omega \ will limit any current flow$ ing into MCLR from external capacitor C $(0.1 <math>\mu$ F), in the event of RA5/MCLR/VPP pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

## 15.4 Power-on Reset (POR)

A Power-on Reset pulse is generated on-chip when VDD rise is detected (in the range of 1.2V-1.7V). To take advantage of the POR, tie the MCLR pin to VDD, as described in Section 15.3 "MCLR". A maximum rise time for VDD is specified. See Section 18.0 "Electrical Characteristics" for details.

When the device starts normal operation (exits the Reset condition), device operating parameters (voltage, frequency, temperature,...) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met. For more information, see Application Note, *AN607 "Power-up Trouble Shooting"* (DS00607).

## 15.5 Power-up Timer (PWRT)

The Power-up Timer (PWRT) of the PIC16F87/88 is a counter that uses the INTRC oscillator as the clock input. This yields a count of 72 ms. While the PWRT is counting, the device is held in Reset.

The power-up time delay depends on the INTRC and will vary from chip-to-chip due to temperature and process variation. See DC parameter #33 for details.

The PWRT is enabled by clearing configuration bit PWRTEN.

## 15.6 Oscillator Start-up Timer (OST)

The Oscillator Start-up Timer (OST) provides a 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over (if enabled). This helps to ensure that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from Sleep.

## 15.7 Brown-out Reset (BOR)

The configuration bit, BOREN, can enable or disable the Brown-out Reset circuit. If VDD falls below VBOR (parameter D005, about 4V) for longer than TBOR (parameter #35, about 100  $\mu$ s), the brown-out situation will reset the device. If VDD falls below VBOR for less than TBOR, a Reset may not occur.

Once the brown-out occurs, the device will remain in Brown-out Reset until VDD rises above VBOR. The Power-up Timer (if enabled) will keep the device in Reset for TPWRT (parameter #33, about 72 ms). If VDD should fall below VBOR during TPWRT, the Brown-out Reset process will restart when VDD rises above VBOR with the Power-up Timer Reset. Unlike previous PIC16 devices, the PWRT is no longer automatically enabled when the Brown-out Reset circuit is enabled. The PWRTEN and BOREN configuration bits are independent of each other.

#### TABLE 15-3: RESET CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	000h	0001 1xxx	0x
MCLR Reset during normal operation	000h	000u uuuu	uu
MCLR Reset during Sleep	000h	0001 Ouuu	uu
WDT Reset	000h	0000 luuu	uu
WDT Wake-up	PC + 1	uuu0 0uuu	uu
Brown-out Reset	000h	0001 luuu	u0
Interrupt Wake-up from Sleep	PC + 1 <sup>(1)</sup>	uuul Ouuu	uu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0'

**Note 1:** When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

Register	Power-on Reset, Brown-out Reset	MCLR Reset, WDT Reset	Wake-up via WDT or Interrupt
W	xxxx xxxx	uuuu uuuu	սսսս սսսս
INDF	N/A	N/A	N/A
TMR0	XXXX XXXX	uuuu uuuu	սսսս սսսս
PCL	0000h	0000h	PC + 1 <sup>(2)</sup>
STATUS	0001 1xxx	000q quuu <sup>(3)</sup>	uuuq quuu <b>(3)</b>
FSR	xxxx xxxx	սսսս սսսս	սսսս սսսս
PORTA (PIC16F87) PORTA (PIC16F88)	xxxx 0000 xxx0 0000	uuuu 0000 uuu0 0000	uuuu uuuu uuuu uuuu
PORTB (PIC16F87) PORTB (PIC16F87)	xxxx xxxx 00xx xxxx	uuuu uuuu 00uu uuuu	นนนน นนนน นนนน นนนน
PCLATH	0 0000	0 0000	u uuuu
INTCON	0000 000x	0000 000u	uuuu uuuu <b>(1)</b>
PIR1	-000 0000	-000 0000	-uuu uuuu <b>(1)</b>
PIR2	00-0	00-0	uu-u <b>(1)</b>
TMR1L	xxxx xxxx	սսսս սսսս	սսսս սսսս
TMR1H	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	-000 0000	-uuu uuuu	-uuu uuuu
TMR2	0000 0000	0000 0000	uuuu uuuu
T2CON	-000 0000	-000 0000	-uuu uuuu
SSPBUF	xxxx xxxx	uuuu uuuu	uuuu uuuu
SSPCON	0000 0000	0000 0000	uuuu uuuu
CCPR1L	XXXX XXXX	uuuu uuuu	uuuu uuuu
CCPR1H	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1CON	00 0000	00 0000	uu uuuu
RCSTA	0000 000x	0000 000x	սսսս սսսս

#### TABLE 15-4: INITIALIZATION CONDITIONS FOR ALL REGISTERS

 $\label{eq:logend: u = unchanged, x = unknown, - = unimplemented bit, read as `0', q = value depends on condition$ 

Note 1: One or more bits in INTCON, PIR1 and PR2 will be affected (to cause wake-up).

**2:** When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

**3:** See Table 15-3 for Reset value for specific condition.

#### 15.12.3 TWO-SPEED CLOCK START-UP MODE

Two-Speed Start-up mode minimizes the latency between oscillator start-up and code execution that may be selected with the IESO (Internal/External Switchover) bit in Configuration Word 2. This mode is achieved by initially using the INTRC for code execution until the primary oscillator is stable.

If this mode is enabled and any of the following conditions exist, the system will begin execution with the INTRC oscillator. This results in almost immediate code execution with a minimum of delay.

- <u>POR and after the Power-up Timer has expired (if</u> <u>PWRTEN = 0);</u>
- or following a wake-up from Sleep;
- or a Reset when running from T1OSC or INTRC (after a Reset, SCS<1:0> are always set to '00').

Note:	Following any Reset, the IRCF bits are zeroed and the frequency selection is
	forced to 31.25 kHz. The user can modify
	the IRCF bits to select a higher internal
	oscillator frequency.

If the primary oscillator is configured to be anything other than XT, LP or HS, then Two-Speed Start-up mode is disabled because the primary oscillator will not require any time to become stable after POR, or an exit from Sleep.

If the IRCF bits of the OSCCON register are configured to a non-zero value prior to entering Sleep mode, the system clock frequency will come from the output of the INTOSC. The IOFS bit in the OSCCON register will be clear until the INTOSC is stable. This will allow the user to determine when the internal oscillator can be used for time critical applications. Checking the state of the OSTS bit will confirm whether the primary clock configuration is engaged. If not, the OSTS bit will remain clear.

When the device is auto-configured in INTRC mode following a POR or wake-up from Sleep, the rules for entering other oscillator modes still apply, meaning the SCS<1:0> bits in OSCCON can be modified before the OST time-out has occurred. This would allow the application to wake-up from Sleep, perform a few instructions using the INTRC as the clock source and go back to Sleep without waiting for the primary oscillator to become stable.

**Note:** Executing a SLEEP instruction will abort the oscillator start-up time and will cause the OSTS bit to remain clear.

- 15.12.3.1 Two-Speed Start-up Mode Sequence
- 1. Wake-up from Sleep, Reset or POR.
- OSCCON bits configured to run from INTRC (31.25 kHz).
- Instructions begin execution by INTRC (31.25 kHz).
- 4. OST enabled to count 1024 clock cycles.
- 5. OST timed out, wait for falling edge of INTRC.
- 6. OSTS is set.
- 7. System clock held low for eight falling edges of new clock (LP, XT or HS).
- 8. System clock is switched to primary source (LP, XT or HS).

The software may read the OSTS bit to determine when the switchover takes place so that any software timing edges can be adjusted.



# PIC16F87/88

SUBLW	Subtract W from Literal	XORLW	Exclusive OR Literal with W			
Syntax:	[ <i>label</i> ] SUBLW k	Syntax:	[ <i>label</i> ] XORLW k			
Operands:	$0 \leq k \leq 255$	Operands:	$0 \le k \le 255$			
$Prevention:   k - (W) \to (W)$		Operation:	(W) .XOR. $k \rightarrow (W)$			
Status Affected:	C, DC, Z	Status Affected:	Z			
Description:	The W register is subtracted (two's complement method) from the eight-bit literal 'k'. The result is placed in the W register.	Description:	The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed ir the W register.			

SUBWF	Subtract W from f	XORWF	Exclusive OR W with f
Syntax:	[ <i>label</i> ] SUBWF f,d	Syntax:	[ label ] XORWF f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d  \in  [0,1] \end{array}$	Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$
Operation:	(f) – (W) $\rightarrow$ (destination)	Operation:	(W) .XOR. (f) $\rightarrow$ (destination)
Status Affected:	C, DC, Z	Status Affected:	Z
Description:	Subtract (two's complement method) W register from register 'f'. If 'd' = 0, the result is stored in the W register. If 'd' = 1, the result is stored back in register 'f'.	Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' = 0, the result is stored in the W register. If 'd' = 1, the result is stored back in register 'f'.

SWAPF	Swap Nibbles in f
Syntax:	[label] SWAPF f,d
Operands:	$\begin{array}{l} 0\leq f\leq 127\\ d\in [0,1] \end{array}$
Operation:	$(f<3:0>) \rightarrow (destination<7:4>), (f<7:4>) \rightarrow (destination<3:0>)$
Status Affected:	None
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' = 0, the result is placed in W register. If 'd' = 1, the result is placed in register 'f'.

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## 17.0 DEVELOPMENT SUPPORT

The PIC<sup>®</sup> microcontrollers and dsPIC<sup>®</sup> digital signal controllers are supported with a full range of software and hardware development tools:

- Integrated Development Environment
- MPLAB<sup>®</sup> IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB C Compiler for Various Device Families
  - HI-TECH C<sup>®</sup> for Various Device Families
  - MPASM<sup>™</sup> Assembler
  - MPLINK<sup>™</sup> Object Linker/ MPLIB<sup>™</sup> Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers
  - MPLAB ICD 3
  - PICkit<sup>™</sup> 3 Debug Express
- Device Programmers
  - PICkit<sup>™</sup> 2 Programmer
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits, and Starter Kits

## 17.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16/32-bit microcontroller market. The MPLAB IDE is a Windows<sup>®</sup> operating system-based application that contains:

- A single graphical interface to all debugging tools
  - Simulator
  - Programmer (sold separately)
  - In-Circuit Emulator (sold separately)
  - In-Circuit Debugger (sold separately)
- · A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either C or assembly)
- One-touch compile or assemble, and download to emulator and simulator tools (automatically updates all project information)
- Debug using:
  - Source files (C or assembly)
  - Mixed C and assembly
  - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

## 18.4 DC Characteristics: PIC16F87/88 (Industrial, Extended) PIC16LF87/88 (Industrial)

DC CH	ARACT	ERISTICS	$\begin{array}{llllllllllllllllllllllllllllllllllll$				
Param No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
	VIL	Input Low Voltage					
		I/O ports:					
D030		with TTL buffer	Vss	_	0.15 Vdd	V	For entire VDD range
D030A			Vss	—	0.8V	V	$4.5V \leq V\text{DD} \leq 5.5V$
D031		with Schmitt Trigger buffer	Vss	—	0.2 Vdd	V	
D032		MCLR, OSC1 (in RC mode)	Vss	_	0.2 Vdd	V	(Note 1)
D033		OSC1 (in XT and LP mode)	Vss	_	0.3V	V	
		OSC1 (in HS mode)	Vss	—	0.3 Vdd	V	
		Ports RB1 and RB4:					
D034		with Schmitt Trigger buffer	Vss	_	0.3 Vdd	V	For entire VDD range
	Vih	Input High Voltage			-	-	-
		I/O ports:					
D040		with TTL buffer	2.0	—	Vdd	V	$4.5V \leq V\text{DD} \leq 5.5V$
D040A			0.25 VDD + 0.8V	—	Vdd	V	For entire VDD range
D041		with Schmitt Trigger buffer	0.8 Vdd	_	Vdd	V	For entire VDD range
D042		MCLR	0.8 Vdd	_	Vdd	V	
D042A		OSC1 (in XT and LP mode)	1.6V	—	Vdd	V	
		OSC1 (in HS mode)	0.7 Vdd	—	Vdd	V	
D043		OSC1 (in RC mode)	0.9 Vdd		Vdd	V	(Note 1)
		Ports RB1 and RB4:					
D044		with Schmitt Trigger buffer	0.7 Vdd	_	Vdd	V	For entire VDD range
D070	Ipurb	PORTB Weak Pull-up Current	50	250	400	μA	VDD = 5V, VPIN = VSS
	lı∟	Input Leakage Current (Notes	2, 3)		-		
D060		I/O ports	—	—	±1	μA	Vss $\leq$ VPIN $\leq$ VDD, pin at high-impedance
D061		MCLR	—	_	±5	μA	$Vss \leq VPIN \leq VDD$
D063		OSC1	_	_	±5	μA	Vss $\leq$ VPIN $\leq$ VDD, XT, HS and LP oscillator configuration

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** In RC oscillator configuration, the OSC1/CLKI pin is a Schmitt Trigger input. It is not recommended that the PIC16F87/88 be driven with external clock in RC mode.

- 2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- **3:** Negative current is defined as current sourced by the pin.

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
100*	Тнідн	Clock High Time	100 kHz mode	4.0		μs	
			400 kHz mode	0.6		μS	
			SSP Module	1.5 TCY			
101*	TLOW	Clock Low Time	100 kHz mode	4.7		μs	
			400 kHz mode	1.3	_	μs	
			SSP Module	1.5 TCY	_		
102*	TR	SDA and SCL Rise Time	100 kHz mode	—	1000	ns	
			400 kHz mode	20 + 0.1 Св	300	ns	CB is specified to be from 10-400 pF
103*	TF	SDA and SCL Fall Time	100 kHz mode	—	300	ns	
			400 kHz mode	20 + 0.1 CB	300	ns	CB is specified to be from 10-400 pF
90*	Tsu:sta	Start Condition Setup Time	100 kHz mode	4.7	_	μs	Only relevant for Repeated Start condition
			400 kHz mode	0.6		μs	
91*	THD:STA	Start Condition Hold Time	100 kHz mode	4.0		μS	After this period, the first clock pulse is generated
			400 kHz mode	0.6		μs	
106*	THD:DAT	Data Input Hold Time	100 kHz mode	0		ns	
			400 kHz mode	0	0.9	μS	
107*	TSU:DAT	Data Input Setup Time	100 kHz mode	250		ns	(Note 2)
			400 kHz mode	100	_	ns	
92*	Tsu:sto	Stop Condition Setup Time	100 kHz mode	4.7		μS	
			400 kHz mode	0.6		μS	
109*	ΤΑΑ	Output Valid from Clock	100 kHz mode	—	3500	ns	(Note 1)
			400 kHz mode	_		ns	
110*	TBUF	Bus Free Time	100 kHz mode	4.7		μS	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μS	
	Св	Bus Capacitive Loading		—	400	pF	

## TABLE 18-10: I<sup>2</sup>C<sup>™</sup> BUS DATA REQUIREMENTS

\* These parameters are characterized but not tested.

**Note 1:** As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

2: A Fast mode (400 kHz) I<sup>2</sup>C<sup>™</sup> bus device can be used in a Standard mode (100 kHz) I<sup>2</sup>C bus system, but the requirement, TsU:DAT ≥ 250 ns, must then be met. This will automatically be the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line, TR max. + TsU:DAT = 1000 + 250 = 1250 ns (according to the Standard mode I<sup>2</sup>C bus specification), before the SCL line is released.



FIGURE 19-17: IPD A/D, -40°C TO +125°C, SLEEP MODE, A/D ENABLED (NOT CONVERTING)



