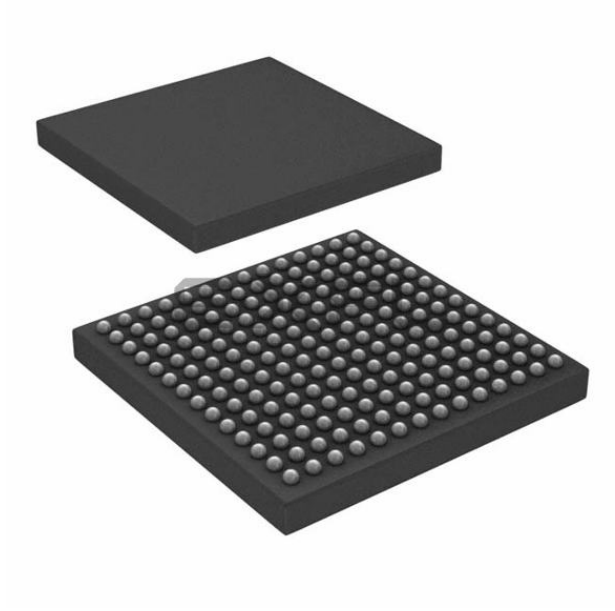

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Floating Point
Interface	Host Interface, Serial Port
Clock Rate	60MHz
Non-Volatile Memory	External
On-Chip RAM	64kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 100°C (TC)
Mounting Type	Surface Mount
Package / Case	196-BGA, CSPBGA
Supplier Device Package	196-CSPBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21065lcca-240

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

544 Kbits Configurable On-Chip SRAM

Dual-Ported for Independent Access by Core Processor and DMA

Configurable in Combinations of 16-, 32-, 48-Bit Data and Program Words in Block 0 and Block 1

DMA Controller

Ten DMA Channels—Two Dedicated to the External Port and Eight Dedicated to the Serial Ports

Background DMA Transfers at up to 66 MHz, in Parallel with Full Speed Processor Execution

Performs Transfers Between:

- **Internal RAM and Host**
- **Internal RAM and Serial Ports**
- **Internal RAM and Master or Slave SHARC**
- **Internal RAM and External Memory or I/O Devices**
- **External Memory and External Devices**

Host Processor Interface

Efficient Interface to 8-, 16-, and 32-Bit Microprocessors

Host Can Directly Read/Write ADSP-21065L IOP Registers

Multiprocessing

Distributed On-Chip Bus Arbitration for Glueless, Parallel Bus Connect Between Two ADSP-21065Ls Plus Host

132 Mbytes/s Transfer Rate Over Parallel Bus

Serial Ports

Independent Transmit and Receive Functions

Programmable 3-Bit to 32-Bit Serial Word Width

I^2S Support Allowing Eight Transmit and Eight Receive Channels

Glueless Interface to Industry Standard Codecs

TDM Multichannel Mode with μ-Law/A-Law Hardware Companding

Multichannel Signaling Protocol

GENERAL DESCRIPTION

The ADSP-21065L is a powerful member of the SHARC family of 32-bit processors optimized for cost sensitive applications. The SHARC—Super Harvard Architecture—offers the highest levels of performance and memory integration of any 32-bit DSP in the industry—they are also the only DSP in the industry that offer both fixed and floating-point capabilities, without compromising precision or performance.

The ADSP-21065L is fabricated in a high speed, low power CMOS process, 0.35 µm technology. With its on-chip instruction cache, the processor can execute every instruction in a single cycle. Table I lists the performance benchmarks for the ADSP-21065L.

The ADSP-21065L SHARC combines a floating-point DSP core with integrated, on-chip system features, including a 544 Kbit SRAM memory, host processor interface, DMA controller, SDRAM controller, and enhanced serial ports.

Figure 1 shows a block diagram of the ADSP-21065L, illustrating the following architectural features:

- Computation Units (ALU, Multiplier, and Shifter) with a Shared Data Register File
- Data Address Generators (DAG1, DAG2)
- Program Sequencer with Instruction Cache
- Timers with Event Capture Modes
- On-Chip, dual-ported SRAM
- External Port for Interfacing to Off-Chip Memory and Peripherals
- Host Port and SDRAM Interface
- DMA Controller
- Enhanced Serial Ports
- JTAG Test Access Port

Table I. Performance Benchmarks

Benchmark	Timing	Cycles
Cycle Time	15.00 ns	1
1024-Pt. Complex FFT (Radix 4, with Digit Reverse)	0.274 ns	18221
Matrix Multiply (Pipelined)		
$[3 \times 3] \times [3 \times 1]$	135 ns	9
$[4 \times 4] \times [4 \times 1]$	240 ns	16
FIR Filter (per Tap)	15 ns	1
IIR Filter (per Biquad)	60 ns	4
Divide Y/X	90 ns	6
Inverse Square Root ($1/\sqrt{x}$)	135 ns	9
DMA Transfers	264 Mbytes/sec.	

ADSP-21000 FAMILY CORE ARCHITECTURE

The ADSP-21065L is code and function compatible with the ADSP-21060/ADSP-21061/ADSP-21062. The ADSP-21065L includes the following architectural features of the SHARC family core.

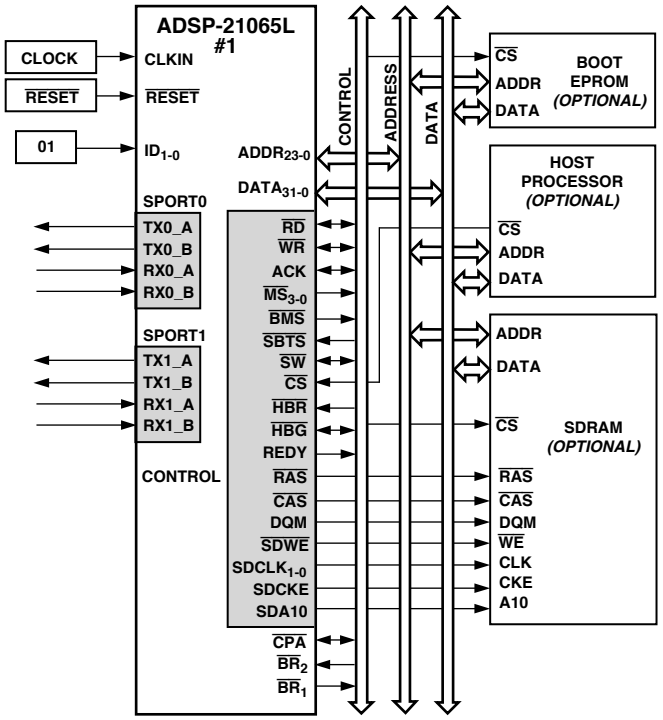


Figure 2. ADSP-21065L Single-Processor System

Independent, Parallel Computation Units
The arithmetic/logic unit (ALU), multiplier, and shifter all perform single-cycle instructions. The three units are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. These computation units support IEEE 32-bit single-precision floating-point, extended precision 40-bit floating-point, and 32-bit fixed-point data formats.

Data Register File
A general-purpose data register file is used for transferring data between the computation units and the data buses, and for storing intermediate results. This 10-port, 32-register (16 primary, 16 secondary) register file, combined with the ADSP-21000 Harvard architecture, allows unconstrained data flow between computation units and internal memory.

Single-Cycle Fetch of Instruction and Two Operands
The ADSP-21065L features an enhanced Super Harvard Architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (see Figure 1). With its separate program and data memory buses, and on-chip instruction cache, the processor can simultaneously fetch two operands and an instruction (from the cache), all in a single cycle.

Instruction Cache
The ADSP-21065L includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and two data values. The cache is selective—only the instructions that fetches conflict with PM bus data accesses are cached. This allows full-speed execution of core, looped operations such as digital filter multiply-accumulates and FFT butterfly processing.

Data Address Generators with Hardware Circular Buffers
The ADSP-21065L's two data address generators (DAGs) implement circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data

I/O transfers). Programs can be downloaded to the ADSP-21065L using DMA transfers. Asynchronous off-chip peripherals can control two DMA channels using DMA Request/Grant lines ($\overline{DMAR}_{1-2}$, $\overline{DMAG}_{1-2}$). Other DMA features include interrupt generation on completion of DMA transfers and DMA chaining for automatically linked DMA transfers.

Serial Ports
The ADSP-21065L features two synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices. The serial ports can operate at 1x clock frequency, providing each with a maximum data rate of 33 Mbit/s. Each serial port has a primary and a secondary set of transmit and receive channels. Independent transmit and receive functions provide greater flexibility for serial communications. Serial port data can be automatically transferred to and from on-chip memory via DMA. Each of the serial ports supports three operation modes: DSP serial port mode, I^2S mode (an interface commonly used by audio codecs), and TDM (Time Division Multiplex) multichannel mode.

The serial ports can operate with little-endian or big-endian transmission formats, with selectable word lengths of 3 bits to 32 bits. They offer selectable synchronization and transmit modes and optional μ-law or A-law companding. Serial port clocks and frame syncs can be internally or externally generated. The serial ports also include keyword and keymask features to enhance interprocessor communication.

Programmable Timers and General-Purpose I/O Ports
The ADSP-21065L has two independent timer blocks, each of which performs two functions—Pulsewidth Generation and Pulse Count and Capture.

In Pulsewidth Generation mode, the ADSP-21065L can generate a modulated waveform with an arbitrary pulsewidth within a maximum period of 71.5 secs.

In Pulse Counter mode, the ADSP-21065L can measure either the high or low pulsewidth and the period of an input waveform.

The ADSP-21065L also contains twelve programmable, general purpose I/O pins that can function as either input or output. As output, these pins can signal peripheral devices; as input, these pins can provide the test for conditional branching.

Program Booting
The internal memory of the ADSP-21065L can be booted at system power-up from an 8-bit EPROM, a host processor, or external memory. Selection of the boot source is controlled by the $\overline{BMS}$ (Boot Memory Select) and BSEL (EPROM Boot) pins. Either 8-, 16-, or 32-bit host processors can be used for booting. For details, see the descriptions of the $\overline{BMS}$ and BSEL pins in the Pin Descriptions section of this data sheet.

Multiprocessing
The ADSP-21065L offers powerful features tailored to multiprocessing DSP systems. The unified address space allows direct interprocessor accesses of both ADSP-21065L's IOP registers. Distributed bus arbitration logic is included on-chip for simple, glueless connection of systems containing a maximum of two ADSP-21065Ls and a host processor. Master processor changeover incurs only one cycle of overhead. Bus lock allows indivisible read-modify-write sequences for semaphores. A vector interrupt is provided for interprocessor commands. Maximum throughput for interprocessor data transfer is 132 Mbytes/sec over the external port.

DEVELOPMENT TOOLS
The ADSP-21065L is supported with a complete set of software and hardware development tools, including the EZ-ICE® In-Circuit Emulator and development software.

The same EZ-ICE hardware that you use for the ADSP-21060/ ADSP-21062 also fully emulates the ADSP-21065L.

Both the SHARC Development Tools family and the VisualDSP® integrated project management and debugging environment support the ADSP-21065L. The VisualDSP project management environment enables you to develop and debug an application from within a single integrated program.

The SHARC Development Tools include an easy to use Assembler that is based on an algebraic syntax; an Assembly library/ librarian; a linker; a loader; a cycle-accurate, instruction-level simulator; a C compiler; and a C run-time library that includes DSP and mathematical functions.

Debugging both C and Assembly programs with the Visual DSP debugger, you can:

- View Mixed C and Assembly Code
- Insert Break Points
- Set Watch Points
- Trace Bus Activity
- Profile Program Execution
- Fill and Dump Memory
- Create Custom Debugger Windows

The Visual IDE enables you to define and manage multiuser projects. Its dialog boxes and property pages enable you to configure and manage all of the SHARC Development Tools. This capability enables you to:

- Control how the development tools process inputs and generate outputs.
- Maintain a one-to-one correspondence with the tool's command line switches.

The EZ-ICE Emulator uses the IEEE 1149.1 JTAG test access port of the ADSP-21065L processor to monitor and control the target board processor during emulation. The EZ-ICE provides full-speed emulation, allowing inspection and modification of memory, registers, and processor stacks. Nonintrusive in-circuit emulation is assured by the use of the processor's JTAG interface—the emulator does not affect target system loading or timing.

In addition to the software and hardware development tools available from Analog Devices, third parties provide a wide range of tools supporting the SHARC processor family. Hardware tools include SHARC PC plug-in cards multiprocessor SHARC VME boards, and daughter and modules with multiple SHARCs and additional memory. These modules are based on the SHARCPAC™ module specification. Third Party software tools include an Ada compiler, DSP libraries, operating systems, and block diagram design tools.

Additional Information
For detailed information on the ADSP-21065L instruction set and architecture, see the *ADSP-21065L SHARC User's Manual*, Third Edition, and the *ADSP-21065L SHARC Technical Reference.*

Pin	Type	Function
$\overline{HBR}$	I/A	**Host Bus Request.** Must be asserted by a host processor to request control of the ADSP-21065L's external bus. When $\overline{HBR}$ is asserted in a multiprocessing system, the ADSP-21065L that is bus master will relinquish the bus and assert $\overline{HBG}$. To relinquish the bus, the ADSP-21065L places the address, data, select, and strobe lines in a high impedance state. It does, however, continue to drive the SDRAM control pins. $\overline{HBR}$ has priority over all ADSP-21065L bus requests ($\overline{BR}_{2-1}$) in a multiprocessor system.
$\overline{HBG}$	I/O	**Host Bus Grant**. Acknowledges an $\overline{HBR}$ bus request, indicating that the host processor may take control of the external bus. $\overline{HBG}$ is asserted by the ADSP-21065L until $\overline{HBR}$ is released. In a multiprocessor system, $\overline{HBG}$ is output by the ADSP-21065L bus master.
$\overline{CS}$	I/A	**Chip Select.** Asserted by host processor to select the ADSP-21065L.
REDY (O/D)	O	**Host Bus Acknowledge.** The ADSP-21065L deasserts REDY to add wait states to an asynchronous access of its internal memory or IOP registers by a host. Open drain output (O/D) by default; can be programmed in ADREDY bit of SYSCON register to be active drive (A/D). REDY will only be output if the $\overline{CS}$ and $\overline{HBR}$ inputs are asserted.
$\overline{DMAR}_1$	I/A	**DMA Request 1** (DMA Channel 9).
$\overline{DMAR}_2$	I/A	**DMA Request 2** (DMA Channel 8).
$\overline{DMAG}_1$	O/T	**DMA Grant 1** (DMA Channel 9).
$\overline{DMAG}_2$	O/T	**DMA Grant 2** (DMA Channel 8).
$\overline{BR}_{2-1}$	I/O/S	**Multiprocessing Bus Requests.** Used by multiprocessing ADSP-21065Ls to arbitrate for bus mastership. An ADSP-21065L drives its own $\overline{BR}$x line (corresponding to the value of its ID_{2-0} inputs) only and monitors all others. In a uniprocessor system, tie both $\overline{BR}$x pins to VDD.
ID_{1-0}	I	**Multiprocessing ID.** Determines which multiprocessor bus request ($\overline{BR}_1$–$\overline{BR}_2$) is used by ADSP-21065L. ID = 01 corresponds to $\overline{BR}_1$, ID = 10 corresponds to $\overline{BR}_2$. ID = 00 in single-processor systems. These lines are a system configuration selection which should be hard-wired or changed only at reset.
$\overline{CPA}$ (O/D)	I/O	**Core Priority Access.** Asserting its $\overline{CPA}$ pin allows the core processor of an ADSP-21065L bus slave to interrupt background DMA transfers and gain access to the external bus. $\overline{CPA}$ is an open drain output that is connected to both ADSP-21065Ls in the system. The $\overline{CPA}$ pin has an internal 5 kΩ pull-up resistor. If core access priority is not required in a system, leave the $\overline{CPA}$ pin unconnected.
DTxX	O	**Data Transmit** (Serial Ports 0, 1; Channels A, B). Each DTxX pin has a 50 kΩ internal pull-up resistor.
DRxX	I	**Data Receive** (Serial Ports 0, 1; Channels A, B). Each DRxX pin has a 50 kΩ internal pull-up resistor.
TCLKx	I/O	**Transmit Clock** (Serial Ports 0, 1). Each TCLK pin has a 50 kΩ internal pull-up resistor.
RCLKx	I/O	**Receive Clock** (Serial Ports 0, 1). Each RCLK pin has a 50 kΩ internal pull-up resistor.
TFSx	I/O	**Transmit Frame Sync** (Serial Ports 0, 1).
RFSx	I/O	**Receive Frame Sync** (Serial Ports 0, 1).
BSEL	I	**EPROM Boot Select.** When BSEL is high, the ADSP-21065L is configured for booting from an 8-bit EPROM. When BSEL is low, the BSEL and $\overline{BMS}$ inputs determine booting mode. See $\overline{BMS}$ for details. This signal is a system configuration selection which should be hardwired.

POWER DISSIPATION ADSP-21065L

These specifications apply to the internal power portion of V_{DD} only. See the Power Dissipation section of this data sheet for calculation of external supply current and total supply current. For a complete discussion of the code used to measure power dissipation, see the technical note SHARC Power Dissipation Measurements.

Specifications are based on the following operating scenarios:

Table II. Internal Current Measurements

Operation	Peak Activity ($I_{DDINPEAK}$)	High Activity ($I_{DDINHIGH}$)	Low Activity ($I_{DDINLOW}$)
Instruction Type	Multifunction	Multifunction	Single Function
Instruction Fetch	Cache	Internal Memory	Internal Memory
Core Memory Access	2 per Cycle (DM and PM)	1 per Cycle (DM)	None
Internal Memory DMA	1 per Cycle	1 per 2 Cycles	1 per 2 Cycles

To estimate power consumption for a specific application, use the following equation where % is the amount of time your program spends in that state:

$\%PEAK \times I_{DDINPEAK} + \%HIGH \times I_{DDINHIGH} + \%LOW \times I_{DDINLOW} + \%IDLE \times I_{DDIDLE} = POWER\ CONSUMPTION$
(See note 4 below Table III.)

OR $\%PEAK \times I_{DDINPEAK} + \%HIGH \times I_{DDINHIGH} + \%LOW \times I_{DDINLOW} + \%IDLE16 \times I_{DDIDLE16} = POWER\ CONSUMPTION$
(See note 5 below Table III.)

Table III. Internal Current Measurement Scenarios

Parameter		Test Conditions	Max	Unit
$I_{DDINPEAK}$	Supply Current (Internal)[1]	t_{CK} = 33 ns, V_{DD} = max	470	mA
		t_{CK} = 30 ns, V_{DD} = max	510	mA
$I_{DDINHIGH}$	Supply Current (Internal)[2]	t_{CK} = 33 ns, V_{DD} = max	275	mA
		t_{CK} = 30 ns, V_{DD} = max	300	mA
$I_{DDINLOW}$	Supply Current (Internal)[3]	t_{CK} = 33 ns, V_{DD} = max	240	mA
		t_{CK} = 30 ns, V_{DD} = max	260	mA
I_{DDIDLE}	Supply Current (IDLE)[4]	t_{CK} = 33 ns, V_{DD} = max	150	mA
		t_{CK} = 30 ns, V_{DD} = max	155	mA
$I_{DDIDLE16}$	Supply Current (IDLE16)[5]	V_{DD} = max	50	mA

NOTES
[1]The test program used to measure $I_{DDINPEAK}$ represents worst-case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified.
[2]$I_{DDINHIGH}$ is a composite average based on a range of high activity code.
[3]$I_{DDINLOW}$ is a composite average based on a range of low activity code.
[4]IDLE denotes ADSP-21065L state during execution of IDLE instruction.
[5]IDLE16 denotes ADSP-21065L state during execution of IDLE16 instruction.

TIMING SPECIFICATIONS

General Notes

Two speed grades of the ADSP-21065L are offered, 60 MHz and 66 MHz instruction rates. The specifications shown are based on a CLKIN frequency of 30 MHz (t_{CK} = 33.3 ns). The DT derating allows specifications at other CLKIN frequencies (within the min–max range of the t_{CK} specification; see Clock Input below). DT is the difference between the actual CLKIN period and a CLKIN period of 33.3 ns:

$$DT = (t_{CK} - 33.3)/32$$

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add parameters to derive longer times.

See Figure 27 in Equivalent Device Loading for AC Measurements (Includes All Fixtures) for voltage reference levels.

Switching Characteristics specify how the processor changes its signals. You have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell you what the processor will do in a given circumstance. You can also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing Requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

(O/D) = Open Drain
(A/D) = Active Drive

Parameter		66 MHz Min	66 MHz Max	60 MHz Min	60 MHz Max	Unit
Clock Input						
Timing Requirements:						
t_{CK}	CLKIN Period	30.00	100	33.33	100	ns
t_{CKL}	CLKIN Width Low	7.0		7.0		ns
t_{CKH}	CLKIN Width High	5.0		5.0		ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V–2.0 V)		3.0		3.0	ns

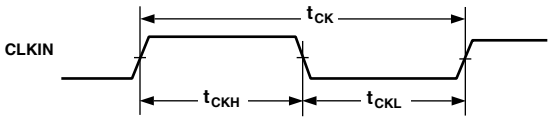


Figure 7. Clock Input

Parameter		Min	Max	Unit
Reset				
Timing Requirements:				
t_{WRST}	$\overline{\text{RESET}}$ Pulsewidth Low[1]	2 t_{CK}		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN High[2]	23.5 + 24 DT	t_{CK}	ns

NOTES
[1]Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 3000 CLKIN cycles while $\overline{\text{RESET}}$ is low, assuming stable V_{DD} and CLKIN (not including start-up time of external clock oscillator).
[2]Only required if multiple ADSP-2106xs must come out of reset synchronous to CLKIN with program counters (PC) equal (i.e., for a SIMD system). Not required for multiple ADSP-2106xs communicating over the shared bus (through the external port), because the bus arbitration logic synchronizes itself automatically after reset.

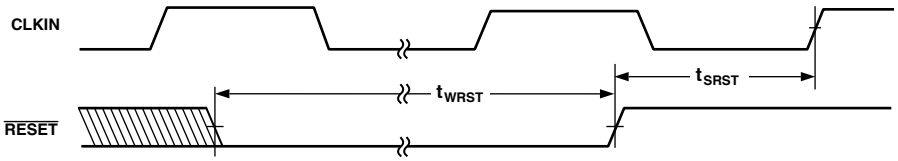


Figure 8. Reset

Parameter		Min	Max	Unit
Interrupts				
Timing Requirements:				
t_{SIR}	$\overline{\text{IRQ}}$2-0 Setup Before CLKIN High or Low[1]	11.0 + 12 DT		ns
t_{HIR}	$\overline{\text{IRQ}}$2-0 Hold Before CLKIN High or Low[1]		0.0 + 12 DT	ns
t_{IPW}	$\overline{\text{IRQ}}$2-0 Pulsewidth[2]	2.0 + t_{CK}/2		ns

NOTES
[1]Only required for $\overline{\text{IRQ}}$x recognition in the following cycle.
[2]Applies only if t_{SIR} and t_{HIR} requirements are not met.

Synchronous Read/Write—Bus Master

Use these specifications for interfacing to external memory systems that require CLKIN-relative timing or for accessing a slave ADSP-21065L (in multiprocessor memory space). These synchronous switching characteristics are also valid during asynchronous memory reads and writes (see Memory Read—Bus Master and Memory Write—Bus Master).

When accessing a slave ADSP-21065L, these switching characteristics must meet the slave's timing requirements for synchronous read/writes (see Synchronous Read/Write—Bus Slave). The slave ADSP-21065L must also meet these (bus master) timing requirements for data and acknowledge setup and hold times.

Parameter		Min	Max	Unit
Timing Requirements:				
t_{SSDATI}	Data Setup Before CLKIN	0.25 + 2 DT		ns
t_{HSDATI}	Data Hold After CLKIN	4.0 – 2 DT		ns
t_{DAAK}	ACK Delay After Address, $\overline{MS}$x, $\overline{SW}$, $\overline{BMS}$[1, 2]		24.0 + 30 DT + W	ns
t_{SACKC}	ACK Setup Before CLKIN[1]	2.75 + 4 DT		ns
t_{HACK}	ACK Hold After CLKIN	2.0 – 4 DT		ns
Switching Characteristics:				
t_{DADRO}	Address, $\overline{MS}$x, $\overline{BMS}$, $\overline{SW}$ Delay After CLKIN[1]		7.0 – 2 DT	ns
t_{HADRO}	Address, $\overline{MS}$x, $\overline{BMS}$, $\overline{SW}$ Hold After CLKIN	0.5 – 2 DT		ns
t_{DRDO}	$\overline{RD}$ High Delay After CLKIN	0.5 – 2 DT	6.0 – 2 DT	ns
t_{DWRO}	$\overline{WR}$ High Delay After CLKIN	0.0 – 3 DT	6.0 – 3 DT	ns
t_{DRWL}	$\overline{RD}$/$\overline{WR}$ Low Delay After CLKIN	7.5 + 4 DT	11.75 + 4 DT	ns
t_{DDATO}	Data Delay After CLKIN		22.0 + 10 DT	ns
t_{DATTR}	Data Disable After CLKIN[3]	1.0 – 2 DT	7.0 – 2 DT	ns
t_{DBM}	BMSTR Delay After CLKIN		3.0	ns
t_{HBM}	BMSTR Hold After CLKIN	–4.0		ns

W = (number of wait states specified in WAIT register) × t_{CK}.

NOTES

[1]Data Hold: User must meet t_{HDA} or t_{HDRH} or synchronous specification t_{HDATI}. See system hold time calculation under test conditions for the calculation of hold times given capacitive and dc loads.

[2]ACK is not sampled on external memory accesses that use the *Internal* wait state mode. For the first CLKIN cycle of a new external memory access, ACK must be valid by t_{DAAK} or t_{DSAK} or synchronous specification t_{SACKC} for wait state modes *External*, *Either*, or *Both* (*Both*, if the internal wait state is zero). For the second and subsequent cycles of a wait stated external memory access, synchronous specifications t_{SACKC} and t_{HACKC} must be met for wait state modes *External*, *Either*, or *Both* (*Both*, after internal wait states have completed).

[3]See System Hold Time Calculation under Test Conditions for calculation of hold times given capacitive and dc loads.

Synchronous Read/Write—Bus Slave

Use these specifications for ADSP-21065L bus master accesses of a slave's IOP registers or internal memory (in multiprocessor memory space). The bus master must meet these (bus slave) timing requirements.

Parameter		Min	Max	Unit
Timing Requirements:				
t_{SADRI}	Address, $\overline{SW}$ Setup Before CLKIN	24.5 + 25 DT		ns
t_{HADRI}	Address, $\overline{SW}$ Hold Before CLKIN		4.0 + 8 DT	ns
t_{SRWLI}	$\overline{RD}/\overline{WR}$ Low Setup Before CLKIN[1]	21.0 + 21 DT		ns
t_{HRWLI}	$\overline{RD}/\overline{WR}$ Low Hold After CLKIN	–2.50 – 5 DT	7.5 + 7 DT	ns
t_{RWHPI}	$\overline{RD}/\overline{WR}$ Pulse High	2.5		ns
t_{SDATWH}	Data Setup Before $\overline{WR}$ High	4.5		ns
t_{HDATWH}	Data Hold After $\overline{WR}$ High	0.0		ns
Switching Characteristics:				
t_{SDDATO}	Data Delay After CLKIN		31.75 + 21 DT	ns
t_{DATTR}	Data Disable After CLKIN[2]	1.0 – 2 DT	7.0 – 2 DT	ns
t_{DACK}	ACK Delay After CLKIN		29.5 + 20 DT	ns
t_{ACKTR}	ACK Disable After CLKIN[2]	1.0 – 2 DT	6.0 – 2 DT	ns

NOTES

[1]t_{SRWLI} is specified when Multiprocessor Memory Space Wait State (MMSWS bit in WAIT register) is disabled; when MMSWS is enabled, t_{SRWLI} (min) = 17.5 + 18 DT.

[2]See System Hold Time Calculation under Test Conditions for calculation of hold times given capacitive and dc loads.

For two ADSP-21065Ls to communicate synchronously as master and slave, certain master and slave specification combinations must be satisfied. Do not compare specification values directly to calculate master/slave clock skew margins for those specifications listed below. The following table shows the appropriate clock skew margin.

Table IV. Bus Master to Slave Skew Margins

Master Specification	Slave Specification	Skew Margin	
t_{SSDATI}	t_{SDDATO}	t_{CK} = 33.3 ns	+ 2.25 ns
		t_{CK} = 30.0 ns	+ 1.50 ns
t_{SACKC}	t_{DACK}	t_{CK} = 33.3 ns	+ 3.00 ns
		t_{CK} = 30.0 ns	+ 2.25 ns
t_{DADRO}	t_{SADRI}	t_{CK} = 33.3 ns	N/A
		t_{CK} = 30.0 ns	+ 2.75 ns
t_{DRWL} (Max)	t_{SRWLI}	t_{CK} = 33.3 ns	+ 1.50 ns
		t_{CK} = 30.0 ns	+ 1.25 ns
t_{DRDO} (Max)	t_{HRWLI} (Max)	t_{CK} = 33.3 ns	N/A
		t_{CK} = 30.0 ns	3.00 ns
t_{DWRO} (Max)	t_{HRWLI} (Max)	t_{CK} = 33.3 ns	N/A
		t_{CK} = 30.0 ns	3.75 ns

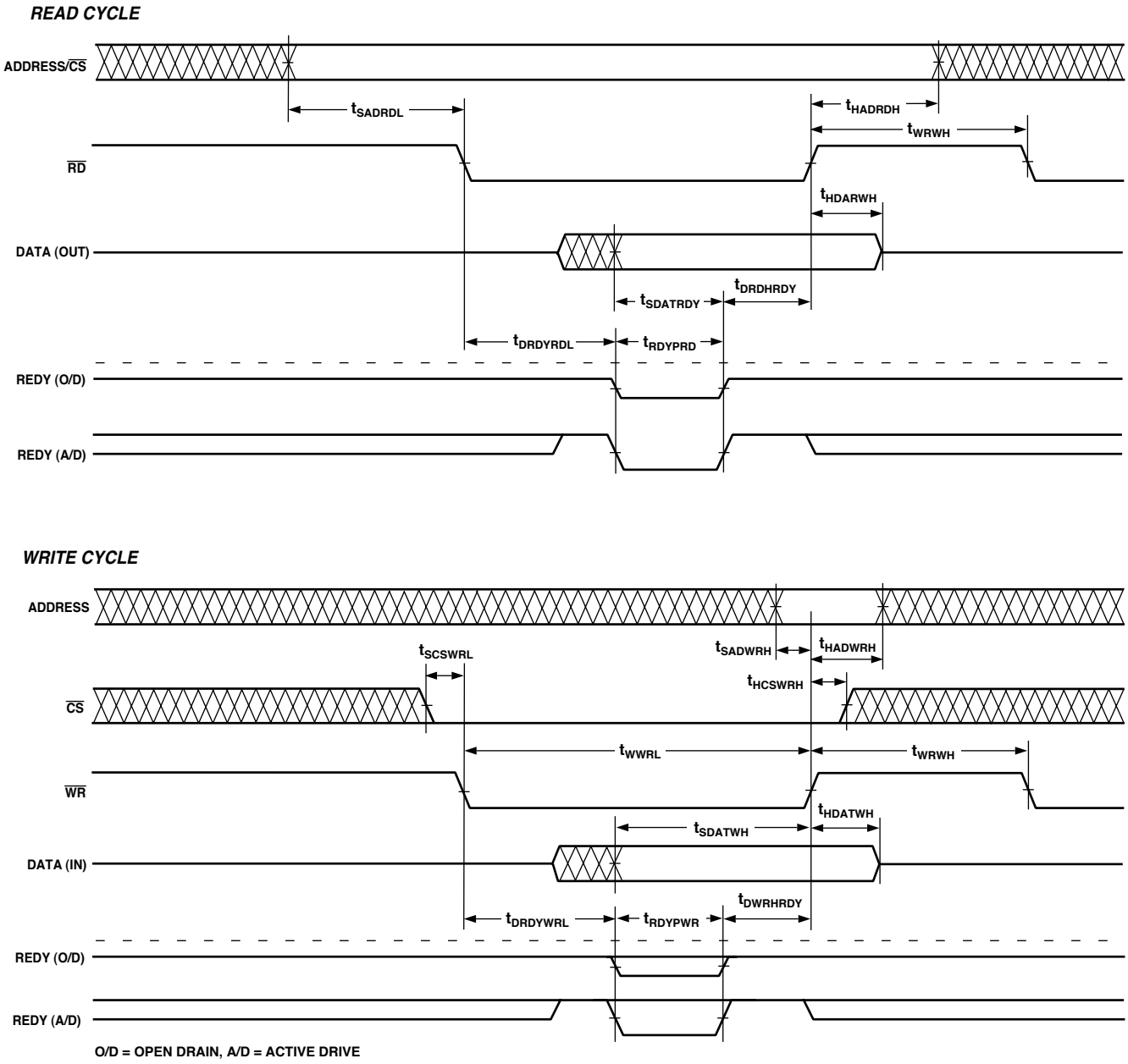
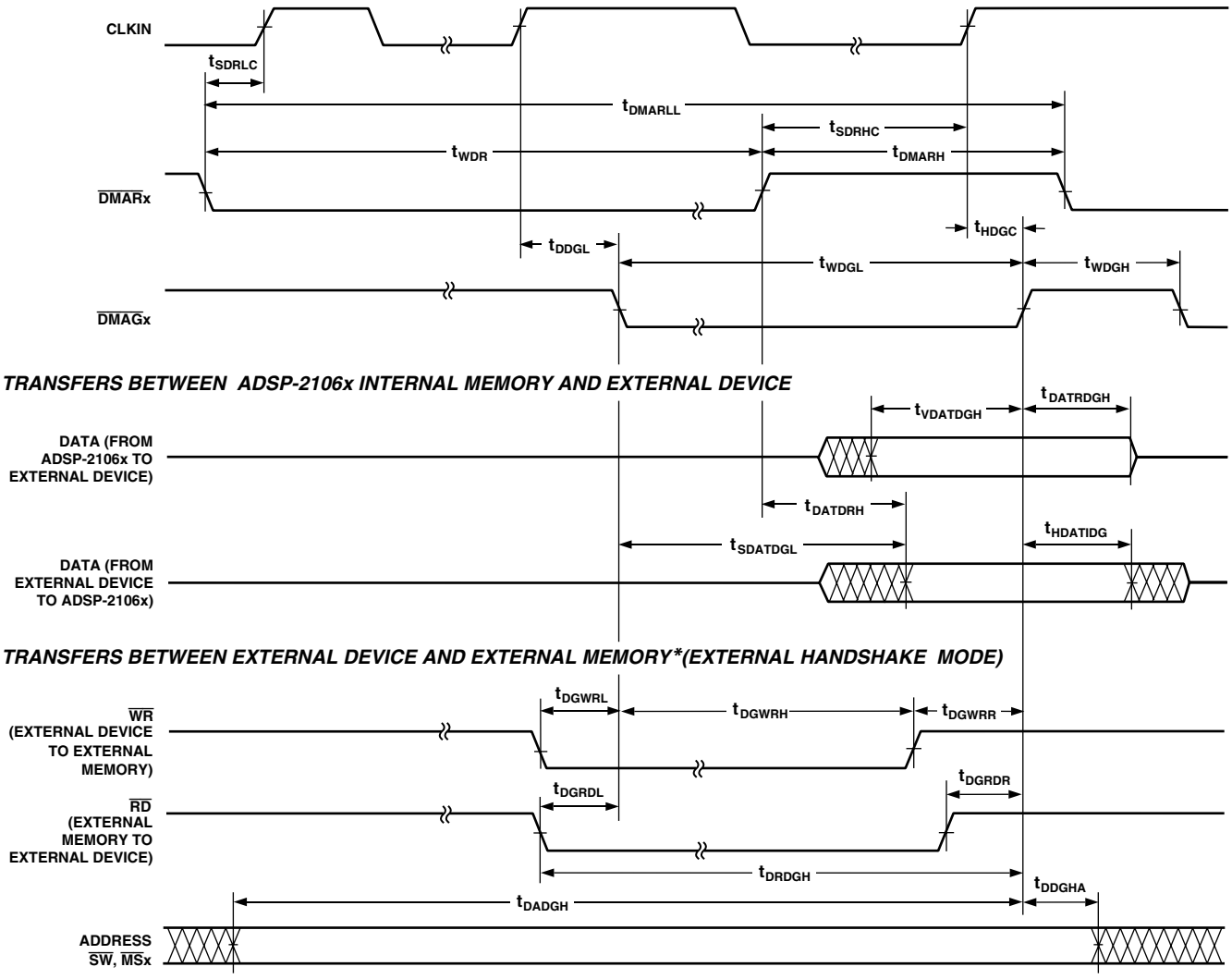


Figure 16. Asynchronous Read/Write—Host to ADSP-21065L



*"MEMORY READ – BUS MASTER," "MEMORY WRITE – BUS MASTER," AND "SYNCHRONOUS READ/WRITE – BUS MASTER" TIMING SPECIFICATIONS FOR $ADDR_{23-0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, $\overline{MS}_{3-0}$, AND ACK ALSO APPLY HERE.

Figure 18. DMA Handshake Timing

Serial Ports

Parameter		Min	Max	Unit
External Clock				
Timing Requirements:				
t_{SFSE}	TFS/RFS Setup Before TCLK/RCLK[1]	4.0		ns
t_{HFSE}	TFS/RFS Hold After TCLK/RCLK[1]	4.0		ns
t_{SDRE}	Receive Data Setup Before RCLK[1]	1.5		ns
t_{HDRE}	Receive Data Hold After RCLK[1]	4.0		ns
t_{SCLKW}	TCLK/RCLK Width	9.0		ns
t_{SCLK}	TCLK/RCLK Period	t_{CK}		ns
Internal Clock				
Timing Requirements:				
t_{SFSI}	TFS Setup Before TCLK[2]; RFS Setup Before RCLK[1]	8.0		ns
t_{HFSI}	TFS/RFS Hold After TCLK/RCLK[1]	1.0		ns
t_{SDRI}	Receive Data Setup Before RCLK[1]	3.0		ns
t_{HDRI}	Receive Data Hold After RCLK[1]	3.0		ns
External or Internal Clock				
Switching Characteristics:				
t_{DFSE}	RFS Delay After RCLK (Internally Generated RFS)[2]		13.0	ns
t_{HOFSE}	RFS Hold After RCLK (Internally Generated RFS)[2]	3.0		ns
External Clock				
Switching Characteristics:				
t_{DFSE}	TFS Delay After TCLK (Internally Generated TFS)[2]		13.0	ns
t_{HOFSE}	TFS Hold After TCLK (Internally Generated TFS)[2]	3.0		ns
t_{DDTE}	Transmit Data Delay After TCLK[2]		12.5	ns
t_{HDTE}	Transmit Data Hold After TCLK[2]	4.0		ns
Internal Clock				
Switching Characteristics:				
t_{DFSI}	TFS Delay After TCLK (Internally Generated TFS)[2]		4.5	ns
t_{HOFSI}	TFS Hold After TCLK (Internally Generated TFS)[2]	–1.5		ns
t_{DDTI}	Transmit Data Delay After TCLK[2]		7.5	ns
t_{HDTI}	Transmit Data Hold After TCLK[2]	0.0		ns
t_{SCLKIW}	TCLK/RCLK Width	$(t_{SCLK}/2) - 2.5$	$(t_{SCLK}/2) + 2.5$	ns
Enable and Three-State				
Switching Characteristics:				
t_{DTENE}	Data Enable from External TCLK[2]	5.0		ns
t_{DDTTE}	Data Disable from External RCLK[2]		10.0	ns
t_{DTENI}	Data Enable from Internal TCLK[2]	0.0		ns
t_{DDTTI}	Data Disable from Internal TCLK[2]		3.0	ns
t_{DCLK}	TCLK/RCLK Delay from CLKIN		18.0 + 6 DT	ns
t_{DPTR}	SPORT Disable After CLKIN		14.0	ns
External Late Frame Sync				
$t_{DDTLFSE}$	Data Delay from Late External TFS or External RFS with MCE = 1, MFD = 0[3, 4]		10.5	ns
$t_{DTENLFSE}$	Data Enable from late FS or MCE = 1, MFD = 0[3, 4]	3.5		ns
$t_{DDTLSCK}$	Data Delay from TCLK/RCLK for Late External TFS or External RFS with MCE = 1, MFD = 0[3, 4]		12.0	ns
$t_{DTENLSCK}$	Data Enable from RCLK/TCLK for Late External FS or MCE = 1, MFD = 0[3, 4]	4.5		ns

NOTES

To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup-and-hold, 2) data delay and data setup-and-hold, and 3) SCLK width.

[1]Referenced to sample edge.

[2]Referenced to drive edge.

[3]MCE = 1, TFS enable and TFS valid follow $t_{DDTENFS}$ and $t_{DDTLFSE}$.

[4]If external RFS/TFS setup to RCLK/TCLK > $t_{SCLK}/2$ then $t_{DDTLSCK}$ and $t_{DTENLSCK}$ apply; otherwise $t_{DDTLFSE}$ and $t_{DTENLFS}$ apply.

*Word selected timing for I^2S mode is the same as TFS/RFS timing (normal framing only).

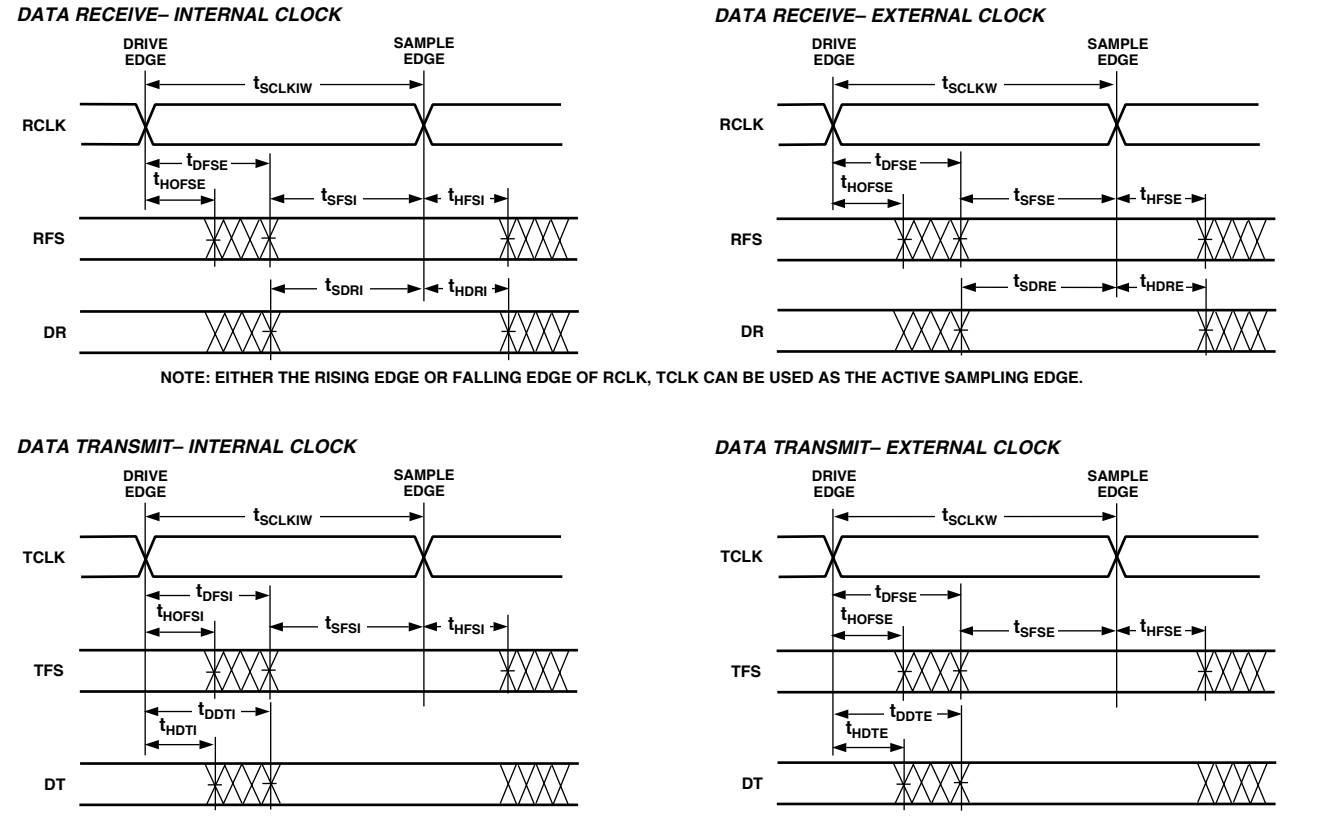


Figure 20. Serial Ports

JTAG Test Access Port and Emulation

Parameter		Min	Max	Unit
Timing Requirements:				
t_{TCK}	TCK Period	t_{CK}		ns
t_{STAP}	TDI, TMS Setup Before TCK High	3.0		ns
t_{HTAP}	TDI, TMS Hold After TCK High	3.0		ns
t_{SSYS}	System Inputs Setup Before TCK Low[1]	7.0		ns
t_{HSYS}	System Inputs Hold After TCK Low[1]	12.0		ns
t_{TRSTW}	$\overline{TRST}$ Pulsewidth	4 t_{CK}		ns
Switching Characteristics:				
t_{DTDO}	TDO Delay from TCK Low		11.0	ns
t_{DSYS}	System Outputs Delay After TCK Low[2]		15.0	ns

NOTES
[1]System Inputs = $DATA_{31-0}$, $ADDR_{23-0}$, $\overline{RD}$, $\overline{WR}$, ACK, $\overline{SBTS}$, $\overline{SW}$, $\overline{HBR}$, $\overline{HBG}$, $\overline{CS}$, $\overline{DMAR_1}$, $\overline{DMAR_2}$, $\overline{BR_{2-1}}$, ID_{1-0}, $\overline{IRQ_{2-0}}$, $FLAG_{11-0}$, DR0x, DR1x, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, BSEL, $\overline{BMS}$, CLKIN, $\overline{RESET}$, $SDCLK_0$, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, SDCKE, PWM_EVENTx.
[2]System Outputs = $DATA_{31-0}$, $ADDR_{23-0}$, MS_{3-0}, $\overline{RD}$, $\overline{WR}$, ACK, $\overline{SW}$, $\overline{HBG}$, REDY, DMAG1, DMAG2, $\overline{BR_{2-1}}$, $\overline{CPA}$, $FLAG_{11-0}$, PWM_EVENTx, DT0x, DT1x, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $\overline{BMS}$, SDCLK0, SDCLK1, DQM, SDA10, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, SDCKE, BM, XTAL.

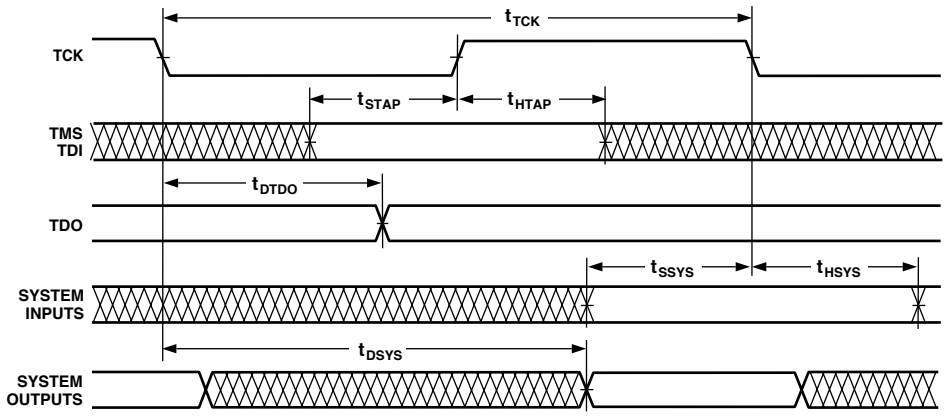


Figure 23. JTAG Test Access Port and Emulation

OUTPUT DRIVE CURRENT

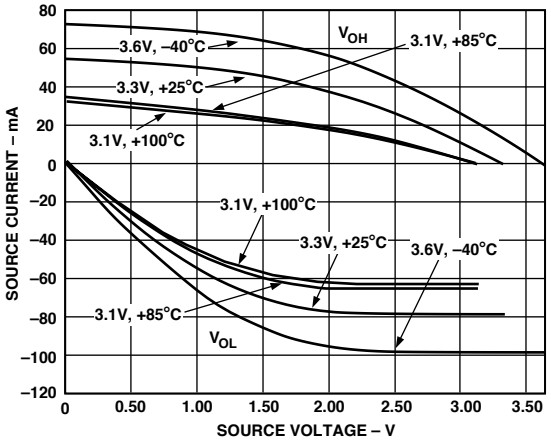


Figure 24. Typical Drive Currents

TEST CONDITIONS

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L and the load current, I_L. This decay time can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times \Delta V}{I_L}$$

The output disable time t_{DIS} is the difference between $t_{MEASURED}$ and t_{DECAY} as shown in Figure 26. The time $t_{MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.5 V.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to when they start driving. The output enable time t_{ENA} is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-21065L's output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (i.e., t_{DATRWH} for the write cycle).

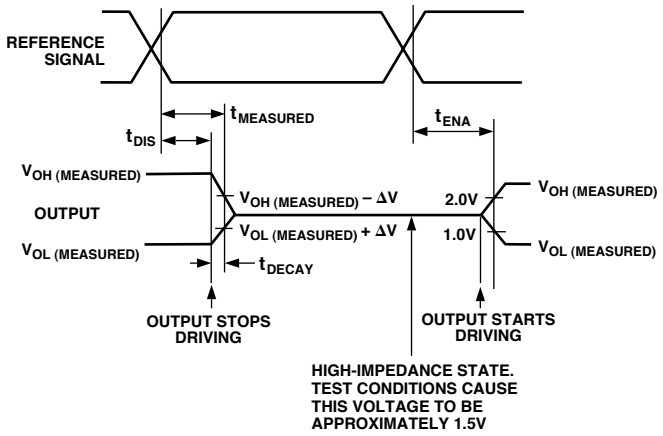


Figure 25. Output Enable

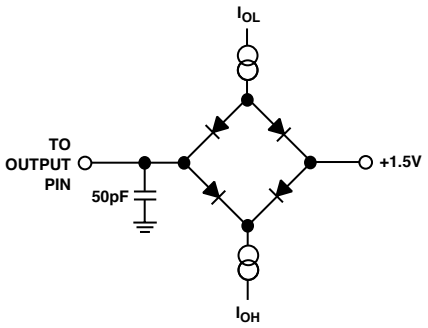


Figure 26. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

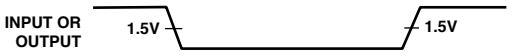


Figure 27. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 50 pF on all pins. The delay and hold specifications given should be derated by a factor of l.8 ns/50 pF for loads other than the nominal value of 50 pF. Figure 28 and Figure 29 show how output rise time varies with capacitance. Figure 30 shows graphically how output delays and hold vary with load capacitance. (Note that this graph or derating does not apply to output disable delays; see the previous section Output Disable time under Test Conditions.) The graphs of Figure 28, Figure 29, and Figure 30 may not be linear outside the ranges shown.

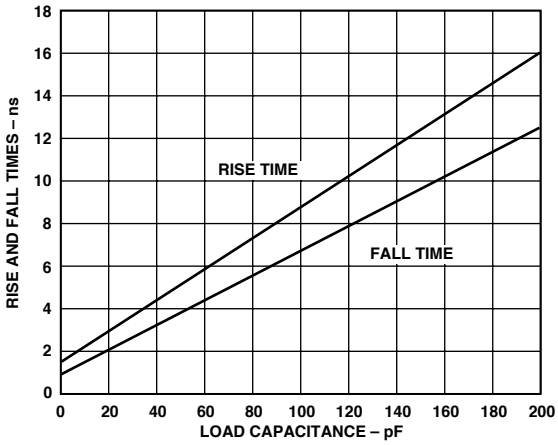


Figure 28. Typical Rise and Fall Time (10%–90% V_{DD})

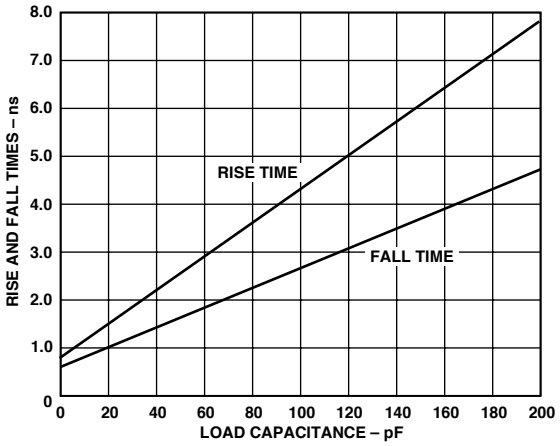


Figure 29. Typical Rise and Fall Time (0.8 V–2.0 V)

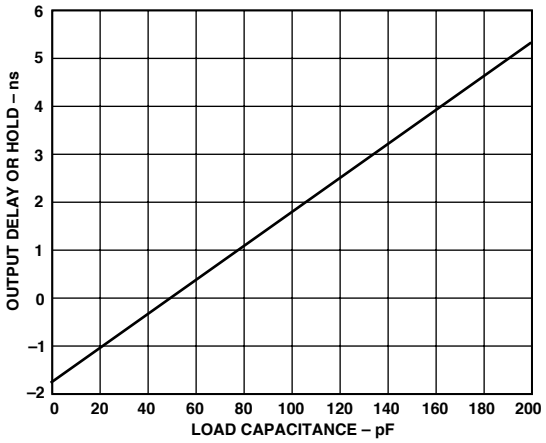


Figure 30. Typical Output Delay or Hold

POWER DISSIPATION

Total power dissipation has two components: one due to internal circuitry and one due to the switching of external output drivers. Internal power dissipation depends on the sequence in which instructions execute and the data operands involved. See I_{DDIN} calculation in Electrical Characteristics section. Internal power dissipation is calculated this way:

$$P_{INT} = I_{DDIN} \times V_{DD}$$

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

– the number of output pins that switch during each cycle (O)
– the maximum frequency at which the pins can switch (f)
– the load capacitance of the pins (C)
– the voltage swing of the pins (V_{DD}).

The external component is calculated using:

$$P_{EXT} = O \times C \times V_{DD}^2 \times f$$

The load capacitance should include the processor's package capacitance (C_{IN}). The frequency f includes driving the load high and then back low. Address and data pins can drive high and low at a maximum rate of $1/t_{CK}$ while in SDRAM burst mode.

Example:

Estimate P_{EXT} with the following assumptions:

– a system with one bank of external memory (32-bit)
– two 1M × 16 SDRAM chips, each with a control signal load of 3 pF and a data signal load of 4 pF
– external data writes occur in burst mode, two every $1/t_{CK}$ cycles, a potential frequency of $1/t_{CK}$ cycles/s. Assume 50% pin switching
– the external SDRAM clock rate is 60 MHz ($2/t_{CK}$).

The P_{EXT} equation is calculated for each class of pins that can drive:

Table V. External Power Calculations

Pin Type	# of Pins	% Switching	× C	× f	× V_{DD}^2	= P_{EXT}
Address	11	50	× 10.7	× 30 MHz	× 10.9 V	= 0.019 W
$\overline{MS_0}$	1	0	× 10.7	—	× 10.9 V	= 0.000 W
$\overline{SDWE}$	1	0	× 10.7	—	× 10.9 V	= 0.000 W
Data	32	50	× 7.7	× 30 MHz	× 10.9 V	= 0.042 W
SDRAM CLK	1	–	× 10.7	× 30 MHz	× 10.9 V	= 0.007 W

P_{EXT} = 0.068 W

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation. (I_{DDIN} see calculation in Electrical Characteristics section):

$$P_{TOTAL} = P_{EXT} + (I_{DDIN} \times V_{DD})$$

Note that the conditions causing a worst-case P_{EXT} differ from those causing a worst-case P_{INT}. Maximum P_{INT} cannot occur while 100% of the output pins are switching from all ones (1s) to all zeros (0s). Note also that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

ENVIRONMENTAL CONDITIONS

Thermal Characteristics

The ADSP-21065L is offered in a 208-lead MQFP and a 196-ball Mini-BGA package.

The ADSP-21065L is specified for a case temperature (T_{CASE}). To ensure that T_{CASE} is not exceeded, an air flow source may be used.

$$T_{CASE} = T_{AMB} + (PD \times \theta_{CA})$$

T_{CASE} = Case temperature (measured on top surface of package)

PD = Power Dissipation in W (this value depends upon the specific application; a method for calculating PD is shown under Power Dissipation)

θ_{JC} = 7.1°C/W for 208-lead MQFP
θ_{JC} = 5.1°C/W for 196-ball Mini-BGA

Airflow

Table VI. Thermal Characteristics (208-Lead MQFP)

(Linear Ft./Min.)	0	100	200	400	600
θ_{CA} (°C/W)	24	20	19	17	13

Table VII. 196-Ball Mini-BGA

(Linear Ft./Min.)	0	200	400
θ_{CA} (°C/W)	38	29	23

208-LEAD MQFP PIN CONFIGURATION

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	VDD	43	$\overline{\text{CAS}}$	85	VDD	127	DATA28	169	ADDR17
2	RFS0	44	$\overline{\text{SDWE}}$	86	DATA3	128	DATA29	170	ADDR16
3	GND	45	VDD	87	DATA4	129	GND	171	ADDR15
4	RCLK0	46	DQM	88	DATA5	130	VDD	172	VDD
5	DR0A	47	SDCKE	89	GND	131	VDD	173	ADDR14
6	DR0B	48	SDA10	90	DATA6	132	DATA30	174	ADDR13
7	TFS0	49	GND	91	DATA7	133	DATA31	175	ADDR12
8	TCLK0	50	$\overline{\text{DMAG}}$1	92	DATA8	134	FLAG7	176	VDD
9	VDD	51	$\overline{\text{DMAG}}$2	93	VDD	135	GND	177	GND
10	GND	52	$\overline{\text{HBG}}$	94	GND	136	FLAG6	178	ADDR11
11	DT0A	53	BMSTR	95	VDD	137	FLAG5	179	ADDR10
12	DT0B	54	VDD	96	DATA9	138	FLAG4	180	ADDR9
13	RFS1	55	$\overline{\text{CS}}$	97	DATA10	139	GND	181	GND
14	GND	56	$\overline{\text{SBTS}}$	98	DATA11	140	VDD	182	VDD
15	RCLK1	57	GND	99	GND	141	VDD	183	ADDR8
16	DR1A	58	$\overline{\text{WR}}$	100	DATA12	142	NC	184	ADDR7
17	DR1B	59	$\overline{\text{RD}}$	101	DATA13	143	ID1	185	ADDR6
18	TFS1	60	GND	102	NC	144	ID0	186	GND
19	TCLK1	61	VDD	103	NC	145	$\overline{\text{EMU}}$	187	GND
20	VDD	62	GND	104	DATA14	146	TDO	188	ADDR5
21	VDD	63	REDY	105	VDD	147	$\overline{\text{TRST}}$	189	ADDR4
22	DT1A	64	$\overline{\text{SW}}$	106	GND	148	TDI	190	ADDR3
23	DT1B	65	$\overline{\text{CPA}}$	107	DATA15	149	TMS	191	VDD
24	PWM_EVENT1	66	VDD	108	DATA16	150	GND	192	VDD
25	GND	67	VDD	109	DATA17	151	TCK	193	ADDR2
26	PWM_EVENT0	68	GND	110	VDD	152	BSEL	194	ADDR1
27	$\overline{\text{BR1}}$	69	ACK	111	DATA18	153	$\overline{\text{BMS}}$	195	ADDR0
28	$\overline{\text{BR2}}$	70	$\overline{\text{MS}}$0	112	DATA19	154	GND	196	GND
29	VDD	71	$\overline{\text{MS}}$1	113	DATA20	155	GND	197	FLAG0
30	CLKIN	72	GND	114	GND	156	VDD	198	FLAG1
31	XTAL	73	GND	115	NC	157	$\overline{\text{RESET}}$	199	FLAG2
32	VDD	74	$\overline{\text{MS}}$2	116	DATA21	158	VDD	200	VDD
33	GND	75	$\overline{\text{MS}}$3	117	DATA22	159	GND	201	FLAG3
34	SDCLK1	76	FLAG11	118	DATA23	160	ADDR23	202	NC
35	GND	77	VDD	119	GND	161	ADDR22	203	NC
36	VDD	78	FLAG10	120	VDD	162	ADDR21	204	GND
37	SDCLK0	79	FLAG9	121	DATA24	163	VDD	205	$\overline{\text{IRQ}}$0
38	$\overline{\text{DMAR}}$1	80	FLAG8	122	DATA25	164	ADDR20	206	$\overline{\text{IRQ}}$1
39	$\overline{\text{DMAR}}$2	81	GND	123	DATA26	165	ADDR19	207	$\overline{\text{IRQ}}$2
40	$\overline{\text{HBR}}$	82	DATA0	124	VDD	166	ADDR18	208	NC
41	GND	83	DATA1	125	GND	167	GND		
42	$\overline{\text{RAS}}$	84	DATA2	126	DATA27	168	GND		

196-BALL MINI-BGA PIN CONFIGURATION

14	13	12	11	10	9	8	7	6	5	4	3	2	1	
NC7	NC8	ADDR18	ADDR17	ADDR14	ADDR11	ADDR8	ADDR7	ADDR6	ADDR3	ADDR0	FLAG2	NC2	NC1	A
TCK	GND	ADDR23	ADDR21	ADDR19	ADDR15	ADDR12	ADDR9	ADDR5	ADDR2	FLAG0	$\overline{\text{IRQ0}}$	RFS0	DR0A	B
TDO	BSEL	$\overline{\text{RESET}}$	ADDR22	ADDR20	ADDR16	ADDR13	ADDR10	ADDR4	ADDR1	FLAG3	$\overline{\text{IRQ2}}$	RCLK0	TCLK0	C
$\overline{\text{EMU}}$	$\overline{\text{TRST}}$	TMS	$\overline{\text{BMS}}$	VDD	VDD	VDD	VDD	VDD	FLAG1	$\overline{\text{IRQ1}}$	DR0B	TFS0	RCLK1	D
FLAG4	ID1	TDI	ID0	VDD	GND	GND	GND	GND	VDD	RFS1	DT0A	DT0B	TFS1	E
FLAG7	FLAG5	FLAG6	VDD	GND	GND	GND	GND	GND	GND	VDD	DR1A	DR1B	TCLK1	F
DATA29	DATA30	DATA31	VDD	GND	GND	GND	GND	GND	GND	VDD	DT1A	DT1B	PWM_ EVENT1	G
DATA26	DATA27	DATA28	VDD	GND	GND	GND	GND	GND	GND	VDD	$\overline{\text{BR2}}$	$\overline{\text{BR1}}$	PWM_ EVENT0	H
DATA23	DATA25	DATA24	VDD	GND	GND	GND	GND	GND	GND	VDD	SDCLK1	XTAL	CLKIN	J
DATA22	DATA20	DATA21	DATA19	VDD	GND	GND	GND	GND	VDD	$\overline{\text{SDWE}}$	$\overline{\text{HBR}}$	SDCLK0	$\overline{\text{DMAR1}}$	K
DATA18	DATA17	DATA16	DATA13	DATA8	VDD	VDD	VDD	VDD	VDD	$\overline{\text{DMAG2}}$	SDA10	$\overline{\text{CAS}}$	$\overline{\text{DMAR2}}$	L
DATA15	DATA14	DATA12	DATA9	DATA5	DATA2	FLAG10	ACK	$\overline{\text{CPA}}$	$\overline{\text{RD}}$	$\overline{\text{CS}}$	$\overline{\text{DMAG1}}$	SDCKE	$\overline{\text{RAS}}$	M
NC6	DATA11	DATA10	DATA7	DATA4	DATA1	FLAG11	$\overline{\text{MS1}}$	GND	REDY	$\overline{\text{SBTS}}$	BMSTR	$\overline{\text{HBG}}$	DQM	N
NC5	DATA6	DATA3	DATA0	FLAG8	FLAG9	$\overline{\text{MS3}}$	$\overline{\text{MS2}}$	$\overline{\text{MS0}}$	$\overline{\text{SW}}$	$\overline{\text{WR}}$	GND	NC4	NC3	P

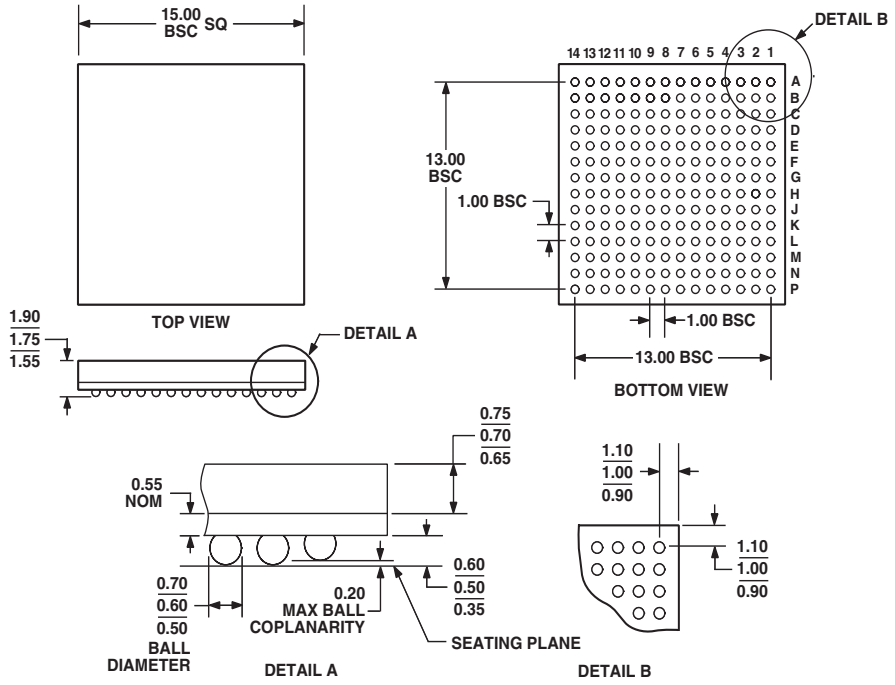
ORDERING GUIDE

Part Number	Case Temperature Range	Instruction Rate	On-Chip SRAM	Operating Voltage	Package Options
ADSP-21065LKS-240	0°C to +85°C	60 MHz	544 Kbit	3.3 V	MQFP
ADSP-21065LCS-240	–40°C to +100°C	60 MHz	544 Kbit	3.3 V	MQFP
ADSP-21065LKCA-240	0°C to +85°C	60 MHz	544 Kbit	3.3 V	Mini-BGA
ADSP-21065LKS-264	0°C to +85°C	66 MHz	544 Kbit	3.3 V	MQFP
ADSP-21065LKCA-264	0°C to +85°C	66 MHz	544 Kbit	3.3 V	Mini-BGA
ADSP-21065LCCA-240	–40°C to +100°C	60 MHz	544 Kbit	3.3 V	Mini-BGA

OUTLINE DIMENSIONS

196-Lead Chip Scale Ball Grid Array [CSPBGA]

Dimensions shown in millimeters



NOTES:
1. THE ACTUAL POSITION OF THE BALL GRID IS WITHIN 0.30 OF ITS IDEAL POSITION RELATIVE TO THE PACKAGE EDGES.
2. THE ACTUAL POSITION OF EACH BALL IS WITHIN 0.10 OF ITS IDEAL POSITION RELATIVE TO THE BALL GRID.
3. DIMENSIONS COMPLY WITH JEDEC STANDARD MS-034AAE-1.
4. CENTER DIMENSIONS ARE NOMINAL.

Revision History

Location	Page
6/03—Data Sheet changed from REV. B to REV. C.	
Edit to GENERAL DESCRIPTION	3
Removal of overbar from DQM	Universal
Edit to POWER DISSIPATION ADSP-21065L (equations above Table III)	13
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