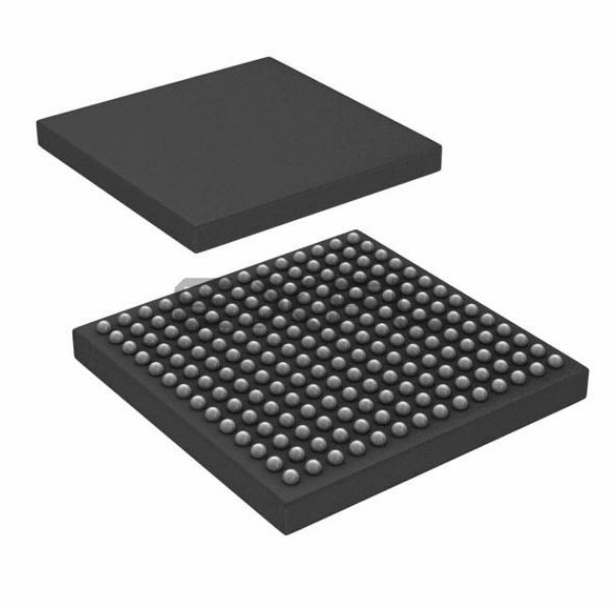

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Floating Point
Interface	Host Interface, Serial Port
Clock Rate	60MHz
Non-Volatile Memory	External
On-Chip RAM	64kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 100°C (TC)
Mounting Type	Surface Mount
Package / Case	196-BGA, CSPBGA
Supplier Device Package	196-CSPBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21065lccaz240

ADSP-21065L* PRODUCT PAGE QUICK LINKS

Last Content Update: 04/08/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- EE-103: Performing Level Conversion Between 5v and 3.3v IC's
- EE-104: Setting Up Streams with the VisualDSP Debugger
- EE-107: ADSP-21065L EPROM Booting
- EE-109: ADSP2106x : Using 2106x SPORT's as Timers
- EE-110: A Quick Primer on ELF and DWARF File Formats
- EE-112: Class Implementation in Analog C++
- EE-116: SHARC Shortword DMA
- EE-127: The ADSP-21065L On-chip SDRAM Controller
- EE-128: DSP in C++: Calling Assembly Class Member Functions From C++
- EE-132: Placing C Code and Data Modules in SHARC memory using VisualDSP++™
- EE-141: Benchmarking C Code on the ADSP-2106x and the ADSP-2116x Family of DSPs
- EE-159: Initializing DSP System & Control Registers From C and C++
- EE-166: ADSP-2106x EPROM Overlay Support with VisualDSP++ 2.0
- EE-175: Emulator and Evaluation Hardware Troubleshooting Guide for VisualDSP++ Users
- EE-191: Implementing a Glueless UART Using The SHARC® DSP SPORTs
- EE-202: Using the Expert Linker for Multiprocessor LDFs
- EE-219: Connecting Character LCD Panels to ADSP-21262 SHARC® DSPs
- EE-244: Interfacing Gated Clocks to ADSP-21065L SHARC® Processors
- EE-247: Interfacing AD7676 ADCs to ADSP-21065L SHARC® Processors
- EE-253: Power Bypass Decoupling of SHARC® Processors
- EE-261: Understanding Jitter Requirements of PLL-Based Processors
- EE-267: Implementing In-Place FFTs on SISD and SIMD SHARC® Processors
- EE-273: Using the VisualDSP++ Command-Line Installer
- EE-280: In-Circuit Flash Programming on ADSP-2106x SHARC® Processors
- EE-285: Migrating from ADSP-21065L to ADSP-21375 SHARC® Processors

- EE-305: Designing and Debugging Systems with SHARC Processors
- EE-323: Implementing Dynamically Loaded Software Modules
- EE-328: Migrating from ADSP-2106x/2116x to ADSP-2126x/2136x/2137x SHARC® Processors
- EE-330: Windows Vista Compatibility in VisualDSP++ 5.0 Development Tools
- EE-332: Cycle Counting and Profiling
- EE-340: Connecting SHARC® and Blackfin® Processors over SPI
- EE-42: C-Programs on the ADSP-2106x
- EE-45: Using the ADSP-2106x/21020 EZ-ICE DBWIN Utility
- EE-46: SHARC Internal Power Measurements
- EE-47: ADSP-2106x Link Ports - Maximum Throughput
- EE-56: Tips and Tricks on SHARC® EPROM and Host Boot Loader
- EE-62: Accessing Short Word Memory In C
- EE-68: Analog Devices JTAG Emulation Technical Reference
- EE-69: Understanding and Using Linker Description Files on SHARC Processors
- EE-70: ADSP-2106x SPORT DTx pins: Is There Potential MCM Data Contention Between Different SHARCs
- EE-74: Analog Devices Serial Port Development and Troubleshooting Guide
- EE-84: External Port DMA Modes of Operation for SHARC Processors
- EE-85: Recommended Handling of Unused SHARC Pins
- EE-86: Interfacing SHARC 2106x DSPs to PLX 9080 PCI Bridge Chips
- EE-98: Using External Bus Arbitration to Group More Than Two ADSP-21065L into a Multiprocessing Cluster
- Interfacing the ADSP21065L SHARC DSP to the AD1819A AC-97 Soundport Codec
- TN: Interfacing I2S Compatible Audio Devices to the ADSP-21065L
- TN: Using the Low Cost, High Performance ADSP21065L DSP for Digital Audio Applications

Data Sheet

- ADSP-21065L: SHARC, 198 MFLOPS, 3.3v Data Sheet

Evaluation Kit Manuals

- ADSP-21061, 21065L and the 21160M EZ-KIT Lite® Installation Procedure

Integrated Circuit Anomalies

- ADSP-21065L Anomaly List for Revision 0.0, 0.1, 0.2, 0.3

Processor Manuals

- ADSP-21065L Technical Reference
- ADSP-21065L User's Manual
- Getting Started with SHARC
- SHARC Processors: Manuals

Product Highlight

- ADSP-21065L SHARC DSP 32-Bit Floating Point Performance Product Highlight
- EZ-KIT Lite for ADSP-21065L SHARC DSP Product Highlight
- SHARC Processor Family

SOFTWARE AND SYSTEMS REQUIREMENTS

- Software and Tools Anomalies Search

TOOLS AND SIMULATIONS

- ADSP-21065L: MBGA Package
- ADSP-21065L: PQFP package
- Designing with BGA
- ADSP-21065L IBIS Datafile (QFP Package)

REFERENCE MATERIALS

Product Selection Guide

- ADI Complementary Parts Guide - Supervisory Devices and DSP Processors

Technical Articles

- An Efficient Asynchronous Sampling-rate Conversion Algorithm for Multi-channel Audio Applications

DESIGN RESOURCES

- ADSP-21065L Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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GENERAL DESCRIPTION

The ADSP-21065L is a powerful member of the SHARC family of 32-bit processors optimized for cost sensitive applications. The SHARC—Super Harvard Architecture—offers the highest levels of performance and memory integration of any 32-bit DSP in the industry—they are also the only DSP in the industry that offer both fixed and floating-point capabilities, without compromising precision or performance.

The ADSP-21065L is fabricated in a high speed, low power CMOS process, 0.35 µm technology. With its on-chip instruction cache, the processor can execute every instruction in a single cycle. Table I lists the performance benchmarks for the ADSP-21065L.

The ADSP-21065L SHARC combines a floating-point DSP core with integrated, on-chip system features, including a 544 Kbit SRAM memory, host processor interface, DMA controller, SDRAM controller, and enhanced serial ports.

Figure 1 shows a block diagram of the ADSP-21065L, illustrating the following architectural features:

- Computation Units (ALU, Multiplier, and Shifter) with a Shared Data Register File
- Data Address Generators (DAG1, DAG2)
- Program Sequencer with Instruction Cache
- Timers with Event Capture Modes
- On-Chip, dual-ported SRAM
- External Port for Interfacing to Off-Chip Memory and Peripherals
- Host Port and SDRAM Interface
- DMA Controller
- Enhanced Serial Ports
- JTAG Test Access Port

Table I. Performance Benchmarks

Benchmark	Timing	Cycles
Cycle Time	15.00 ns	1
1024-Pt. Complex FFT (Radix 4, with Digit Reverse)	0.274 ns	18221
Matrix Multiply (Pipelined)		
$[3 \times 3] \times [3 \times 1]$	135 ns	9
$[4 \times 4] \times [4 \times 1]$	240 ns	16
FIR Filter (per Tap)	15 ns	1
IIR Filter (per Biquad)	60 ns	4
Divide Y/X	90 ns	6
Inverse Square Root ($1/\sqrt{x}$)	135 ns	9
DMA Transfers	264 Mbytes/sec.	

ADSP-21000 FAMILY CORE ARCHITECTURE

The ADSP-21065L is code and function compatible with the ADSP-21060/ADSP-21061/ADSP-21062. The ADSP-21065L includes the following architectural features of the SHARC family core.

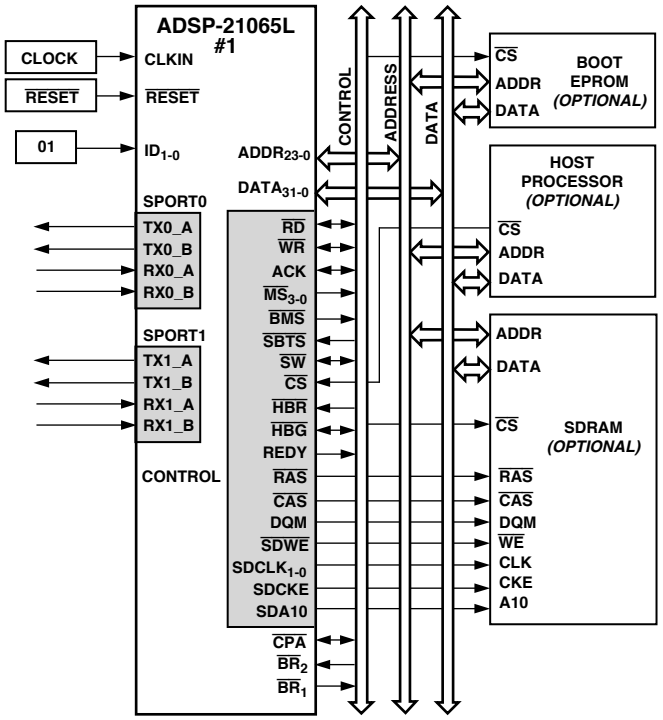

Figure 2. ADSP-21065L Single-Processor System

Independent, Parallel Computation Units
The arithmetic/logic unit (ALU), multiplier, and shifter all perform single-cycle instructions. The three units are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. These computation units support IEEE 32-bit single-precision floating-point, extended precision 40-bit floating-point, and 32-bit fixed-point data formats.

Data Register File
A general-purpose data register file is used for transferring data between the computation units and the data buses, and for storing intermediate results. This 10-port, 32-register (16 primary, 16 secondary) register file, combined with the ADSP-21000 Harvard architecture, allows unconstrained data flow between computation units and internal memory.

Single-Cycle Fetch of Instruction and Two Operands
The ADSP-21065L features an enhanced Super Harvard Architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (see Figure 1). With its separate program and data memory buses, and on-chip instruction cache, the processor can simultaneously fetch two operands and an instruction (from the cache), all in a single cycle.

Instruction Cache
The ADSP-21065L includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and two data values. The cache is selective—only the instructions that fetches conflict with PM bus data accesses are cached. This allows full-speed execution of core, looped operations such as digital filter multiply-accumulates and FFT butterfly processing.

Data Address Generators with Hardware Circular Buffers
The ADSP-21065L's two data address generators (DAGs) implement circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data

structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The ADSP-21065L's two DAGs contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reducing overhead, increasing performance, and simplifying implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set
The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the ADSP-21065L can conditionally execute a multiply, an add, a subtract and a branch, all in a single instruction.

ADSP-21065L FEATURES

The ADSP-21065L is designed to achieve the highest system throughput to enable maximum system performance. It can be clocked by either a crystal or a TTL-compatible clock signal. The ADSP-21065L uses an input clock with a frequency equal to half the instruction rate—a 33 MHz input clock yields a 15 ns processor cycle (which is equivalent to 66 MHz). Interfaces on the ADSP-21065L operate as shown below. Hereafter in this document, 1x = input clock frequency, and 2x = processor's instruction rate.

The following clock operation ratings are based on 1x = 33 MHz (instruction rate/core = 66 MHz):

SDRAM	66 MHz
External SRAM	33 MHz
Serial Ports	33 MHz
Multiprocessing	33 MHz
Host (Asynchronous)	33 MHz

Augmenting the ADSP-21000 family core, the ADSP-21065L adds the following architectural features:

Dual-Ported On-Chip Memory
The ADSP-21065L contains 544 Kbits of on-chip SRAM, organized into two banks: Bank 0 has 288 Kbits, and Bank 1 has 256 Kbits. Bank 0 is configured with 9 columns of 2K × 16 bits, and Bank 1 is configured with 8 columns of 2K × 16 bits. Each memory block is dual-ported for single-cycle, independent accesses by the core processor and I/O processor or DMA controller. The dual-ported memory and separate on-chip buses allow two data transfers from the core and one from I/O, all in a single cycle (see Figure 4 for the ADSP-21065L Memory Map).

On the ADSP-21065L, the memory can be configured as a maximum of 16K words of 32-bit data, 34K words for 16-bit data, 10K words of 48-bit instructions (and 40-bit data) or combinations of different word sizes up to 544 Kbits. All the memory can be accessed as 16-bit, 32-bit or 48-bit.

While each memory block can store combinations of code and data, accesses are most efficient when one block stores data, using the DM bus for transfers, and the other block stores instructions and data, using the PM bus for transfers. Using the DM and PM busses in this way, with one dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache. Single-cycle execution is also maintained when one of the data operands is transferred to or from off-chip, via the ADSP-21065L's external port.

Off-Chip Memory and Peripherals Interface
The ADSP-21065L's external port provides the processor's interface to off-chip memory and peripherals. The 64M words, off-chip address space is included in the ADSP-21065L's unified address space. The separate on-chip buses—for program memory, data memory and I/O—are multiplexed at the external port to create an external system bus with a single 24-bit address bus, four memory selects, and a single 32-bit data bus. The on-chip Super Harvard Architecture provides three bus performance, while the off-chip unified address space gives flexibility to the designer.

SDRAM Interface
The SDRAM interface enables the ADSP-21065L to transfer data to and from synchronous DRAM (SDRAM) at 2x clock frequency. The synchronous approach coupled with 2x clock frequency supports data transfer at a high throughput—up to 220 Mbytes/sec.

The SDRAM interface provides a glueless interface with standard SDRAMs—16 Mb, 64 Mb, and 128 Mb—and includes options to support additional buffers between the ADSP-21065L and SDRAM. The SDRAM interface is extremely flexible and provides capability for connecting SDRAMs to any one of the ADSP-21065L's four external memory banks.

Systems with several SDRAM devices connected in parallel may require buffering to meet overall system timing requirements. The ADSP-21065L supports pipelining of the address and control signals to enable such buffering between itself and multiple SDRAM devices.

Host Processor Interface
The ADSP-21065L's host interface provides easy connection to standard microprocessor buses—8-, 16-, and 32-bit—requiring little additional hardware. Supporting asynchronous transfers at speeds up to 1x clock frequency, the host interface is accessed through the ADSP-21065L's external port. Two channels of DMA are available for the host interface; code and data transfers are accomplished with low software overhead.

The host processor requests the ADSP-21065L's external bus with the host bus request ($\overline{\text{HBR}}$), host bus grant ($\overline{\text{HBG}}$), and ready (REDY) signals. The host can directly read and write the IOP registers of the ADSP-21065L and can access the DMA channel setup and mailbox registers. Vector interrupt support enables efficient execution of host commands.

DMA Controller
The ADSP-21065L's on-chip DMA controller allows zero-overhead, nonintrusive data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions.

DMA transfers can occur between the ADSP-21065L's internal memory and either external memory, external peripherals, or a host processor. DMA transfers can also occur between the ADSP-21065L's internal memory and its serial ports. DMA transfers between external memory and external peripheral devices are another option. External bus packing to 16-, 32-, or 48-bit internal words is performed during DMA transfers.

Ten channels of DMA are available on the ADSP-21065L—eight via the serial ports, and two via the processor's external port (for either host processor, other ADSP-21065L, memory or

I/O transfers). Programs can be downloaded to the ADSP-21065L using DMA transfers. Asynchronous off-chip peripherals can control two DMA channels using DMA Request/Grant lines ($\overline{DMAR}_{1-2}$, $\overline{DMAG}_{1-2}$). Other DMA features include interrupt generation on completion of DMA transfers and DMA chaining for automatically linked DMA transfers.

Serial Ports
The ADSP-21065L features two synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices. The serial ports can operate at 1x clock frequency, providing each with a maximum data rate of 33 Mbit/s. Each serial port has a primary and a secondary set of transmit and receive channels. Independent transmit and receive functions provide greater flexibility for serial communications. Serial port data can be automatically transferred to and from on-chip memory via DMA. Each of the serial ports supports three operation modes: DSP serial port mode, I^2S mode (an interface commonly used by audio codecs), and TDM (Time Division Multiplex) multichannel mode.

The serial ports can operate with little-endian or big-endian transmission formats, with selectable word lengths of 3 bits to 32 bits. They offer selectable synchronization and transmit modes and optional μ-law or A-law companding. Serial port clocks and frame syncs can be internally or externally generated. The serial ports also include keyword and keymask features to enhance interprocessor communication.

Programmable Timers and General-Purpose I/O Ports
The ADSP-21065L has two independent timer blocks, each of which performs two functions—Pulsewidth Generation and Pulse Count and Capture.

In Pulsewidth Generation mode, the ADSP-21065L can generate a modulated waveform with an arbitrary pulsewidth within a maximum period of 71.5 secs.

In Pulse Counter mode, the ADSP-21065L can measure either the high or low pulsewidth and the period of an input waveform.

The ADSP-21065L also contains twelve programmable, general purpose I/O pins that can function as either input or output. As output, these pins can signal peripheral devices; as input, these pins can provide the test for conditional branching.

Program Booting
The internal memory of the ADSP-21065L can be booted at system power-up from an 8-bit EPROM, a host processor, or external memory. Selection of the boot source is controlled by the $\overline{BMS}$ (Boot Memory Select) and BSEL (EPROM Boot) pins. Either 8-, 16-, or 32-bit host processors can be used for booting. For details, see the descriptions of the $\overline{BMS}$ and BSEL pins in the Pin Descriptions section of this data sheet.

Multiprocessing
The ADSP-21065L offers powerful features tailored to multiprocessing DSP systems. The unified address space allows direct interprocessor accesses of both ADSP-21065L's IOP registers. Distributed bus arbitration logic is included on-chip for simple, glueless connection of systems containing a maximum of two ADSP-21065Ls and a host processor. Master processor changeover incurs only one cycle of overhead. Bus lock allows indivisible read-modify-write sequences for semaphores. A vector interrupt is provided for interprocessor commands. Maximum throughput for interprocessor data transfer is 132 Mbytes/sec over the external port.

DEVELOPMENT TOOLS
The ADSP-21065L is supported with a complete set of software and hardware development tools, including the EZ-ICE® In-Circuit Emulator and development software.

The same EZ-ICE hardware that you use for the ADSP-21060/ ADSP-21062 also fully emulates the ADSP-21065L.

Both the SHARC Development Tools family and the VisualDSP® integrated project management and debugging environment support the ADSP-21065L. The VisualDSP project management environment enables you to develop and debug an application from within a single integrated program.

The SHARC Development Tools include an easy to use Assembler that is based on an algebraic syntax; an Assembly library/ librarian; a linker; a loader; a cycle-accurate, instruction-level simulator; a C compiler; and a C run-time library that includes DSP and mathematical functions.

Debugging both C and Assembly programs with the Visual DSP debugger, you can:

- View Mixed C and Assembly Code
- Insert Break Points
- Set Watch Points
- Trace Bus Activity
- Profile Program Execution
- Fill and Dump Memory
- Create Custom Debugger Windows

The Visual IDE enables you to define and manage multiuser projects. Its dialog boxes and property pages enable you to configure and manage all of the SHARC Development Tools. This capability enables you to:

- Control how the development tools process inputs and generate outputs.
- Maintain a one-to-one correspondence with the tool's command line switches.

The EZ-ICE Emulator uses the IEEE 1149.1 JTAG test access port of the ADSP-21065L processor to monitor and control the target board processor during emulation. The EZ-ICE provides full-speed emulation, allowing inspection and modification of memory, registers, and processor stacks. Nonintrusive in-circuit emulation is assured by the use of the processor's JTAG interface—the emulator does not affect target system loading or timing.

In addition to the software and hardware development tools available from Analog Devices, third parties provide a wide range of tools supporting the SHARC processor family. Hardware tools include SHARC PC plug-in cards multiprocessor SHARC VME boards, and daughter and modules with multiple SHARCs and additional memory. These modules are based on the SHARCPAC™ module specification. Third Party software tools include an Ada compiler, DSP libraries, operating systems, and block diagram design tools.

Additional Information
For detailed information on the ADSP-21065L instruction set and architecture, see the *ADSP-21065L SHARC User's Manual*, Third Edition, and the *ADSP-21065L SHARC Technical Reference.*

The BTMS, BTCK, $\overline{\text{BTRST}}$ and BTDI signals are provided so that the test access port can also be used for board-level testing. When the connector is not being used for emulation, place jumpers between the Bxxx pins and the xxx pins. If you are not going to use the test access port for board testing, tie $\overline{\text{BTRST}}$ to GND and tie or pull-up BTCK to V_{DD}. The $\overline{\text{TRST}}$ pin must be asserted after power-up (through $\overline{\text{BTRST}}$ on the connector) or held low for proper operation of the ADSP-2106x. None of the Bxxx pins (Pins 5, 7, 9, 11) are connected on the EZ-ICE probe.

The JTAG signals are terminated on the EZ-ICE probe as follows:

Signal	Termination
TMS	Driven through 22 Ω resistor (16 mA driver)
TCK	Driven at 10 MHz through 22 Ω resistor (16 mA driver)
$\overline{\text{TRST}}$*	Driven through 22 Ω resistor (16 mA driver) (pulled up by on-chip 20 kΩ resistor)
TDI	Driven by 22 Ω resistor (16 mA driver)
TDO	One TTL load, Split Termination (160/220)
CLKIN	One TTL load, Split Termination (160/220). (Caution: Do not connect to CLKIN if internal XTAL oscillator is used.)
EMU	Active Low 4.7 kΩ pull-up resistor, one TTL load (open-drain output from ADSP-2106xs)

*$\overline{\text{TRST}}$ is driven low until the EZ-ICE probe is turned on by the emulator at software start-up. After software start-up, $\overline{\text{TRST}}$ is driven high.

Connecting CLKIN to Pin 4 of the EZ-ICE header is optional. The emulator only uses CLKIN when directed to perform operations such as starting, stopping, and single-stepping two ADSP-21065Ls in a synchronous manner. If you do not need these operations to occur synchronously on the two processors, simply tie Pin 4 of the EZ-ICE header to ground.

For systems which use the internal clock generator and an external discrete crystal, do not directly connect the CLKIN pin to the JTAG probe. This will load the oscillator circuit and possibly cause it to fail to oscillate. Instead the JTAG probe's CLKIN can be driven by the XTAL pin through a high impedance buffer.

If synchronous multiprocessor operations are needed and CLKIN is connected, clock skew between multiple ADSP-2106x processors and the CLKIN pin on the EZ-ICE header must be minimal. If the skew is too large, synchronous operations may be off by one cycle between processors. For synchronous multiprocessor operation TCK, TMS, CLKIN and $\overline{\text{EMU}}$ should be treated as critical signals in terms of skew, and should be laid out as short as possible on your board.

If synchronous multiprocessor operations are not needed (i.e., CLKIN is not connected), just use appropriate parallel termination on TCK and TMS. TDI, TDO, $\overline{\text{EMU}}$ and $\overline{\text{TRST}}$ are not critical signals in terms of skew.

For complete information on the SHARC EZ-ICE, see the *ADSP-21000 Family JTAG EZ-ICE User's Guide and Reference.*

ADSP-21065L–SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter		Test Conditions	C Grade Min	C Grade Max	K Grade Min	K Grade Max	Unit
V_{DD}	Supply Voltage		3.13	3.60	3.13	3.60	V
T_{CASE}	Case Operating Temperature		–40	+100	0	+85	°C
V_{IH}	High Level Input Voltage	@ V_{DD} = max	2.0	V_{DD} + 0.5	2.0	V_{DD} + 0.5	V
V_{IL1}	Low Level Input Voltage[1]	@ V_{DD} = min	–0.5	0.8	–0.5	0.8	V
V_{IL2}	Low Level Input Voltage[2]	@ V_{DD} = min	–0.5	0.7	–0.5	0.7	V

NOTE
See Environmental Conditions for information on thermal specifications.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	C and K Grades Min	C and K Grades Max	Unit
V_{OH}	High Level Output Voltage[3]	@ V_{DD} = min, I_{OH} = –2.0 mA[4]	2.4		V
V_{OL}	Low Level Output Voltage[3]	@ V_{DD} = min, I_{OL} = 4.0 mA[4]		0.4	V
I_{IH}	High Level Input Current[5]	@ V_{DD} = max, V_{IN} = V_{DD} max		10	µA
I_{IL}	Low Level Input Current[5]	@ V_{DD} = max, V_{IN} = 0 V		10	µA
I_{ILP}	Low Level Input Current[6]	@ V_{DD} = max, V_{IN} = 0 V		150	µA
I_{OZH}	Three-State Leakage Current[7, 8, 9, 10]	@ V_{DD} = max, V_{IN} = V_{DD} max		10	µA
I_{OZL}	Three-State Leakage Current[7]	@ V_{DD} = max, V_{IN} = 0 V		8	µA
I_{OZLS}	Three-State Leakage Current[8]	@ V_{DD} = max, V_{IN} = 0 V		150	µA
I_{OZLA}	Three-State Leakage Current[11]	@ V_{DD} = max, V_{IN} = 1.5 V		350	µA
I_{OZLAR}	Three-State Leakage Current[10]	@ V_{DD} = max, V_{IN} = 0 V		4	mA
I_{OZLC}	Three-State Leakage Current[9]	@ V_{DD} = max, V_{IN} = 0 V		1.5	mA
C_{IN}	Input Capacitance[12, 13]	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		8	pF

NOTES
[1] Applies to input and bidirectional pins: $DATA_{31-0}$, $ADDR_{23-0}$, BSEL, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $\overline{SBTS}$, $\overline{IRQ}_{2-0}$, $FLAG_{11-0}$, $\overline{HBG}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR}_{2-1}$, $\overline{ID}_{2-0}$, RPBA, $\overline{CPA}$, TFS0, TFS1, RFS0, RFS1, $\overline{BMS}$, TMS, TDI, TCK, $\overline{HBR}$, DR0A, DR1A, DR0B, DR1B, TCLK0, TCLK1, RCLK0, RCLK1, $\overline{RESET}$, $\overline{TRST}$, PWM_EVENT0, PWM_EVENT1, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, $\overline{SDCKE}$.
[2] Applies to input pin CLKIN.
[3] Applies to output and bidirectional pins: $DATA_{31-0}$, $ADDR_{23-0}$, MS_{3-0}, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $FLAG_{11-0}$, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR}_{2-1}$, $\overline{CPA}$, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, DT0A, DT1A, DT0B, DT1B, XTAL, $\overline{BMS}$, TDO, $\overline{EMU}$, BMSTR, PWM_EVENT0, PWM_EVENT1, $\overline{RAS}$, $\overline{CAS}$, DQM, $\overline{SDWE}$, SDCLK0, SDCLK1, $\overline{SDCKE}$, SDA10.
[4] See Output Drive Currents for typical drive current capabilities.
[5] Applies to input pins: ACK, $\overline{SBTS}$, $\overline{IRQ}_{2-0}$, $\overline{HBR}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, ID_{1-0}, BSEL, CLKIN, $\overline{RESET}$, TCK (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID_{1-0} = 01 and another ADSP-21065L is not requesting bus mastership.)
[6] Applies to input pins with internal pull-ups: DR0A, DR1A, DR0B, DR1B, $\overline{TRST}$, TMS, TDI.
[7] Applies to three-statable pins: $DATA_{31-0}$, $ADDR_{23-0}$, $\overline{MS}_{3-0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $FLAG_{11-0}$, REDY, $\overline{HBG}$, $\overline{DMAG}_1$, $\overline{DMAG}_2$, $\overline{BMS}$, TDO, $\overline{RAS}$, $\overline{CAS}$, DQM, $\overline{SDWE}$, SDCLK0, SDCLK1, $\overline{SDCKE}$, SDA10, and $\overline{EMU}$ (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID_{1-0} = 01 and another ADSP-21065L is not requesting bus mastership).
[8] Applies to three-statable pins with internal pull-ups: DT0A, DT1A, DT0B, DT1B, TCLK0, TCLK1, RCLK0, RCLK1.
[9] Applies to $\overline{CPA}$ pin.
[10] Applies to ACK pin when pulled up.
[11] Applies to ACK pin when keeper latch enabled.
[12] Guaranteed but not tested.
[13] Applies to all signal pins.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . –0.3 V to +4.6 V
Input Voltage . . . . . –0.5 V to V_{DD} + 0.5 V
Output Voltage Swing . . . . . –0.5 V to V_{DD} + 0.5 V
Load Capacitance . . . . . 200 pF
Junction Temperature Under Bias . . . . . 130°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (5 seconds) . . . . . 280°C

*Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADSP-21065L features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

POWER DISSIPATION ADSP-21065L

These specifications apply to the internal power portion of V_{DD} only. See the Power Dissipation section of this data sheet for calculation of external supply current and total supply current. For a complete discussion of the code used to measure power dissipation, see the technical note SHARC Power Dissipation Measurements.

Specifications are based on the following operating scenarios:

Table II. Internal Current Measurements

Operation	Peak Activity ($I_{DDINPEAK}$)	High Activity ($I_{DDINHIGH}$)	Low Activity ($I_{DDINLOW}$)
Instruction Type	Multifunction	Multifunction	Single Function
Instruction Fetch	Cache	Internal Memory	Internal Memory
Core Memory Access	2 per Cycle (DM and PM)	1 per Cycle (DM)	None
Internal Memory DMA	1 per Cycle	1 per 2 Cycles	1 per 2 Cycles

To estimate power consumption for a specific application, use the following equation where % is the amount of time your program spends in that state:

$\%PEAK \times I_{DDINPEAK} + \%HIGH \times I_{DDINHIGH} + \%LOW \times I_{DDINLOW} + \%IDLE \times I_{DDIDLE} = POWER\ CONSUMPTION$
(See note 4 below Table III.)

OR $\%PEAK \times I_{DDINPEAK} + \%HIGH \times I_{DDINHIGH} + \%LOW \times I_{DDINLOW} + \%IDLE16 \times I_{DDIDLE16} = POWER\ CONSUMPTION$
(See note 5 below Table III.)

Table III. Internal Current Measurement Scenarios

Parameter		Test Conditions	Max	Unit
$I_{DDINPEAK}$	Supply Current (Internal)[1]	t_{CK} = 33 ns, V_{DD} = max	470	mA
		t_{CK} = 30 ns, V_{DD} = max	510	mA
$I_{DDINHIGH}$	Supply Current (Internal)[2]	t_{CK} = 33 ns, V_{DD} = max	275	mA
		t_{CK} = 30 ns, V_{DD} = max	300	mA
$I_{DDINLOW}$	Supply Current (Internal)[3]	t_{CK} = 33 ns, V_{DD} = max	240	mA
		t_{CK} = 30 ns, V_{DD} = max	260	mA
I_{DDIDLE}	Supply Current (IDLE)[4]	t_{CK} = 33 ns, V_{DD} = max	150	mA
		t_{CK} = 30 ns, V_{DD} = max	155	mA
$I_{DDIDLE16}$	Supply Current (IDLE16)[5]	V_{DD} = max	50	mA

NOTES
[1]The test program used to measure $I_{DDINPEAK}$ represents worst-case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified.
[2]$I_{DDINHIGH}$ is a composite average based on a range of high activity code.
[3]$I_{DDINLOW}$ is a composite average based on a range of low activity code.
[4]IDLE denotes ADSP-21065L state during execution of IDLE instruction.
[5]IDLE16 denotes ADSP-21065L state during execution of IDLE16 instruction.

TIMING SPECIFICATIONS

General Notes

Two speed grades of the ADSP-21065L are offered, 60 MHz and 66 MHz instruction rates. The specifications shown are based on a CLKIN frequency of 30 MHz (t_{CK} = 33.3 ns). The DT derating allows specifications at other CLKIN frequencies (within the min–max range of the t_{CK} specification; see Clock Input below). DT is the difference between the actual CLKIN period and a CLKIN period of 33.3 ns:

$$DT = (t_{CK} - 33.3)/32$$

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add parameters to derive longer times.

See Figure 27 in Equivalent Device Loading for AC Measurements (Includes All Fixtures) for voltage reference levels.

Synchronous Read/Write—Bus Master

Use these specifications for interfacing to external memory systems that require CLKIN-relative timing or for accessing a slave ADSP-21065L (in multiprocessor memory space). These synchronous switching characteristics are also valid during asynchronous memory reads and writes (see Memory Read—Bus Master and Memory Write—Bus Master).

When accessing a slave ADSP-21065L, these switching characteristics must meet the slave's timing requirements for synchronous read/writes (see Synchronous Read/Write—Bus Slave). The slave ADSP-21065L must also meet these (bus master) timing requirements for data and acknowledge setup and hold times.

Parameter		Min	Max	Unit
Timing Requirements:				
t_{SSDATI}	Data Setup Before CLKIN	0.25 + 2 DT		ns
t_{HSDATI}	Data Hold After CLKIN	4.0 – 2 DT		ns
t_{DAAK}	ACK Delay After Address, $\overline{MS}$x, $\overline{SW}$, $\overline{BMS}$[1, 2]		24.0 + 30 DT + W	ns
t_{SACKC}	ACK Setup Before CLKIN[1]	2.75 + 4 DT		ns
t_{HACK}	ACK Hold After CLKIN	2.0 – 4 DT		ns
Switching Characteristics:				
t_{DADRO}	Address, $\overline{MS}$x, $\overline{BMS}$, $\overline{SW}$ Delay After CLKIN[1]		7.0 – 2 DT	ns
t_{HADRO}	Address, $\overline{MS}$x, $\overline{BMS}$, $\overline{SW}$ Hold After CLKIN	0.5 – 2 DT		ns
t_{DRDO}	$\overline{RD}$ High Delay After CLKIN	0.5 – 2 DT	6.0 – 2 DT	ns
t_{DWRO}	$\overline{WR}$ High Delay After CLKIN	0.0 – 3 DT	6.0 – 3 DT	ns
t_{DRWL}	$\overline{RD}$/$\overline{WR}$ Low Delay After CLKIN	7.5 + 4 DT	11.75 + 4 DT	ns
t_{DDATO}	Data Delay After CLKIN		22.0 + 10 DT	ns
t_{DATTR}	Data Disable After CLKIN[3]	1.0 – 2 DT	7.0 – 2 DT	ns
t_{DBM}	BMSTR Delay After CLKIN		3.0	ns
t_{HBM}	BMSTR Hold After CLKIN	–4.0		ns

W = (number of wait states specified in WAIT register) × t_{CK}.

NOTES

[1]Data Hold: User must meet t_{HDA} or t_{HDRH} or synchronous specification t_{HDATI}. See system hold time calculation under test conditions for the calculation of hold times given capacitive and dc loads.

[2]ACK is not sampled on external memory accesses that use the *Internal* wait state mode. For the first CLKIN cycle of a new external memory access, ACK must be valid by t_{DAAK} or t_{DSAK} or synchronous specification t_{SACKC} for wait state modes *External*, *Either*, or *Both* (*Both*, if the internal wait state is zero). For the second and subsequent cycles of a wait stated external memory access, synchronous specifications t_{SACKC} and t_{HACKC} must be met for wait state modes *External*, *Either*, or *Both* (*Both*, after internal wait states have completed).

[3]See System Hold Time Calculation under Test Conditions for calculation of hold times given capacitive and dc loads.

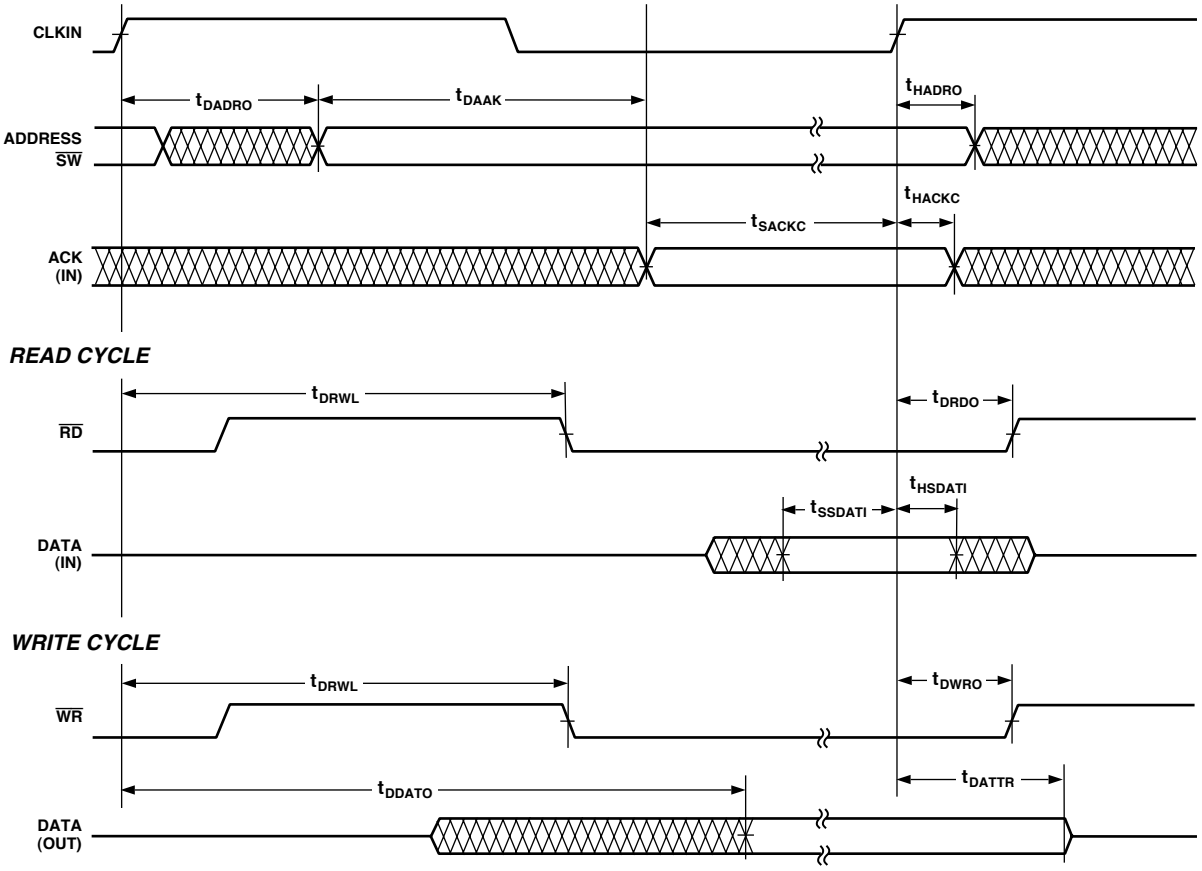

Figure 13. Synchronous Read/Write—Bus Master

Synchronous Read/Write—Bus Slave

Use these specifications for ADSP-21065L bus master accesses of a slave's IOP registers or internal memory (in multiprocessor memory space). The bus master must meet these (bus slave) timing requirements.

Parameter		Min	Max	Unit
Timing Requirements:				
t_{SADRI}	Address, $\overline{SW}$ Setup Before CLKIN	24.5 + 25 DT		ns
t_{HADRI}	Address, $\overline{SW}$ Hold Before CLKIN		4.0 + 8 DT	ns
t_{SRWLI}	$\overline{RD}/\overline{WR}$ Low Setup Before CLKIN[1]	21.0 + 21 DT		ns
t_{HRWLI}	$\overline{RD}/\overline{WR}$ Low Hold After CLKIN	–2.50 – 5 DT	7.5 + 7 DT	ns
t_{RWHPI}	$\overline{RD}/\overline{WR}$ Pulse High	2.5		ns
t_{SDATWH}	Data Setup Before $\overline{WR}$ High	4.5		ns
t_{HDATWH}	Data Hold After $\overline{WR}$ High	0.0		ns
Switching Characteristics:				
t_{SDDATO}	Data Delay After CLKIN		31.75 + 21 DT	ns
t_{DATTR}	Data Disable After CLKIN[2]	1.0 – 2 DT	7.0 – 2 DT	ns
t_{DACK}	ACK Delay After CLKIN		29.5 + 20 DT	ns
t_{ACKTR}	ACK Disable After CLKIN[2]	1.0 – 2 DT	6.0 – 2 DT	ns

NOTES

[1]t_{SRWLI} is specified when Multiprocessor Memory Space Wait State (MMSWS bit in WAIT register) is disabled; when MMSWS is enabled, t_{SRWLI} (min) = 17.5 + 18 DT.

[2]See System Hold Time Calculation under Test Conditions for calculation of hold times given capacitive and dc loads.

For two ADSP-21065Ls to communicate synchronously as master and slave, certain master and slave specification combinations must be satisfied. Do not compare specification values directly to calculate master/slave clock skew margins for those specifications listed below. The following table shows the appropriate clock skew margin.

Table IV. Bus Master to Slave Skew Margins

Master Specification	Slave Specification	Skew Margin	
t_{SSDATI}	t_{SDDATO}	t_{CK} = 33.3 ns	+ 2.25 ns
		t_{CK} = 30.0 ns	+ 1.50 ns
t_{SACKC}	t_{DACK}	t_{CK} = 33.3 ns	+ 3.00 ns
		t_{CK} = 30.0 ns	+ 2.25 ns
t_{DADRO}	t_{SADRI}	t_{CK} = 33.3 ns	N/A
		t_{CK} = 30.0 ns	+ 2.75 ns
t_{DRWL} (Max)	t_{SRWLI}	t_{CK} = 33.3 ns	+ 1.50 ns
		t_{CK} = 30.0 ns	+ 1.25 ns
t_{DRDO} (Max)	t_{HRWLI} (Max)	t_{CK} = 33.3 ns	N/A
		t_{CK} = 30.0 ns	3.00 ns
t_{DWRO} (Max)	t_{HRWLI} (Max)	t_{CK} = 33.3 ns	N/A
		t_{CK} = 30.0 ns	3.75 ns

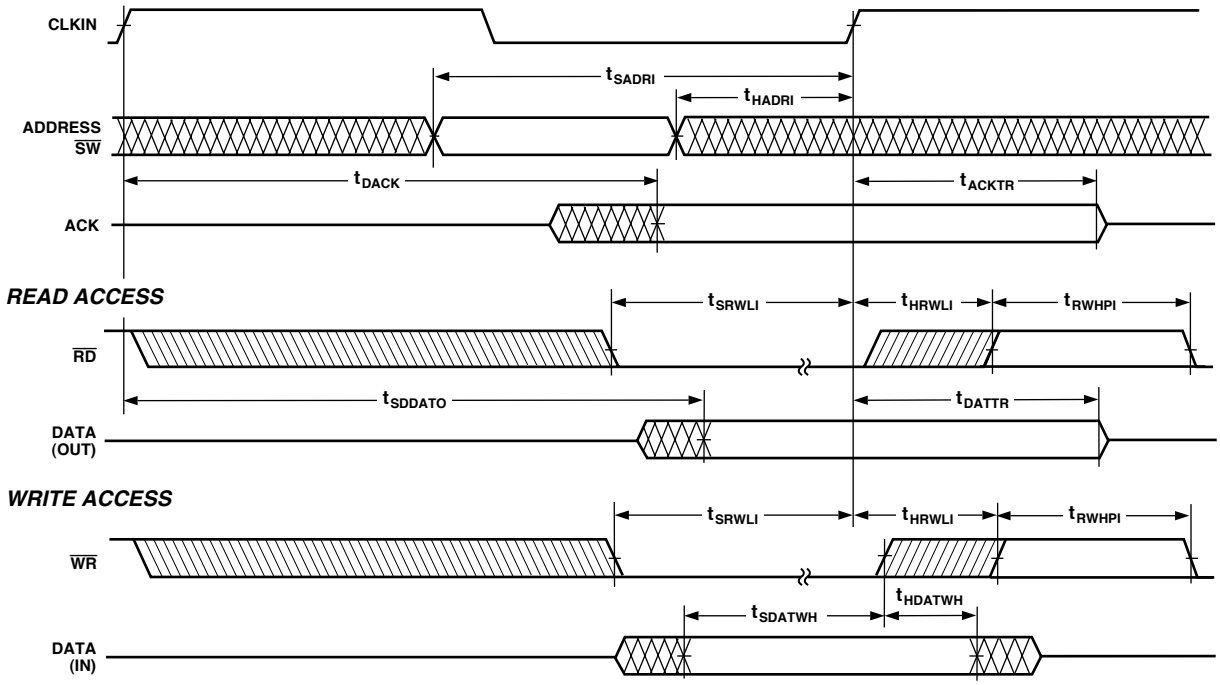

Figure 14. Synchronous Read/Write—Bus Slave

Serial Ports

Parameter		Min	Max	Unit
External Clock				
Timing Requirements:				
t_{SFSE}	TFS/RFS Setup Before TCLK/RCLK[1]	4.0		ns
t_{HFSE}	TFS/RFS Hold After TCLK/RCLK[1]	4.0		ns
t_{SDRE}	Receive Data Setup Before RCLK[1]	1.5		ns
t_{HDRE}	Receive Data Hold After RCLK[1]	4.0		ns
t_{SCLKW}	TCLK/RCLK Width	9.0		ns
t_{SCLK}	TCLK/RCLK Period	t_{CK}		ns
Internal Clock				
Timing Requirements:				
t_{SFSI}	TFS Setup Before TCLK[2]; RFS Setup Before RCLK[1]	8.0		ns
t_{HFSI}	TFS/RFS Hold After TCLK/RCLK[1]	1.0		ns
t_{SDRI}	Receive Data Setup Before RCLK[1]	3.0		ns
t_{HDRI}	Receive Data Hold After RCLK[1]	3.0		ns
External or Internal Clock				
Switching Characteristics:				
t_{DFSE}	RFS Delay After RCLK (Internally Generated RFS)[2]		13.0	ns
t_{HOFSE}	RFS Hold After RCLK (Internally Generated RFS)[2]	3.0		ns
External Clock				
Switching Characteristics:				
t_{DFSE}	TFS Delay After TCLK (Internally Generated TFS)[2]		13.0	ns
t_{HOFSE}	TFS Hold After TCLK (Internally Generated TFS)[2]	3.0		ns
t_{DDTE}	Transmit Data Delay After TCLK[2]		12.5	ns
t_{HDTE}	Transmit Data Hold After TCLK[2]	4.0		ns
Internal Clock				
Switching Characteristics:				
t_{DFSI}	TFS Delay After TCLK (Internally Generated TFS)[2]		4.5	ns
t_{HOFSI}	TFS Hold After TCLK (Internally Generated TFS)[2]	–1.5		ns
t_{DDTI}	Transmit Data Delay After TCLK[2]		7.5	ns
t_{HDTI}	Transmit Data Hold After TCLK[2]	0.0		ns
t_{SCLKIW}	TCLK/RCLK Width	$(t_{SCLK}/2) - 2.5$	$(t_{SCLK}/2) + 2.5$	ns
Enable and Three-State				
Switching Characteristics:				
t_{DTENE}	Data Enable from External TCLK[2]	5.0		ns
t_{DDTTE}	Data Disable from External RCLK[2]		10.0	ns
t_{DTENI}	Data Enable from Internal TCLK[2]	0.0		ns
t_{DDTTI}	Data Disable from Internal TCLK[2]		3.0	ns
t_{DCLK}	TCLK/RCLK Delay from CLKIN		18.0 + 6 DT	ns
t_{DPTR}	SPORT Disable After CLKIN		14.0	ns
External Late Frame Sync				
$t_{DDTLFSE}$	Data Delay from Late External TFS or External RFS with MCE = 1, MFD = 0[3, 4]		10.5	ns
$t_{DTENLFSE}$	Data Enable from late FS or MCE = 1, MFD = 0[3, 4]	3.5		ns
$t_{DDTLSCK}$	Data Delay from TCLK/RCLK for Late External TFS or External RFS with MCE = 1, MFD = 0[3, 4]		12.0	ns
$t_{DTENLSCK}$	Data Enable from RCLK/TCLK for Late External FS or MCE = 1, MFD = 0[3, 4]	4.5		ns

NOTES

To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup-and-hold, 2) data delay and data setup-and-hold, and 3) SCLK width.

[1]Referenced to sample edge.

[2]Referenced to drive edge.

[3]MCE = 1, TFS enable and TFS valid follow $t_{DDTENFS}$ and $t_{DDTLFSE}$.

[4]If external RFS/TFS setup to RCLK/TCLK > $t_{SCLK}/2$ then $t_{DDTLSCK}$ and $t_{DTENLSCK}$ apply; otherwise $t_{DDTLFSE}$ and $t_{DTENLFS}$ apply.

*Word selected timing for I^2S mode is the same as TFS/RFS timing (normal framing only).

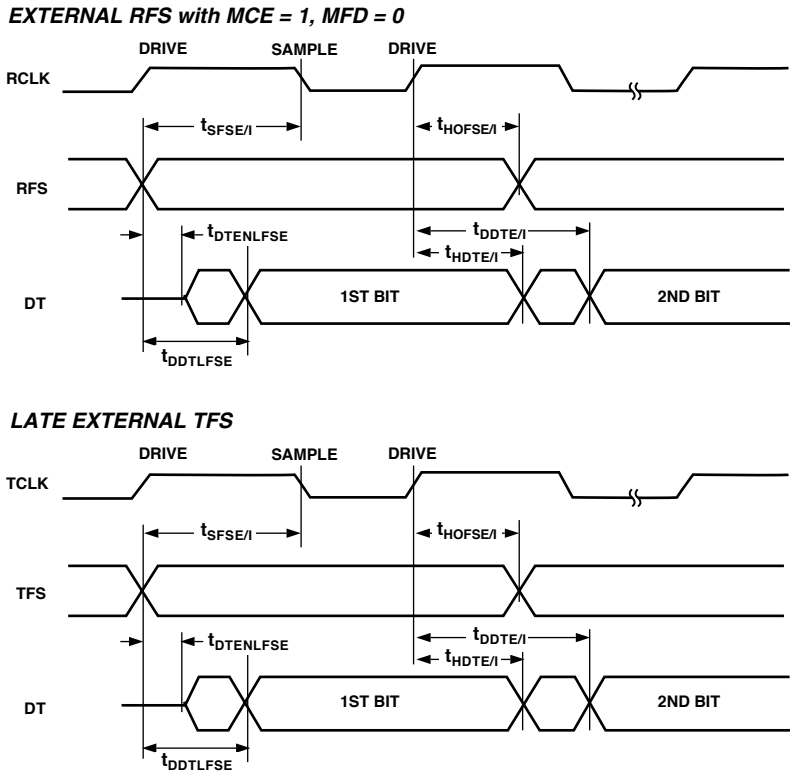

Figure 21. External Late Frame Sync (Frame Sync Setup < $t_{SCLK}/2$)

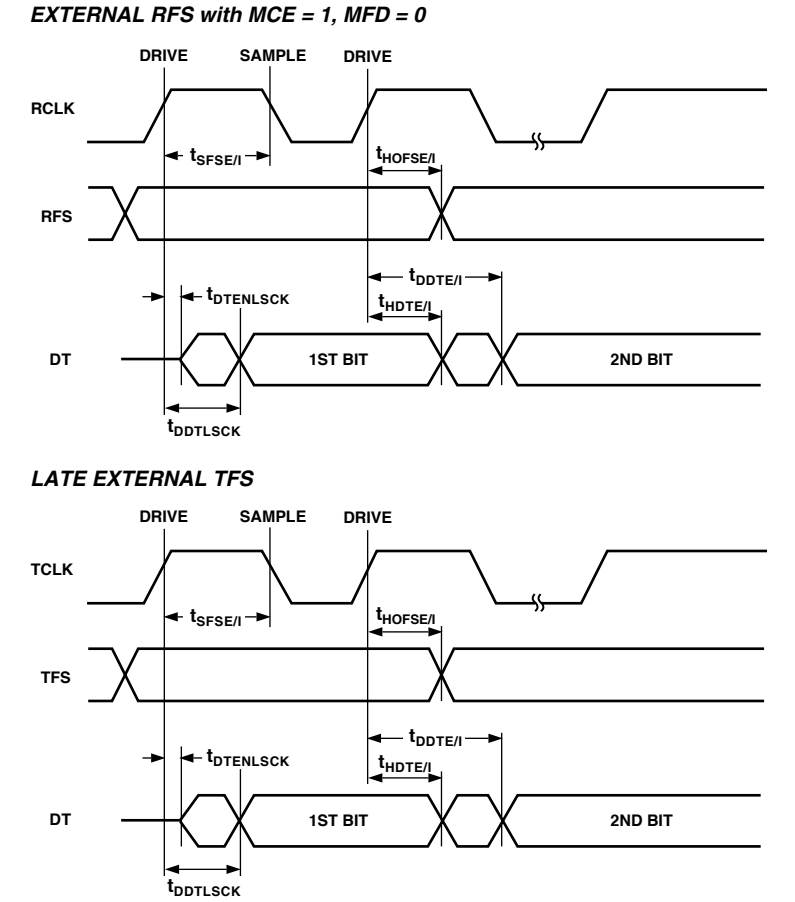

Figure 22. External Late Frame Sync (Frame Sync Setup > $t_{SCLK}/2$)

JTAG Test Access Port and Emulation

Parameter		Min	Max	Unit
Timing Requirements:				
t_{TCK}	TCK Period	t_{CK}		ns
t_{STAP}	TDI, TMS Setup Before TCK High	3.0		ns
t_{HTAP}	TDI, TMS Hold After TCK High	3.0		ns
t_{SSYS}	System Inputs Setup Before TCK Low[1]	7.0		ns
t_{HSYS}	System Inputs Hold After TCK Low[1]	12.0		ns
t_{TRSTW}	$\overline{TRST}$ Pulsewidth	4 t_{CK}		ns
Switching Characteristics:				
t_{DTDO}	TDO Delay from TCK Low		11.0	ns
t_{DSYS}	System Outputs Delay After TCK Low[2]		15.0	ns

NOTES
[1]System Inputs = $DATA_{31-0}$, $ADDR_{23-0}$, $\overline{RD}$, $\overline{WR}$, ACK, $\overline{SBTS}$, $\overline{SW}$, $\overline{HBR}$, $\overline{HBG}$, $\overline{CS}$, $\overline{DMAR_1}$, $\overline{DMAR_2}$, $\overline{BR_{2-1}}$, ID_{1-0}, $\overline{IRQ_{2-0}}$, $FLAG_{11-0}$, DR0x, DR1x, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, BSEL, $\overline{BMS}$, CLKIN, $\overline{RESET}$, $SDCLK_0$, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, SDCKE, PWM_EVENTx.
[2]System Outputs = $DATA_{31-0}$, $ADDR_{23-0}$, MS_{3-0}, $\overline{RD}$, $\overline{WR}$, ACK, $\overline{SW}$, $\overline{HBG}$, REDY, DMAG1, DMAG2, $\overline{BR_{2-1}}$, $\overline{CPA}$, $FLAG_{11-0}$, PWM_EVENTx, DT0x, DT1x, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $\overline{BMS}$, SDCLK0, SDCLK1, DQM, SDA10, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, SDCKE, BM, XTAL.

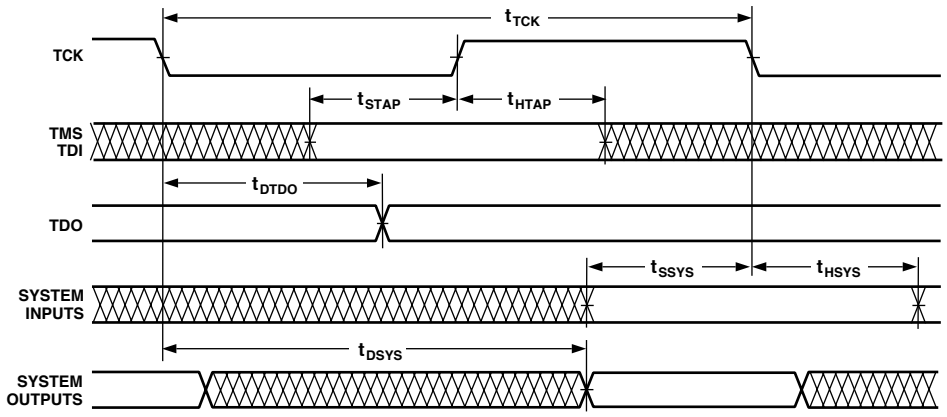

Figure 23. JTAG Test Access Port and Emulation

OUTPUT DRIVE CURRENT

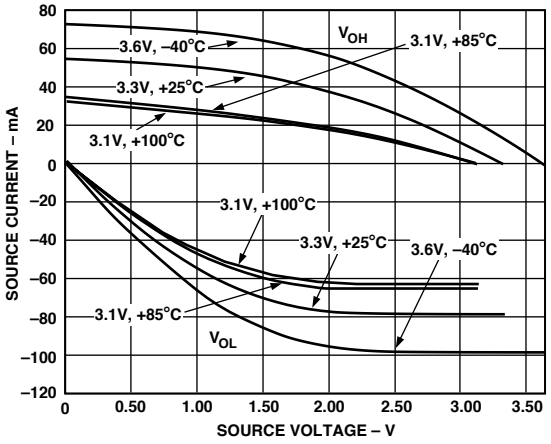

Figure 24. Typical Drive Currents

TEST CONDITIONS

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L and the load current, I_L. This decay time can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times \Delta V}{I_L}$$

The output disable time t_{DIS} is the difference between $t_{MEASURED}$ and t_{DECAY} as shown in Figure 26. The time $t_{MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.5 V.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to when they start driving. The output enable time t_{ENA} is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-21065L's output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (i.e., t_{DATRWH} for the write cycle).

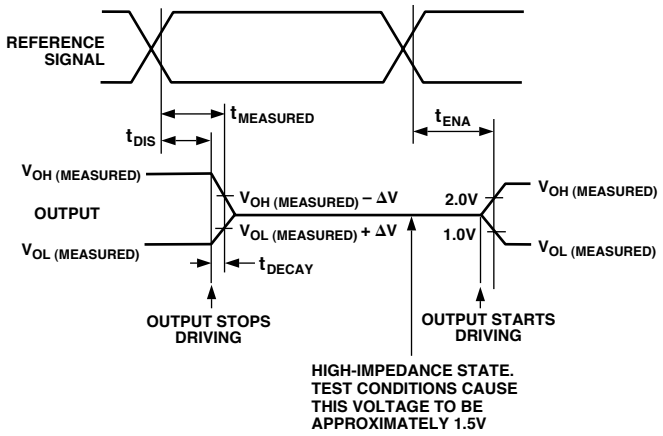

Figure 25. Output Enable

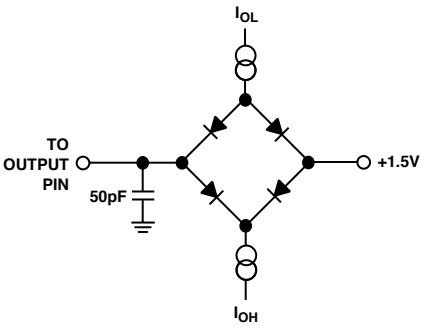

Figure 26. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

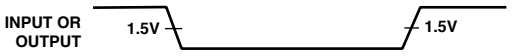

Figure 27. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 50 pF on all pins. The delay and hold specifications given should be derated by a factor of l.8 ns/50 pF for loads other than the nominal value of 50 pF. Figure 28 and Figure 29 show how output rise time varies with capacitance. Figure 30 shows graphically how output delays and hold vary with load capacitance. (Note that this graph or derating does not apply to output disable delays; see the previous section Output Disable time under Test Conditions.) The graphs of Figure 28, Figure 29, and Figure 30 may not be linear outside the ranges shown.

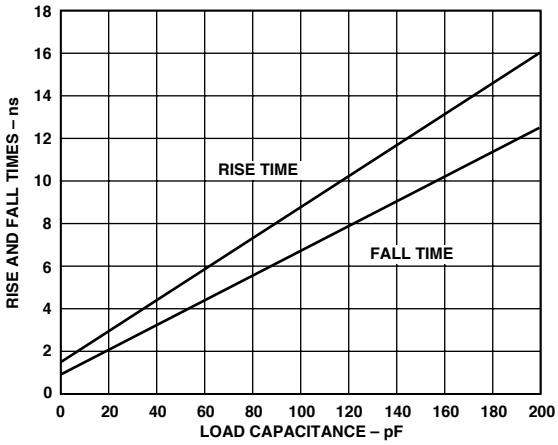

Figure 28. Typical Rise and Fall Time (10%–90% V_{DD})

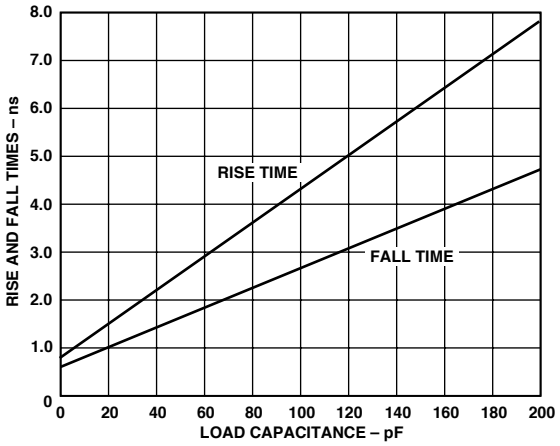

Figure 29. Typical Rise and Fall Time (0.8 V–2.0 V)

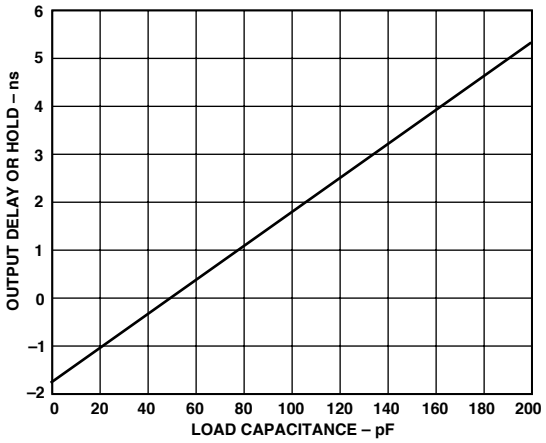

Figure 30. Typical Output Delay or Hold

POWER DISSIPATION

Total power dissipation has two components: one due to internal circuitry and one due to the switching of external output drivers. Internal power dissipation depends on the sequence in which instructions execute and the data operands involved. See I_{DDIN} calculation in Electrical Characteristics section. Internal power dissipation is calculated this way:

$$P_{INT} = I_{DDIN} \times V_{DD}$$

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

– the number of output pins that switch during each cycle (O)
– the maximum frequency at which the pins can switch (f)
– the load capacitance of the pins (C)
– the voltage swing of the pins (V_{DD}).

The external component is calculated using:

$$P_{EXT} = O \times C \times V_{DD}^2 \times f$$

The load capacitance should include the processor's package capacitance (C_{IN}). The frequency f includes driving the load high and then back low. Address and data pins can drive high and low at a maximum rate of $1/t_{CK}$ while in SDRAM burst mode.

Example:

Estimate P_{EXT} with the following assumptions:

– a system with one bank of external memory (32-bit)
– two 1M × 16 SDRAM chips, each with a control signal load of 3 pF and a data signal load of 4 pF
– external data writes occur in burst mode, two every $1/t_{CK}$ cycles, a potential frequency of $1/t_{CK}$ cycles/s. Assume 50% pin switching
– the external SDRAM clock rate is 60 MHz ($2/t_{CK}$).

The P_{EXT} equation is calculated for each class of pins that can drive:

Table V. External Power Calculations

Pin Type	# of Pins	% Switching	× C	× f	× V_{DD}^2	= P_{EXT}
Address	11	50	× 10.7	× 30 MHz	× 10.9 V	= 0.019 W
$\overline{MS_0}$	1	0	× 10.7	—	× 10.9 V	= 0.000 W
$\overline{SDWE}$	1	0	× 10.7	—	× 10.9 V	= 0.000 W
Data	32	50	× 7.7	× 30 MHz	× 10.9 V	= 0.042 W
SDRAM CLK	1	–	× 10.7	× 30 MHz	× 10.9 V	= 0.007 W

P_{EXT} = 0.068 W

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation. (I_{DDIN} see calculation in Electrical Characteristics section):

$$P_{TOTAL} = P_{EXT} + (I_{DDIN} \times V_{DD})$$

Note that the conditions causing a worst-case P_{EXT} differ from those causing a worst-case P_{INT}. Maximum P_{INT} cannot occur while 100% of the output pins are switching from all ones (1s) to all zeros (0s). Note also that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

ENVIRONMENTAL CONDITIONS

Thermal Characteristics

The ADSP-21065L is offered in a 208-lead MQFP and a 196-ball Mini-BGA package.

The ADSP-21065L is specified for a case temperature (T_{CASE}). To ensure that T_{CASE} is not exceeded, an air flow source may be used.

$$T_{CASE} = T_{AMB} + (PD \times \theta_{CA})$$

T_{CASE} = Case temperature (measured on top surface of package)

PD = Power Dissipation in W (this value depends upon the specific application; a method for calculating PD is shown under Power Dissipation)

θ_{JC} = 7.1°C/W for 208-lead MQFP
θ_{JC} = 5.1°C/W for 196-ball Mini-BGA

Airflow

Table VI. Thermal Characteristics (208-Lead MQFP)

(Linear Ft./Min.)	0	100	200	400	600
θ_{CA} (°C/W)	24	20	19	17	13

Table VII. 196-Ball Mini-BGA

(Linear Ft./Min.)	0	200	400
θ_{CA} (°C/W)	38	29	23

208-LEAD MQFP PIN CONFIGURATION

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	VDD	43	$\overline{\text{CAS}}$	85	VDD	127	DATA28	169	ADDR17
2	RFS0	44	$\overline{\text{SDWE}}$	86	DATA3	128	DATA29	170	ADDR16
3	GND	45	VDD	87	DATA4	129	GND	171	ADDR15
4	RCLK0	46	DQM	88	DATA5	130	VDD	172	VDD
5	DR0A	47	SDCKE	89	GND	131	VDD	173	ADDR14
6	DR0B	48	SDA10	90	DATA6	132	DATA30	174	ADDR13
7	TFS0	49	GND	91	DATA7	133	DATA31	175	ADDR12
8	TCLK0	50	$\overline{\text{DMAG}}$1	92	DATA8	134	FLAG7	176	VDD
9	VDD	51	$\overline{\text{DMAG}}$2	93	VDD	135	GND	177	GND
10	GND	52	$\overline{\text{HBG}}$	94	GND	136	FLAG6	178	ADDR11
11	DT0A	53	BMSTR	95	VDD	137	FLAG5	179	ADDR10
12	DT0B	54	VDD	96	DATA9	138	FLAG4	180	ADDR9
13	RFS1	55	$\overline{\text{CS}}$	97	DATA10	139	GND	181	GND
14	GND	56	$\overline{\text{SBTS}}$	98	DATA11	140	VDD	182	VDD
15	RCLK1	57	GND	99	GND	141	VDD	183	ADDR8
16	DR1A	58	$\overline{\text{WR}}$	100	DATA12	142	NC	184	ADDR7
17	DR1B	59	$\overline{\text{RD}}$	101	DATA13	143	ID1	185	ADDR6
18	TFS1	60	GND	102	NC	144	ID0	186	GND
19	TCLK1	61	VDD	103	NC	145	$\overline{\text{EMU}}$	187	GND
20	VDD	62	GND	104	DATA14	146	TDO	188	ADDR5
21	VDD	63	REDY	105	VDD	147	$\overline{\text{TRST}}$	189	ADDR4
22	DT1A	64	$\overline{\text{SW}}$	106	GND	148	TDI	190	ADDR3
23	DT1B	65	$\overline{\text{CPA}}$	107	DATA15	149	TMS	191	VDD
24	PWM_EVENT1	66	VDD	108	DATA16	150	GND	192	VDD
25	GND	67	VDD	109	DATA17	151	TCK	193	ADDR2
26	PWM_EVENT0	68	GND	110	VDD	152	BSEL	194	ADDR1
27	$\overline{\text{BR1}}$	69	ACK	111	DATA18	153	$\overline{\text{BMS}}$	195	ADDR0
28	$\overline{\text{BR2}}$	70	$\overline{\text{MS}}$0	112	DATA19	154	GND	196	GND
29	VDD	71	$\overline{\text{MS}}$1	113	DATA20	155	GND	197	FLAG0
30	CLKIN	72	GND	114	GND	156	VDD	198	FLAG1
31	XTAL	73	GND	115	NC	157	$\overline{\text{RESET}}$	199	FLAG2
32	VDD	74	$\overline{\text{MS}}$2	116	DATA21	158	VDD	200	VDD
33	GND	75	$\overline{\text{MS}}$3	117	DATA22	159	GND	201	FLAG3
34	SDCLK1	76	FLAG11	118	DATA23	160	ADDR23	202	NC
35	GND	77	VDD	119	GND	161	ADDR22	203	NC
36	VDD	78	FLAG10	120	VDD	162	ADDR21	204	GND
37	SDCLK0	79	FLAG9	121	DATA24	163	VDD	205	$\overline{\text{IRQ}}$0
38	$\overline{\text{DMAR}}$1	80	FLAG8	122	DATA25	164	ADDR20	206	$\overline{\text{IRQ}}$1
39	$\overline{\text{DMAR}}$2	81	GND	123	DATA26	165	ADDR19	207	$\overline{\text{IRQ}}$2
40	$\overline{\text{HBR}}$	82	DATA0	124	VDD	166	ADDR18	208	NC
41	GND	83	DATA1	125	GND	167	GND		
42	$\overline{\text{RAS}}$	84	DATA2	126	DATA27	168	GND		