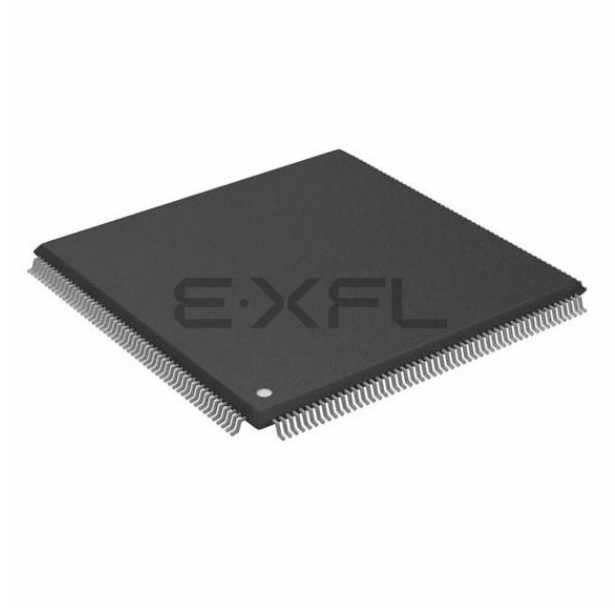

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	Host Interface, Serial Port
Clock Rate	60MHz
Non-Volatile Memory	External
On-Chip RAM	64kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 100°C (TC)
Mounting Type	Surface Mount
Package / Case	208-BFQFP
Supplier Device Package	208-MQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21065lcsz-240

ADSP-21065L* PRODUCT PAGE QUICK LINKS

Last Content Update: 04/08/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- EE-103: Performing Level Conversion Between 5v and 3.3v IC's
- EE-104: Setting Up Streams with the VisualDSP Debugger
- EE-107: ADSP-21065L EPROM Booting
- EE-109: ADSP2106x : Using 2106x SPORT's as Timers
- EE-110: A Quick Primer on ELF and DWARF File Formats
- EE-112: Class Implementation in Analog C++
- EE-116: SHARC Shortword DMA
- EE-127: The ADSP-21065L On-chip SDRAM Controller
- EE-128: DSP in C++: Calling Assembly Class Member Functions From C++
- EE-132: Placing C Code and Data Modules in SHARC memory using VisualDSP++™
- EE-141: Benchmarking C Code on the ADSP-2106x and the ADSP-2116x Family of DSPs
- EE-159: Initializing DSP System & Control Registers From C and C++
- EE-166: ADSP-2106x EPROM Overlay Support with VisualDSP++ 2.0
- EE-175: Emulator and Evaluation Hardware Troubleshooting Guide for VisualDSP++ Users
- EE-191: Implementing a Glueless UART Using The SHARC® DSP SPORTs
- EE-202: Using the Expert Linker for Multiprocessor LDFs
- EE-219: Connecting Character LCD Panels to ADSP-21262 SHARC® DSPs
- EE-244: Interfacing Gated Clocks to ADSP-21065L SHARC® Processors
- EE-247: Interfacing AD7676 ADCs to ADSP-21065L SHARC® Processors
- EE-253: Power Bypass Decoupling of SHARC® Processors
- EE-261: Understanding Jitter Requirements of PLL-Based Processors
- EE-267: Implementing In-Place FFTs on SISD and SIMD SHARC® Processors
- EE-273: Using the VisualDSP++ Command-Line Installer
- EE-280: In-Circuit Flash Programming on ADSP-2106x SHARC® Processors
- EE-285: Migrating from ADSP-21065L to ADSP-21375 SHARC® Processors

- EE-305: Designing and Debugging Systems with SHARC Processors
- EE-323: Implementing Dynamically Loaded Software Modules
- EE-328: Migrating from ADSP-2106x/2116x to ADSP-2126x/2136x/2137x SHARC® Processors
- EE-330: Windows Vista Compatibility in VisualDSP++ 5.0 Development Tools
- EE-332: Cycle Counting and Profiling
- EE-340: Connecting SHARC® and Blackfin® Processors over SPI
- EE-42: C-Programs on the ADSP-2106x
- EE-45: Using the ADSP-2106x/21020 EZ-ICE DBWIN Utility
- EE-46: SHARC Internal Power Measurements
- EE-47: ADSP-2106x Link Ports - Maximum Throughput
- EE-56: Tips and Tricks on SHARC® EPROM and Host Boot Loader
- EE-62: Accessing Short Word Memory In C
- EE-68: Analog Devices JTAG Emulation Technical Reference
- EE-69: Understanding and Using Linker Description Files on SHARC Processors
- EE-70: ADSP-2106x SPORT DTx pins: Is There Potential MCM Data Contention Between Different SHARCs
- EE-74: Analog Devices Serial Port Development and Troubleshooting Guide
- EE-84: External Port DMA Modes of Operation for SHARC Processors
- EE-85: Recommended Handling of Unused SHARC Pins
- EE-86: Interfacing SHARC 2106x DSPs to PLX 9080 PCI Bridge Chips
- EE-98: Using External Bus Arbitration to Group More Than Two ADSP-21065L into a Multiprocessing Cluster
- Interfacing the ADSP21065L SHARC DSP to the AD1819A AC-97 Soundport Codec
- TN: Interfacing I2S Compatible Audio Devices to the ADSP-21065L
- TN: Using the Low Cost, High Performance ADSP21065L DSP for Digital Audio Applications

Data Sheet

- ADSP-21065L: SHARC, 198 MFLOPS, 3.3v Data Sheet

Evaluation Kit Manuals

- ADSP-21061, 21065L and the 21160M EZ-KIT Lite® Installation Procedure

Integrated Circuit Anomalies

- ADSP-21065L Anomaly List for Revision 0.0, 0.1, 0.2, 0.3

Processor Manuals

- ADSP-21065L Technical Reference
- ADSP-21065L User's Manual
- Getting Started with SHARC
- SHARC Processors: Manuals

Product Highlight

- ADSP-21065L SHARC DSP 32-Bit Floating Point Performance Product Highlight
- EZ-KIT Lite for ADSP-21065L SHARC DSP Product Highlight
- SHARC Processor Family

SOFTWARE AND SYSTEMS REQUIREMENTS

- Software and Tools Anomalies Search

TOOLS AND SIMULATIONS

- ADSP-21065L: MBGA Package
- ADSP-21065L: PQFP package
- Designing with BGA
- ADSP-21065L IBIS Datafile (QFP Package)

REFERENCE MATERIALS

Product Selection Guide

- ADI Complementary Parts Guide - Supervisory Devices and DSP Processors

Technical Articles

- An Efficient Asynchronous Sampling-rate Conversion Algorithm for Multi-channel Audio Applications

DESIGN RESOURCES

- ADSP-21065L Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The ADSP-21065L's two DAGs contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reducing overhead, increasing performance, and simplifying implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set
The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the ADSP-21065L can conditionally execute a multiply, an add, a subtract and a branch, all in a single instruction.

ADSP-21065L FEATURES

The ADSP-21065L is designed to achieve the highest system throughput to enable maximum system performance. It can be clocked by either a crystal or a TTL-compatible clock signal. The ADSP-21065L uses an input clock with a frequency equal to half the instruction rate—a 33 MHz input clock yields a 15 ns processor cycle (which is equivalent to 66 MHz). Interfaces on the ADSP-21065L operate as shown below. Hereafter in this document, 1x = input clock frequency, and 2x = processor's instruction rate.

The following clock operation ratings are based on 1x = 33 MHz (instruction rate/core = 66 MHz):

SDRAM	66 MHz
External SRAM	33 MHz
Serial Ports	33 MHz
Multiprocessing	33 MHz
Host (Asynchronous)	33 MHz

Augmenting the ADSP-21000 family core, the ADSP-21065L adds the following architectural features:

Dual-Ported On-Chip Memory
The ADSP-21065L contains 544 Kbits of on-chip SRAM, organized into two banks: Bank 0 has 288 Kbits, and Bank 1 has 256 Kbits. Bank 0 is configured with 9 columns of 2K × 16 bits, and Bank 1 is configured with 8 columns of 2K × 16 bits. Each memory block is dual-ported for single-cycle, independent accesses by the core processor and I/O processor or DMA controller. The dual-ported memory and separate on-chip buses allow two data transfers from the core and one from I/O, all in a single cycle (see Figure 4 for the ADSP-21065L Memory Map).

On the ADSP-21065L, the memory can be configured as a maximum of 16K words of 32-bit data, 34K words for 16-bit data, 10K words of 48-bit instructions (and 40-bit data) or combinations of different word sizes up to 544 Kbits. All the memory can be accessed as 16-bit, 32-bit or 48-bit.

While each memory block can store combinations of code and data, accesses are most efficient when one block stores data, using the DM bus for transfers, and the other block stores instructions and data, using the PM bus for transfers. Using the DM and PM busses in this way, with one dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache. Single-cycle execution is also maintained when one of the data operands is transferred to or from off-chip, via the ADSP-21065L's external port.

Off-Chip Memory and Peripherals Interface
The ADSP-21065L's external port provides the processor's interface to off-chip memory and peripherals. The 64M words, off-chip address space is included in the ADSP-21065L's unified address space. The separate on-chip buses—for program memory, data memory and I/O—are multiplexed at the external port to create an external system bus with a single 24-bit address bus, four memory selects, and a single 32-bit data bus. The on-chip Super Harvard Architecture provides three bus performance, while the off-chip unified address space gives flexibility to the designer.

SDRAM Interface
The SDRAM interface enables the ADSP-21065L to transfer data to and from synchronous DRAM (SDRAM) at 2x clock frequency. The synchronous approach coupled with 2x clock frequency supports data transfer at a high throughput—up to 220 Mbytes/sec.

The SDRAM interface provides a glueless interface with standard SDRAMs—16 Mb, 64 Mb, and 128 Mb—and includes options to support additional buffers between the ADSP-21065L and SDRAM. The SDRAM interface is extremely flexible and provides capability for connecting SDRAMs to any one of the ADSP-21065L's four external memory banks.

Systems with several SDRAM devices connected in parallel may require buffering to meet overall system timing requirements. The ADSP-21065L supports pipelining of the address and control signals to enable such buffering between itself and multiple SDRAM devices.

Host Processor Interface
The ADSP-21065L's host interface provides easy connection to standard microprocessor buses—8-, 16-, and 32-bit—requiring little additional hardware. Supporting asynchronous transfers at speeds up to 1x clock frequency, the host interface is accessed through the ADSP-21065L's external port. Two channels of DMA are available for the host interface; code and data transfers are accomplished with low software overhead.

The host processor requests the ADSP-21065L's external bus with the host bus request ($\overline{\text{HBR}}$), host bus grant ($\overline{\text{HBG}}$), and ready (REDY) signals. The host can directly read and write the IOP registers of the ADSP-21065L and can access the DMA channel setup and mailbox registers. Vector interrupt support enables efficient execution of host commands.

DMA Controller
The ADSP-21065L's on-chip DMA controller allows zero-overhead, nonintrusive data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions.

DMA transfers can occur between the ADSP-21065L's internal memory and either external memory, external peripherals, or a host processor. DMA transfers can also occur between the ADSP-21065L's internal memory and its serial ports. DMA transfers between external memory and external peripheral devices are another option. External bus packing to 16-, 32-, or 48-bit internal words is performed during DMA transfers.

Ten channels of DMA are available on the ADSP-21065L—eight via the serial ports, and two via the processor's external port (for either host processor, other ADSP-21065L, memory or

PIN DESCRIPTIONS

ADSP-21065L pin definitions are listed below. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$).

Unused inputs should be tied or pulled to VDD or GND, except for $\text{ADDR}_{23\text{-}0}$, $\text{DATA}_{31\text{-}0}$, $\text{FLAG}_{11\text{-}0}$, $\overline{\text{SW}}$, and inputs that have internal pull-up or pull-down resistors ($\overline{\text{CPA}}$, ACK, DTxX, DRxX, TCLKx, RCLKx, TMS, and TDI)—these pins can be left floating. These pins have a logic-level hold circuit that prevents the input from floating internally.

I = Input S = Synchronous P = Power Supply (O/D) = Open Drain
O = Output A = Asynchronous G = Ground (A/D) = Active Drive
T = Three-state (when $\overline{\text{SBTS}}$ is asserted, or when the ADSP-2106x is a bus slave)

Pin	Type	Function
$\text{ADDR}_{23\text{-}0}$	I/O/T	**External Bus Address**. The ADSP-21065L outputs addresses for external memory and peripherals on these pins. In a multiprocessor system the bus master outputs addresses for read/writes of the IOP registers of the other ADSP-21065L. The ADSP-21065L inputs addresses when a host processor or multiprocessing bus master is reading or writing its IOP registers.
$\text{DATA}_{31\text{-}0}$	I/O/T	**External Bus Data**. The ADSP-21065L inputs and outputs data and instructions on these pins. The external data bus transfers 32-bit single-precision floating-point data and 32-bit fixed-point data over bits 31-0. 16-bit short word data is transferred over bits 15-0 of the bus. Pull-up resistors on unused DATA pins are not necessary.
$\overline{\text{MS}}_{3\text{-}0}$	I/O/T	**Memory Select Lines**. These lines are asserted as chip selects for the corresponding banks of external memory. Internal $\text{ADDR}_{25\text{-}24}$ are decoded into $\overline{\text{MS}}_{3\text{-}0}$. The $\overline{\text{MS}}_{3\text{-}0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the $\overline{\text{MS}}_{3\text{-}0}$ lines are inactive; they are active, however, when a conditional memory access instruction is executed, whether or not the condition is true. Additionally, an $\overline{\text{MS}}_{3\text{-}0}$ line which is mapped to SDRAM may be asserted even when no SDRAM access is active. In a multiprocessor system, the $\overline{\text{MS}}_{3\text{-}0}$ lines are output by the bus master.
$\overline{\text{RD}}$	I/O/T	**Memory Read Strobe**. This pin is asserted when the ADSP-21065L reads from external memory devices or from the IOP register of another ADSP-21065L. External devices (including another ADSP-21065L) must assert $\overline{\text{RD}}$ to read from the ADSP-21065L's IOP registers. In a multiprocessor system, $\overline{\text{RD}}$ is output by the bus master and is input by another ADSP-21065L.
$\overline{\text{WR}}$	I/O/T	**Memory Write Strobe.** This pin is asserted when the ADSP-21065L writes to external memory devices or to the IOP register of another ADSP-21065L. External devices must assert $\overline{\text{WR}}$ to write to the ADSP-21065L's IOP registers. In a multiprocessor system, $\overline{\text{WR}}$ is output by the bus master and is input by the other ADSP-21065L.
$\overline{\text{SW}}$	I/O/T	**Synchronous Write Select.** This signal interfaces the ADSP-21065L to synchronous memory devices (including another ADSP-21065L). The ADSP-21065L asserts $\overline{\text{SW}}$ to provide an early indication of an impending write cycle, which can be aborted if $\overline{\text{WR}}$ is not later asserted (e.g., in a conditional write instruction). In a multiprocessor system, $\overline{\text{SW}}$ is output by the bus master and is input by the other ADSP-21065L to determine if the multiprocessor access is a read or write. $\overline{\text{SW}}$ is asserted at the same time as the address output.
ACK	I/O/S	**Memory Acknowledge**. External devices can deassert ACK to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access. The ADSP-21065L deasserts ACK as an output to add wait states to a synchronous access of its IOP registers. In a multiprocessor system, a slave ADSP-21065L deasserts the bus master's ACK input to add wait state(s) to an access of its IOP registers. The bus master has a keeper latch on its ACK pin that maintains the input at the level to which it was last driven.
$\overline{\text{SBTS}}$	I/S	**Suspend Bus Three-State.** External devices can assert $\overline{\text{SBTS}}$ to place the external bus address, data, selects, and strobes—but not SDRAM control pins—in a high impedance state for the following cycle. If the ADSP-21065L attempts to access external memory while $\overline{\text{SBTS}}$ is asserted, the processor will halt and the memory access will not finish until $\overline{\text{SBTS}}$ is deasserted. $\overline{\text{SBTS}}$ should only be used to recover from host processor/ADSP-21065L deadlock.
$\overline{\text{IRQ}}_{2\text{-}0}$	I/A	Interrupt Request Lines. May be either edge-triggered or level-sensitive.
$\text{FLAG}_{11\text{-}0}$	I/O/A	Flag Pins. Each is configured via control bits as either an input or an output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals.

ADSP-21065L–SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter		Test Conditions	C Grade Min	C Grade Max	K Grade Min	K Grade Max	Unit
V_{DD}	Supply Voltage		3.13	3.60	3.13	3.60	V
T_{CASE}	Case Operating Temperature		–40	+100	0	+85	°C
V_{IH}	High Level Input Voltage	@ V_{DD} = max	2.0	V_{DD} + 0.5	2.0	V_{DD} + 0.5	V
V_{IL1}	Low Level Input Voltage[1]	@ V_{DD} = min	–0.5	0.8	–0.5	0.8	V
V_{IL2}	Low Level Input Voltage[2]	@ V_{DD} = min	–0.5	0.7	–0.5	0.7	V

NOTE
See Environmental Conditions for information on thermal specifications.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	C and K Grades Min	C and K Grades Max	Unit
V_{OH}	High Level Output Voltage[3]	@ V_{DD} = min, I_{OH} = –2.0 mA[4]	2.4		V
V_{OL}	Low Level Output Voltage[3]	@ V_{DD} = min, I_{OL} = 4.0 mA[4]		0.4	V
I_{IH}	High Level Input Current[5]	@ V_{DD} = max, V_{IN} = V_{DD} max		10	µA
I_{IL}	Low Level Input Current[5]	@ V_{DD} = max, V_{IN} = 0 V		10	µA
I_{ILP}	Low Level Input Current[6]	@ V_{DD} = max, V_{IN} = 0 V		150	µA
I_{OZH}	Three-State Leakage Current[7, 8, 9, 10]	@ V_{DD} = max, V_{IN} = V_{DD} max		10	µA
I_{OZL}	Three-State Leakage Current[7]	@ V_{DD} = max, V_{IN} = 0 V		8	µA
I_{OZLS}	Three-State Leakage Current[8]	@ V_{DD} = max, V_{IN} = 0 V		150	µA
I_{OZLA}	Three-State Leakage Current[11]	@ V_{DD} = max, V_{IN} = 1.5 V		350	µA
I_{OZLAR}	Three-State Leakage Current[10]	@ V_{DD} = max, V_{IN} = 0 V		4	mA
I_{OZLC}	Three-State Leakage Current[9]	@ V_{DD} = max, V_{IN} = 0 V		1.5	mA
C_{IN}	Input Capacitance[12, 13]	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		8	pF

NOTES
[1] Applies to input and bidirectional pins: $DATA_{31-0}$, $ADDR_{23-0}$, BSEL, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $\overline{SBTS}$, $\overline{IRQ}_{2-0}$, $FLAG_{11-0}$, $\overline{HBG}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR}_{2-1}$, $\overline{ID}_{2-0}$, RPBA, $\overline{CPA}$, TFS0, TFS1, RFS0, RFS1, $\overline{BMS}$, TMS, TDI, TCK, $\overline{HBR}$, DR0A, DR1A, DR0B, DR1B, TCLK0, TCLK1, RCLK0, RCLK1, $\overline{RESET}$, $\overline{TRST}$, PWM_EVENT0, PWM_EVENT1, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, $\overline{SDCKE}$.
[2] Applies to input pin CLKIN.
[3] Applies to output and bidirectional pins: $DATA_{31-0}$, $ADDR_{23-0}$, MS_{3-0}, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $FLAG_{11-0}$, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR}_{2-1}$, $\overline{CPA}$, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, DT0A, DT1A, DT0B, DT1B, XTAL, $\overline{BMS}$, TDO, $\overline{EMU}$, BMSTR, PWM_EVENT0, PWM_EVENT1, $\overline{RAS}$, $\overline{CAS}$, DQM, $\overline{SDWE}$, SDCLK0, SDCLK1, $\overline{SDCKE}$, SDA10.
[4] See Output Drive Currents for typical drive current capabilities.
[5] Applies to input pins: ACK, $\overline{SBTS}$, $\overline{IRQ}_{2-0}$, $\overline{HBR}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, ID_{1-0}, BSEL, CLKIN, $\overline{RESET}$, TCK (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID_{1-0} = 01 and another ADSP-21065L is not requesting bus mastership.)
[6] Applies to input pins with internal pull-ups: DR0A, DR1A, DR0B, DR1B, $\overline{TRST}$, TMS, TDI.
[7] Applies to three-statable pins: $DATA_{31-0}$, $ADDR_{23-0}$, $\overline{MS}_{3-0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $FLAG_{11-0}$, REDY, $\overline{HBG}$, $\overline{DMAG}_1$, $\overline{DMAG}_2$, $\overline{BMS}$, TDO, $\overline{RAS}$, $\overline{CAS}$, DQM, $\overline{SDWE}$, SDCLK0, SDCLK1, $\overline{SDCKE}$, SDA10, and $\overline{EMU}$ (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID_{1-0} = 01 and another ADSP-21065L is not requesting bus mastership).
[8] Applies to three-statable pins with internal pull-ups: DT0A, DT1A, DT0B, DT1B, TCLK0, TCLK1, RCLK0, RCLK1.
[9] Applies to $\overline{CPA}$ pin.
[10] Applies to ACK pin when pulled up.
[11] Applies to ACK pin when keeper latch enabled.
[12] Guaranteed but not tested.
[13] Applies to all signal pins.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . –0.3 V to +4.6 V
Input Voltage . . . . . –0.5 V to V_{DD} + 0.5 V
Output Voltage Swing . . . . . –0.5 V to V_{DD} + 0.5 V
Load Capacitance . . . . . 200 pF
Junction Temperature Under Bias . . . . . 130°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (5 seconds) . . . . . 280°C

*Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADSP-21065L features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

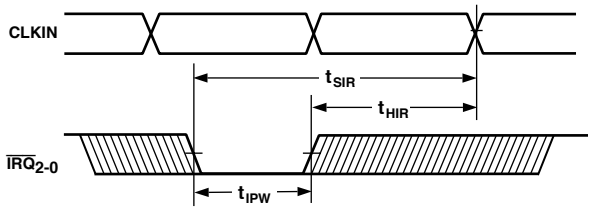


Figure 9. Interrupts

Parameter		Min	Max	Unit
Timer				
Timing Requirements:				
t_{STI}	Timer Setup Before SDCLK High	0.0		ns
t_{HTI}	Timer Hold After SDCLK High	6.0		ns
Switching Characteristics:				
t_{DTEX}	Timer Delay After SDCLK High		1.0	ns
t_{HTEX}	Timer Hold After SDCLK High	–5.0		ns

Parameter		Min	Max	Unit
Flags				
Timing Requirements:				
t_{SFI}	$FLAG_{11-0}$IN Setup Before SDCLK High[1]	–2.0		ns
t_{HFI}	$FLAG_{11-0}$IN Hold After SDCLK High[1]	6.0		ns
Switching Characteristics:				
t_{DFO}	$FLAG_{11-0}$OUT Delay After SDCLK High		1.0	ns
t_{HFO}	$FLAG_{11-0}$OUT Hold After SDCLK High	–4.0		ns
t_{DFOE}	SDCLK High to $FLAG_{11-0}$OUT Enable	–4.0		ns
t_{DFOD}	SDCLK High to $FLAG_{11-0}$OUT Disable		–1.75	ns

NOTE
[1]Flag inputs meeting these setup and hold times will affect conditional instructions in the following instruction cycle.

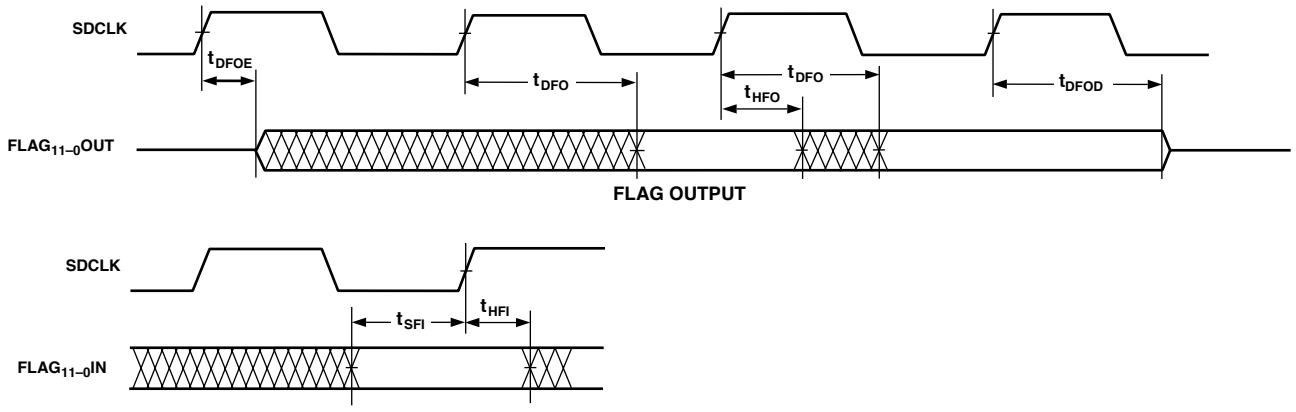


Figure 10. Flags

Memory Write—Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the ADSP-21065L is the bus master when accessing external memory space. These switching characteristics also apply for bus master synchronous read/write timing (see Synchronous Read/Write—Bus Master below). If these timing requirements are met, the synchronous read/write timing can be ignored (and vice versa). An exception to this is the ACK pin timing requirements as described in the note below.

Parameter		Min	Max	Unit
Timing Requirements:				
t_{DAAK}	ACK Delay from Address[1, 2]		24.0 + 30 DT + W	ns
t_{DSAK}	ACK Delay from $\overline{WR}$ Low[1]		19.5 + 24 DT + W	ns
Switching Characteristics:				
t_{DAWH}	Address, Selects to $\overline{WR}$ Deasserted[2]	29.0 + 31 DT + W		ns
t_{DAWL}	Address, Selects to $\overline{WR}$ Low[2]	3.5 + 6 DT		ns
t_{WW}	$\overline{WR}$ Pulsewidth	24.5 + 25 DT + W		ns
t_{DDWH}	Data Setup Before $\overline{WR}$ High	15.5 + 19 DT + W		ns
t_{DWHA}	Address Hold After $\overline{WR}$ Deasserted	0.0 + 1 DT + H		ns
t_{DATRWH}	Data Disable After $\overline{WR}$ Deasserted[3]	1.0 + 1 DT + H	4.0 + 1 DT + H	ns
t_{WWR}	$\overline{WR}$ High to $\overline{WR}$, $\overline{RD}$ Low	4.5 + 7 DT + H		ns
t_{WRDGL}	$\overline{WR}$ High to $\overline{DMAG}$x Low	11.0 + 13 DT + H		ns
t_{DDWR}	Data Disable Before $\overline{WR}$ or $\overline{RD}$ Low	3.5 + 6 DT + I		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	4.5 + 6 DT		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
H = t_{CK} (if an address hold cycle occurs, as specified in WAIT register; otherwise H = 0).
I = t_{CK} (if a bus idle cycle occurs, as specified in WAIT register; otherwise I = 0).

NOTES

[1]ACK is not sampled on external memory accesses that use the *Internal* wait state mode. For the first CLKIN cycle of a new external memory access, ACK must be valid by t_{DAAK} or t_{DSAK} or synchronous specification t_{SACKC} for wait state modes *External*, *Either*, or *Both* (*Both*, if the internal wait state is zero). For the second and subsequent cycles of a wait stated external memory access, synchronous specifications t_{SACKC} and t_{HACKC} must be met for wait state modes *External*, *Either*, or *Both* (*Both*, after internal wait states have completed).

[2]The falling edge of $\overline{MS}$x, $\overline{SW}$, and $\overline{BMS}$ is referenced.

[3]See System Hold Time Calculation under Test Conditions for calculation of hold times given capacitive and dc loads.

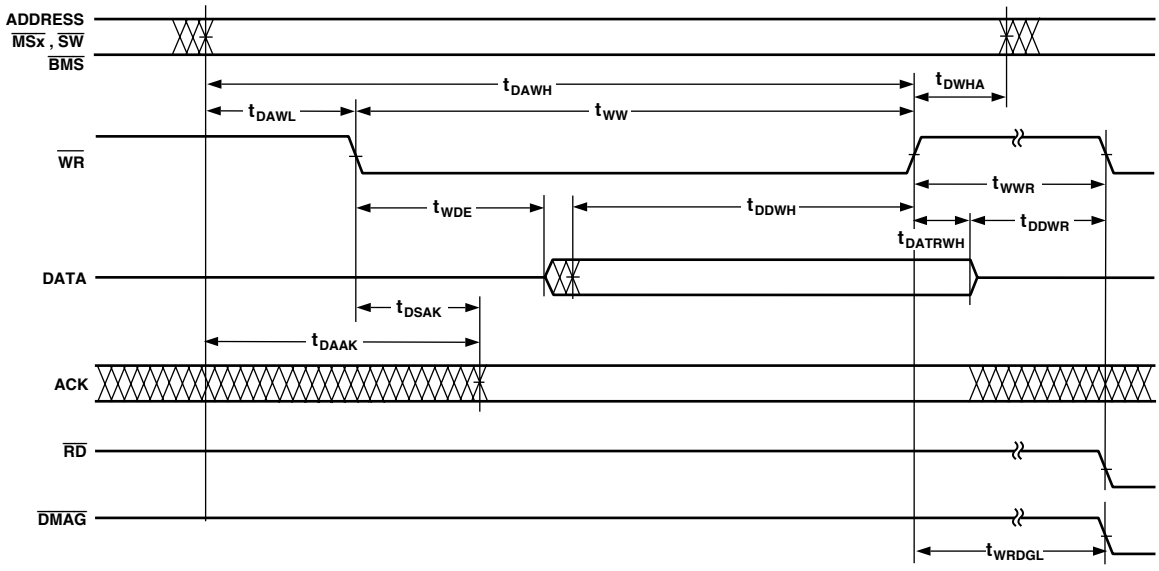


Figure 12. Memory Write—Bus Master

Synchronous Read/Write—Bus Master

Use these specifications for interfacing to external memory systems that require CLKIN-relative timing or for accessing a slave ADSP-21065L (in multiprocessor memory space). These synchronous switching characteristics are also valid during asynchronous memory reads and writes (see Memory Read—Bus Master and Memory Write—Bus Master).

When accessing a slave ADSP-21065L, these switching characteristics must meet the slave's timing requirements for synchronous read/writes (see Synchronous Read/Write—Bus Slave). The slave ADSP-21065L must also meet these (bus master) timing requirements for data and acknowledge setup and hold times.

Parameter		Min	Max	Unit
Timing Requirements:				
t_{SSDATI}	Data Setup Before CLKIN	0.25 + 2 DT		ns
t_{HSDATI}	Data Hold After CLKIN	4.0 – 2 DT		ns
t_{DAAK}	ACK Delay After Address, $\overline{MS}$x, $\overline{SW}$, $\overline{BMS}$[1, 2]		24.0 + 30 DT + W	ns
t_{SACKC}	ACK Setup Before CLKIN[1]	2.75 + 4 DT		ns
t_{HACK}	ACK Hold After CLKIN	2.0 – 4 DT		ns
Switching Characteristics:				
t_{DADRO}	Address, $\overline{MS}$x, $\overline{BMS}$, $\overline{SW}$ Delay After CLKIN[1]		7.0 – 2 DT	ns
t_{HADRO}	Address, $\overline{MS}$x, $\overline{BMS}$, $\overline{SW}$ Hold After CLKIN	0.5 – 2 DT		ns
t_{DRDO}	$\overline{RD}$ High Delay After CLKIN	0.5 – 2 DT	6.0 – 2 DT	ns
t_{DWRO}	$\overline{WR}$ High Delay After CLKIN	0.0 – 3 DT	6.0 – 3 DT	ns
t_{DRWL}	$\overline{RD}$/$\overline{WR}$ Low Delay After CLKIN	7.5 + 4 DT	11.75 + 4 DT	ns
t_{DDATO}	Data Delay After CLKIN		22.0 + 10 DT	ns
t_{DATTR}	Data Disable After CLKIN[3]	1.0 – 2 DT	7.0 – 2 DT	ns
t_{DBM}	BMSTR Delay After CLKIN		3.0	ns
t_{HBM}	BMSTR Hold After CLKIN	–4.0		ns

W = (number of wait states specified in WAIT register) × t_{CK}.

NOTES

[1]Data Hold: User must meet t_{HDA} or t_{HDRH} or synchronous specification t_{HDATI}. See system hold time calculation under test conditions for the calculation of hold times given capacitive and dc loads.

[2]ACK is not sampled on external memory accesses that use the *Internal* wait state mode. For the first CLKIN cycle of a new external memory access, ACK must be valid by t_{DAAK} or t_{DSAK} or synchronous specification t_{SACKC} for wait state modes *External*, *Either*, or *Both* (*Both*, if the internal wait state is zero). For the second and subsequent cycles of a wait stated external memory access, synchronous specifications t_{SACKC} and t_{HACKC} must be met for wait state modes *External*, *Either*, or *Both* (*Both*, after internal wait states have completed).

[3]See System Hold Time Calculation under Test Conditions for calculation of hold times given capacitive and dc loads.

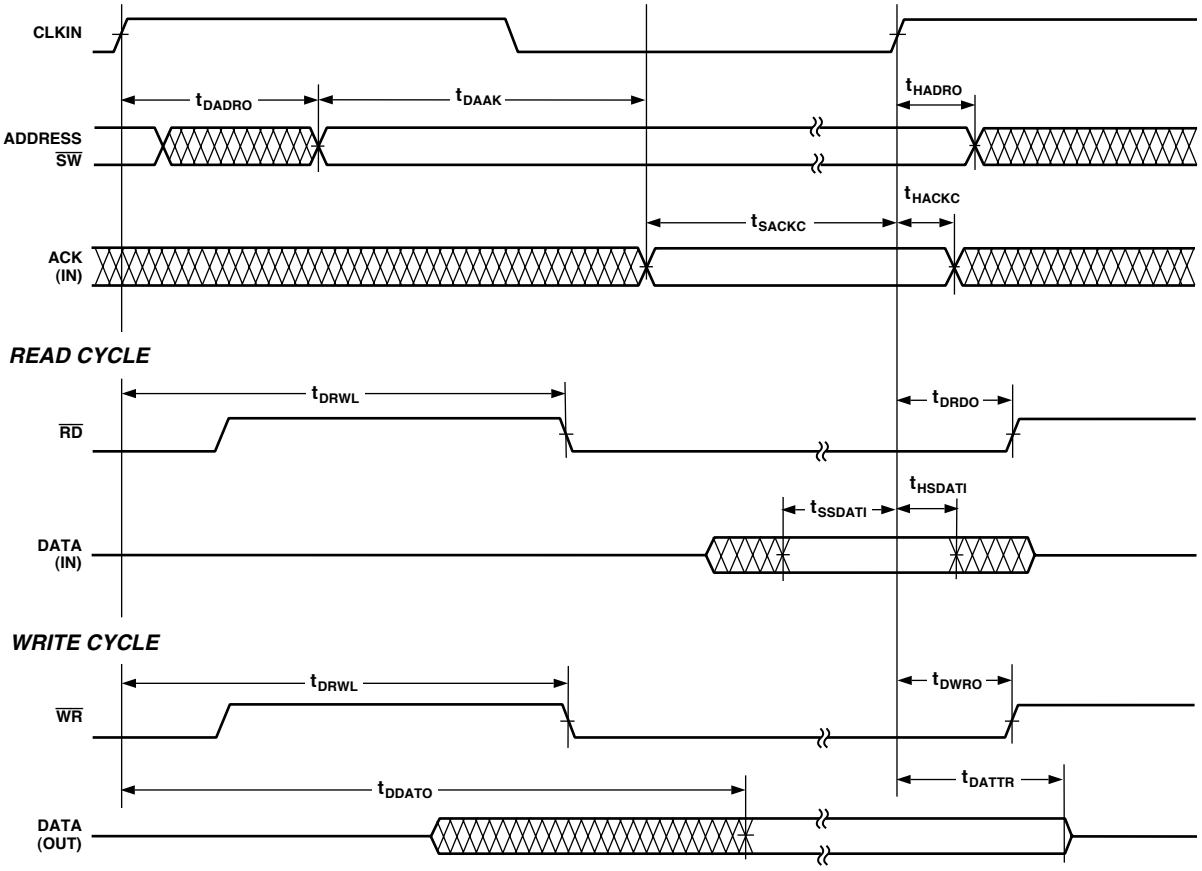


Figure 13. Synchronous Read/Write—Bus Master

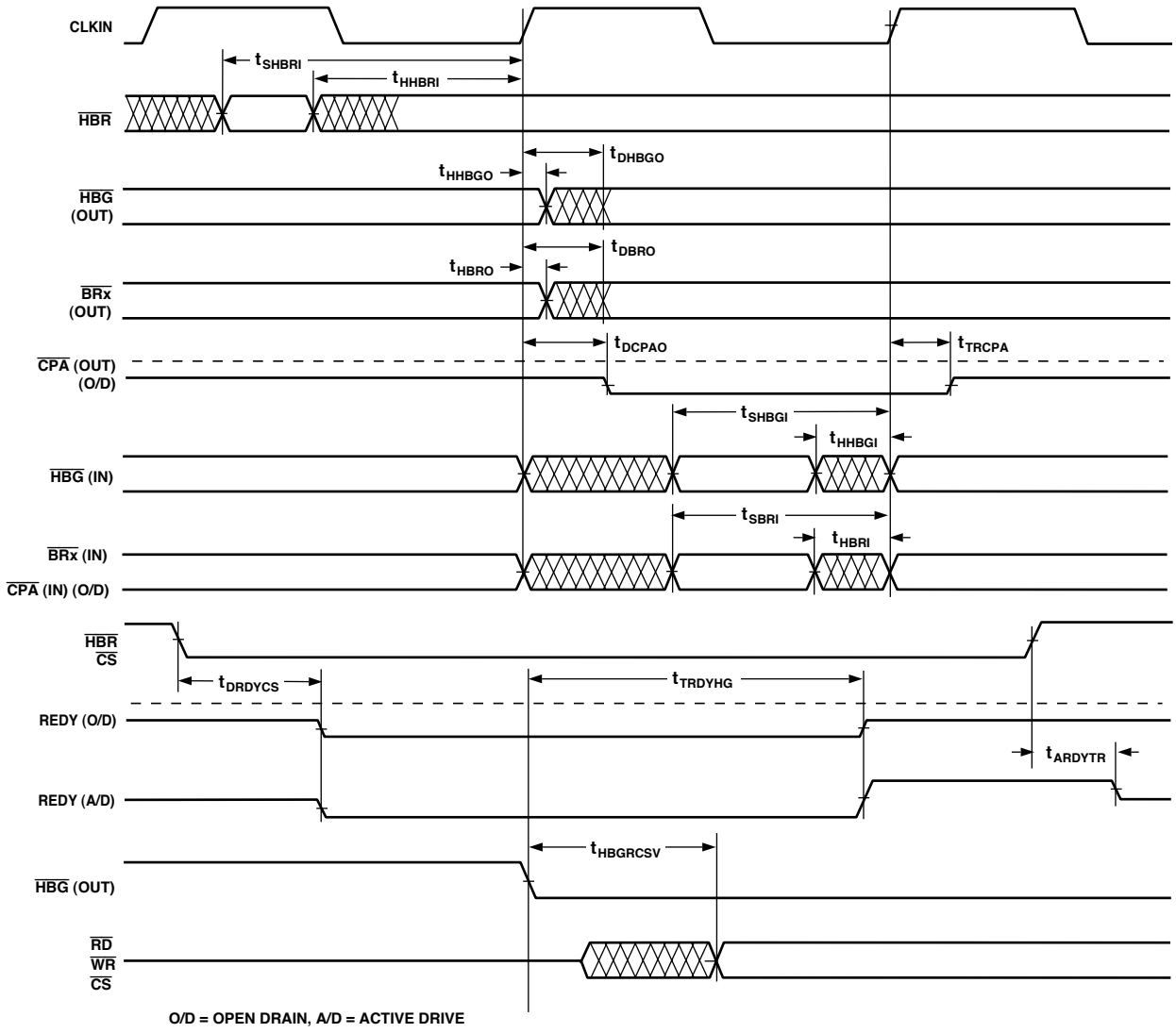


Figure 15. Multiprocessor Bus Request and Host Bus Request

Three-State Timing—Bus Master, Bus Slave, $\overline{\text{HBR}}$, $\overline{\text{SBTS}}$

These specifications show how the memory interface is disabled (stops driving) or enabled (resumes driving) relative to CLKIN and the $\overline{\text{SBTS}}$ pin. This timing is applicable to bus master transition cycles (BTC) and host transition cycles (HTC) as well as the $\overline{\text{SBTS}}$ pin.

Parameter		Min	Max	Unit
Timing Requirements:				
t_{STSCK}	$\overline{\text{SBTS}}$ Setup Before CLKIN	7.0 + 8 DT		ns
t_{HTSCK}	$\overline{\text{SBTS}}$ Hold Before CLKIN		1.0 + 8 DT	ns
Switching Characteristics:				
t_{MIENA}	Address/Select Enable After CLKIN	1.0 – 2 DT		ns
t_{MIENS}	Strobes Enable After CLKIN[1]	–0.5 – 2 DT		ns
t_{MIENHG}	$\overline{\text{HBG}}$ Enable After CLKIN	2.0 – 2 DT		ns
t_{MITRA}	Address/Select Disable After CLKIN		3.0 – 4 DT	ns
t_{MITRS}	Strobes Disable After CLKIN[1]		4.0 – 4 DT	ns
t_{MITRHG}	$\overline{\text{HBG}}$ Disable After CLKIN		5.5 – 4 DT	ns
t_{DATEN}	Data Enable After CLKIN[2]	10.0 + 5 DT		ns
t_{DATTR}	Data Disable After CLKIN[2]	1.0 – 2 DT	7.0 – 2 DT	ns
t_{ACKEN}	ACK Enable After CLKIN[2]	7.5 + 4 DT		ns
t_{ACKTR}	ACK Disable After CLKIN[2]	1.0 – 2 DT	6.0 – 2 DT	ns
t_{MTRHBG}	Memory Interface Disable Before $\overline{\text{HBG}}$ Low[3]	2.0 + 2 DT		ns
t_{MENHBG}	Memory Interface Enable After $\overline{\text{HBG}}$ High[3]	15.75 + DT		ns

NOTES

[1]Strobes = $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{SW}}$, $\overline{\text{DMAG}}$.

[2]In addition to bus master transition cycles, these specs also apply to bus master and bus slave synchronous read/write.

[3]Memory Interface = Address, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS}}$x, $\overline{\text{SW}}$, $\overline{\text{DMAG}}$x, $\overline{\text{BMS}}$ (in EPROM boot mode).

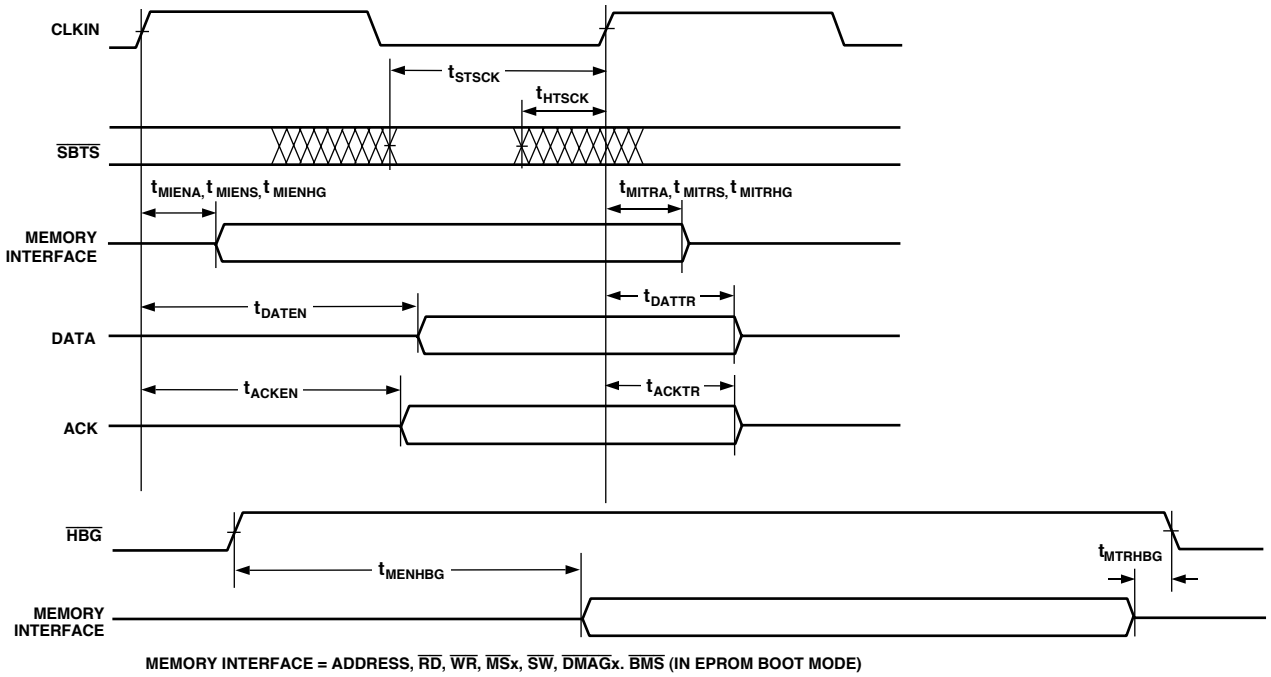


Figure 17. Three-State Timing

DMA Handshake

These specifications describe the three DMA handshake modes. In all three modes DMAR is used to initiate transfers. For handshake mode, $\overline{\text{DMAG}}$ controls the latching or enabling of data externally. For external handshake mode, the data transfer is controlled by the $\text{ADDR}_{23\text{-}0}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{SW}}$, $\overline{\text{MS}}_{3\text{-}0}$, ACK, and $\overline{\text{DMAG}}$ signals. External mode cannot be used for transfers with SDRAM. For Paced Master mode, the data transfer is controlled by $\text{ADDR}_{23\text{-}0}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS}}_{3\text{-}0}$, and ACK (not $\overline{\text{DMAG}}$). For Paced Master mode, the Memory Read-Bus Master, Memory Write-Bus Master, and Synchronous Read/Write-Bus Master timing specifications for $\text{ADDR}_{23\text{-}0}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS}}_{3\text{-}0}$, $\overline{\text{SW}}$, $\text{DATA}_{31\text{-}0}$, and ACK also apply.

Parameter		Min	Max	Unit
Timing Requirements:				
t_{SDRLC}	$\overline{\text{DMAR}}$x Low Setup Before CLKIN[1]	5.0		ns
t_{SDRHC}	$\overline{\text{DMAR}}$x High Setup Before CLKIN[1]	5.0		ns
t_{WDR}	$\overline{\text{DMAR}}$x Width Low (Nonsynchronous)	6.0		ns
$t_{SDATDGL}$	Data Setup After $\overline{\text{DMAG}}$x Low[2]		15.0 + 20 DT	ns
$t_{HDATIDG}$	Data Hold After $\overline{\text{DMAG}}$x High	0.0		ns
t_{DATDRH}	Data Valid After $\overline{\text{DMAR}}$x High[2]		25.0 + 14 DT	ns
t_{DMARLL}	$\overline{\text{DMAR}}$x Low Edge to Low Edge	18.0 + 14 DT		ns
t_{DMARH}	$\overline{\text{DMAR}}$x Width High	6.0		ns
Switching Characteristics:				
t_{DDGL}	$\overline{\text{DMAG}}$x Low Delay After CLKIN	14.0 + 10 DT	20.0 + 10 DT	ns
t_{WDGH}	$\overline{\text{DMAG}}$x High Width	10.0 + 12 DT + HI		ns
t_{WDGL}	$\overline{\text{DMAG}}$x Low Width	16.0 + 20 DT		ns
t_{HDGC}	$\overline{\text{DMAG}}$x High Delay After CLKIN	0.0 – 2 DT	6.0 – 2 DT	ns
t_{DADGH}	Address Select Valid to $\overline{\text{DMAG}}$x High	28.0 + 16 DT		ns
t_{DDGHA}	Address Select Hold After $\overline{\text{DMAG}}$x High	–1.0		ns
$t_{VDATDGH}$	Data Valid Before $\overline{\text{DMAG}}$x High[3]	16.0 + 20 DT		ns
$t_{DATRDGH}$	Data Disable After $\overline{\text{DMAG}}$x High[4]	0.0	4.0	ns
t_{DGWRL}	$\overline{\text{WR}}$ Low Before $\overline{\text{DMAG}}$x Low	5.0 + 6 DT	8.0 + 6 DT	ns
t_{DGWRH}	$\overline{\text{DMAG}}$x Low Before $\overline{\text{WR}}$ High	18.0 + 19 DT + W		ns
t_{DGWRR}	$\overline{\text{WR}}$ High Before $\overline{\text{DMAG}}$x High	0.75 + 1 DT	3.0 + 1 DT	ns
t_{DGRDL}	$\overline{\text{RD}}$ Low Before $\overline{\text{DMAG}}$x Low	5.0	8.0	ns
t_{DRDGH}	$\overline{\text{RD}}$ Low Before $\overline{\text{DMAG}}$x High	24.0 + 26 DT + W		ns
t_{DGRDR}	$\overline{\text{RD}}$ High Before $\overline{\text{DMAG}}$x High	0.0	2.0	ns
t_{DGWR}	$\overline{\text{DMAG}}$x High to $\overline{\text{WR}}$, $\overline{\text{RD}}$ Low	5.0 + 6 DT + HI		ns

W = (number of wait states specified in WAIT register) × t_{CK}.

HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).

NOTES

[1]Only required for recognition in the current cycle.

[2]$t_{SDATDGL}$ is the data setup requirement if $\overline{\text{DMAR}}$x is not being used to hold off completion of a write. Otherwise, if $\overline{\text{DMAR}}$x low holds off completion of the write, the data can be driven t_{DATDRH} after $\overline{\text{DMAR}}$x is brought high.

[3]$t_{VDATDGH}$ is valid if $\overline{\text{DMAR}}$x is not being used to hold off completion of a read. If $\overline{\text{DMAR}}$x is used to prolong the read, then $t_{VDATDGH}$ = 8 + 9 DT + (n × t_{CK}) where *n* equals the number of extra cycles that the access is prolonged.

[4]See System Hold Time Calculation under Test Conditions for calculation of hold times given capacitive and dc loads.

SDRAM Interface—Bus Master
Use these specifications for ADSP-21065L bus master accesses of SDRAM.

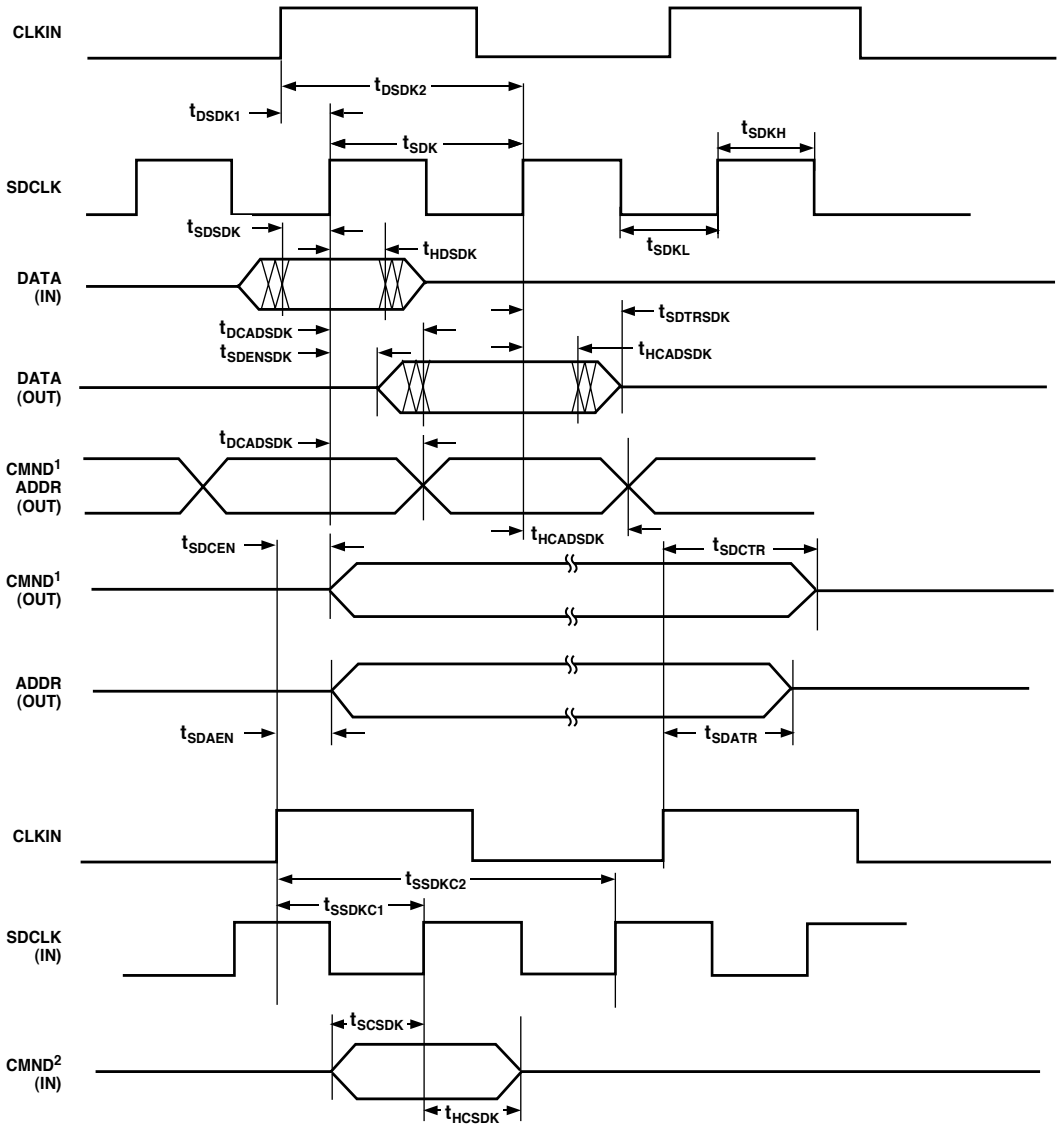
Parameter		Min	Max	Unit
Timing Requirements:				
t_{SDSDK}	Data Setup Before SDCLK	2.0		ns
t_{HDSDK}	Data Hold After SDCLK	1.25		ns
Switching Characteristics:				
t_{DSDK1}	First SDCLK Rise Delay After CLKIN	9.0 + 6 DT	12.75 + 6 DT	ns
t_{DSDK2}	Second SDCLK Rise Delay After CLKIN	25.5 + 22 DT	29.25 + 22 DT	ns
t_{SDK}	SDCLK Period	16.67	$t_{CK}/2$	ns
t_{SDKH}	SDCLK Width High	7.5 + 8 DT		ns
t_{SDKL}	SDCLK Width Low	6.5 + 8 DT		ns
$t_{DCADSDK}$	Command, Address, Data, Delay After SDCLK[1]		10.0 + 5 DT	ns
$t_{HCADSDK}$	Command, Address, Data, Hold After SDCLK[1]	4.5 + 5 DT		ns
$t_{SDTRSDK}$	Data Three-State After SDCLK		9.5 + 5 DT	ns
$t_{SDENSDK}$	Data Enable After SDCLK[2]	6.0 + 5 DT		ns
t_{SDCTR}	SDCLK, Command Three-State After CLKIN[1]	5.0 + 3 DT	9.75 + 3 DT	ns
t_{SDCEN}	SDCLK, Command Enable After CLKIN[1]	5.0 + 2 DT	10.0 + 2 DT	ns
t_{SDATR}	Address Three-State After CLKIN	–1.0 – 4 DT	3.0 – 4 DT	ns
t_{SDAEN}	Address Enable After CLKIN	1.0 – 2 DT	7.0 – 2 DT	ns

NOTES
[1]Command = SDCKE, $\overline{MS}$x, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, DQM, and SDA10.
[2]SDRAM controller adds one SDRAM CLK three-stated cycle delay ($t_{CK}/2$) on a Read followed by a Write.

SDRAM Interface—Bus Slave
These timing requirements allow a bus slave to sample the bus master's SDRAM command and detect when a refresh occurs.

Parameter		Min	Max	Unit
Timing Requirements:				
t_{SSDKC1}	First SDCLK Rise After CLKIN	6.50 + 16 DT	17.5 + 16 DT	ns
t_{SSDKC2}	Second SDCLK Rise After CLKIN	23.25	34.25	ns
t_{SCSDK}	Command Setup Before SDCLK*	0.0		ns
t_{HCSDK}	Command Hold After SDCLK*	2.0		ns

NOTE
*Command = SDCKE, $\overline{RAS}$, $\overline{CAS}$, and $\overline{SDWE}$.



NOTES
[1]COMMAND = SDCKE, $\overline{MS}_X$, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, DQM, AND SDA10.
[2]SDRAM CONTROLLER ADDS ONE SDRAM CLK THREE-STATED CYCLE DELAY ($t_{CK}/2$) ON A READ FOLLOWED BY A WRITE.

Figure 19. SDRAM Interface

Serial Ports

Parameter		Min	Max	Unit
External Clock				
Timing Requirements:				
t_{SFSE}	TFS/RFS Setup Before TCLK/RCLK[1]	4.0		ns
t_{HFSE}	TFS/RFS Hold After TCLK/RCLK[1]	4.0		ns
t_{SDRE}	Receive Data Setup Before RCLK[1]	1.5		ns
t_{HDRE}	Receive Data Hold After RCLK[1]	4.0		ns
t_{SCLKW}	TCLK/RCLK Width	9.0		ns
t_{SCLK}	TCLK/RCLK Period	t_{CK}		ns
Internal Clock				
Timing Requirements:				
t_{SFSI}	TFS Setup Before TCLK[2]; RFS Setup Before RCLK[1]	8.0		ns
t_{HFSI}	TFS/RFS Hold After TCLK/RCLK[1]	1.0		ns
t_{SDRI}	Receive Data Setup Before RCLK[1]	3.0		ns
t_{HDRI}	Receive Data Hold After RCLK[1]	3.0		ns
External or Internal Clock				
Switching Characteristics:				
t_{DFSE}	RFS Delay After RCLK (Internally Generated RFS)[2]		13.0	ns
t_{HOFSE}	RFS Hold After RCLK (Internally Generated RFS)[2]	3.0		ns
External Clock				
Switching Characteristics:				
t_{DFSE}	TFS Delay After TCLK (Internally Generated TFS)[2]		13.0	ns
t_{HOFSE}	TFS Hold After TCLK (Internally Generated TFS)[2]	3.0		ns
t_{DDTE}	Transmit Data Delay After TCLK[2]		12.5	ns
t_{HDTE}	Transmit Data Hold After TCLK[2]	4.0		ns
Internal Clock				
Switching Characteristics:				
t_{DFSI}	TFS Delay After TCLK (Internally Generated TFS)[2]		4.5	ns
t_{HOFSI}	TFS Hold After TCLK (Internally Generated TFS)[2]	–1.5		ns
t_{DDTI}	Transmit Data Delay After TCLK[2]		7.5	ns
t_{HDTI}	Transmit Data Hold After TCLK[2]	0.0		ns
t_{SCLKIW}	TCLK/RCLK Width	$(t_{SCLK}/2) - 2.5$	$(t_{SCLK}/2) + 2.5$	ns
Enable and Three-State				
Switching Characteristics:				
t_{DTENE}	Data Enable from External TCLK[2]	5.0		ns
t_{DDTTE}	Data Disable from External RCLK[2]		10.0	ns
t_{DTENI}	Data Enable from Internal TCLK[2]	0.0		ns
t_{DDTTI}	Data Disable from Internal TCLK[2]		3.0	ns
t_{DCLK}	TCLK/RCLK Delay from CLKIN		18.0 + 6 DT	ns
t_{DPTR}	SPORT Disable After CLKIN		14.0	ns
External Late Frame Sync				
$t_{DDTLFSE}$	Data Delay from Late External TFS or External RFS with MCE = 1, MFD = 0[3, 4]		10.5	ns
$t_{DTENLFSE}$	Data Enable from late FS or MCE = 1, MFD = 0[3, 4]	3.5		ns
$t_{DDTLSCK}$	Data Delay from TCLK/RCLK for Late External TFS or External RFS with MCE = 1, MFD = 0[3, 4]		12.0	ns
$t_{DTENLSCK}$	Data Enable from RCLK/TCLK for Late External FS or MCE = 1, MFD = 0[3, 4]	4.5		ns

NOTES

To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup-and-hold, 2) data delay and data setup-and-hold, and 3) SCLK width.

[1]Referenced to sample edge.

[2]Referenced to drive edge.

[3]MCE = 1, TFS enable and TFS valid follow $t_{DDTENFS}$ and $t_{DDTLFSE}$.

[4]If external RFS/TFS setup to RCLK/TCLK > $t_{SCLK}/2$ then $t_{DDTLSCK}$ and $t_{DTENLSCK}$ apply; otherwise $t_{DDTLFSE}$ and $t_{DTENLFS}$ apply.

*Word selected timing for I^2S mode is the same as TFS/RFS timing (normal framing only).

OUTPUT DRIVE CURRENT

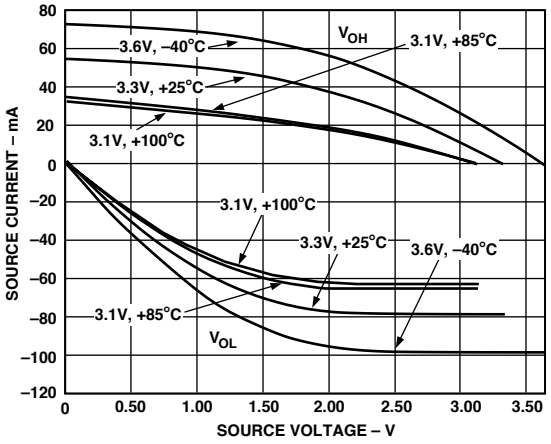


Figure 24. Typical Drive Currents

TEST CONDITIONS

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L and the load current, I_L. This decay time can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times \Delta V}{I_L}$$

The output disable time t_{DIS} is the difference between $t_{MEASURED}$ and t_{DECAY} as shown in Figure 26. The time $t_{MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.5 V.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to when they start driving. The output enable time t_{ENA} is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-21065L's output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (i.e., t_{DATRWH} for the write cycle).

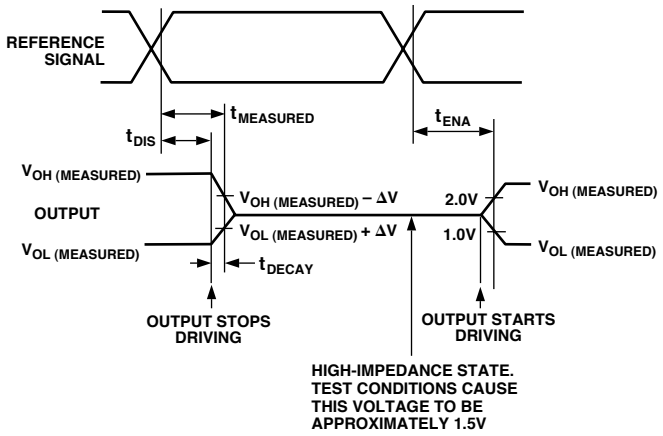


Figure 25. Output Enable

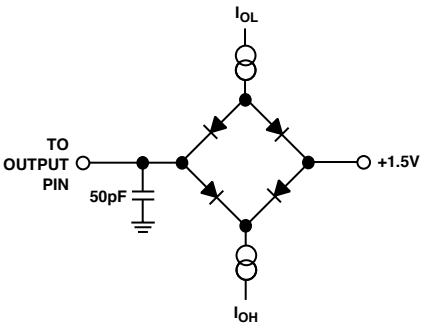


Figure 26. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

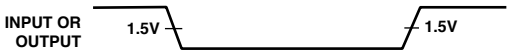


Figure 27. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 50 pF on all pins. The delay and hold specifications given should be derated by a factor of l.8 ns/50 pF for loads other than the nominal value of 50 pF. Figure 28 and Figure 29 show how output rise time varies with capacitance. Figure 30 shows graphically how output delays and hold vary with load capacitance. (Note that this graph or derating does not apply to output disable delays; see the previous section Output Disable time under Test Conditions.) The graphs of Figure 28, Figure 29, and Figure 30 may not be linear outside the ranges shown.

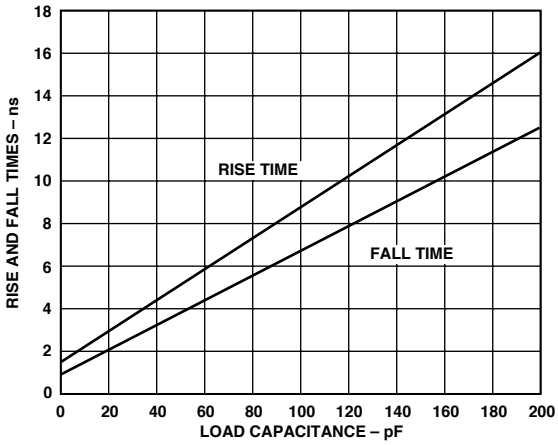


Figure 28. Typical Rise and Fall Time (10%–90% V_{DD})

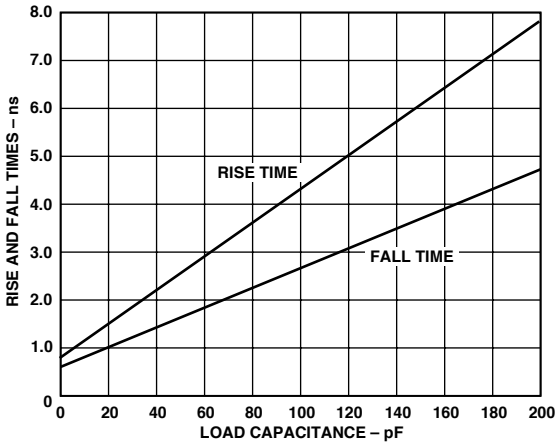


Figure 29. Typical Rise and Fall Time (0.8 V–2.0 V)

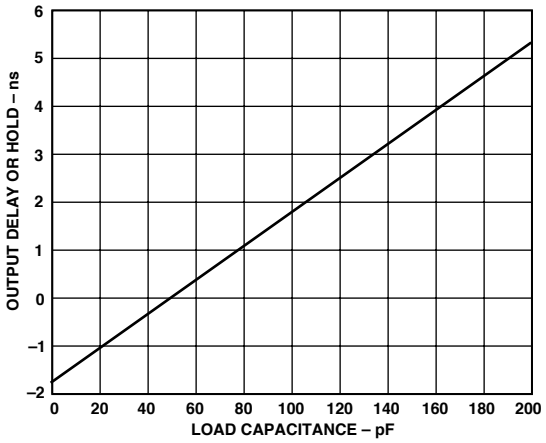


Figure 30. Typical Output Delay or Hold

208-LEAD MQFP PIN CONFIGURATION

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	VDD	43	$\overline{\text{CAS}}$	85	VDD	127	DATA28	169	ADDR17
2	RFS0	44	$\overline{\text{SDWE}}$	86	DATA3	128	DATA29	170	ADDR16
3	GND	45	VDD	87	DATA4	129	GND	171	ADDR15
4	RCLK0	46	DQM	88	DATA5	130	VDD	172	VDD
5	DR0A	47	SDCKE	89	GND	131	VDD	173	ADDR14
6	DR0B	48	SDA10	90	DATA6	132	DATA30	174	ADDR13
7	TFS0	49	GND	91	DATA7	133	DATA31	175	ADDR12
8	TCLK0	50	$\overline{\text{DMAG}}$1	92	DATA8	134	FLAG7	176	VDD
9	VDD	51	$\overline{\text{DMAG}}$2	93	VDD	135	GND	177	GND
10	GND	52	$\overline{\text{HBG}}$	94	GND	136	FLAG6	178	ADDR11
11	DT0A	53	BMSTR	95	VDD	137	FLAG5	179	ADDR10
12	DT0B	54	VDD	96	DATA9	138	FLAG4	180	ADDR9
13	RFS1	55	$\overline{\text{CS}}$	97	DATA10	139	GND	181	GND
14	GND	56	$\overline{\text{SBTS}}$	98	DATA11	140	VDD	182	VDD
15	RCLK1	57	GND	99	GND	141	VDD	183	ADDR8
16	DR1A	58	$\overline{\text{WR}}$	100	DATA12	142	NC	184	ADDR7
17	DR1B	59	$\overline{\text{RD}}$	101	DATA13	143	ID1	185	ADDR6
18	TFS1	60	GND	102	NC	144	ID0	186	GND
19	TCLK1	61	VDD	103	NC	145	$\overline{\text{EMU}}$	187	GND
20	VDD	62	GND	104	DATA14	146	TDO	188	ADDR5
21	VDD	63	REDY	105	VDD	147	$\overline{\text{TRST}}$	189	ADDR4
22	DT1A	64	$\overline{\text{SW}}$	106	GND	148	TDI	190	ADDR3
23	DT1B	65	$\overline{\text{CPA}}$	107	DATA15	149	TMS	191	VDD
24	PWM_EVENT1	66	VDD	108	DATA16	150	GND	192	VDD
25	GND	67	VDD	109	DATA17	151	TCK	193	ADDR2
26	PWM_EVENT0	68	GND	110	VDD	152	BSEL	194	ADDR1
27	$\overline{\text{BR1}}$	69	ACK	111	DATA18	153	$\overline{\text{BMS}}$	195	ADDR0
28	$\overline{\text{BR2}}$	70	$\overline{\text{MS}}$0	112	DATA19	154	GND	196	GND
29	VDD	71	$\overline{\text{MS}}$1	113	DATA20	155	GND	197	FLAG0
30	CLKIN	72	GND	114	GND	156	VDD	198	FLAG1
31	XTAL	73	GND	115	NC	157	$\overline{\text{RESET}}$	199	FLAG2
32	VDD	74	$\overline{\text{MS}}$2	116	DATA21	158	VDD	200	VDD
33	GND	75	$\overline{\text{MS}}$3	117	DATA22	159	GND	201	FLAG3
34	SDCLK1	76	FLAG11	118	DATA23	160	ADDR23	202	NC
35	GND	77	VDD	119	GND	161	ADDR22	203	NC
36	VDD	78	FLAG10	120	VDD	162	ADDR21	204	GND
37	SDCLK0	79	FLAG9	121	DATA24	163	VDD	205	$\overline{\text{IRQ}}$0
38	$\overline{\text{DMAR}}$1	80	FLAG8	122	DATA25	164	ADDR20	206	$\overline{\text{IRQ}}$1
39	$\overline{\text{DMAR}}$2	81	GND	123	DATA26	165	ADDR19	207	$\overline{\text{IRQ}}$2
40	$\overline{\text{HBR}}$	82	DATA0	124	VDD	166	ADDR18	208	NC
41	GND	83	DATA1	125	GND	167	GND		
42	$\overline{\text{RAS}}$	84	DATA2	126	DATA27	168	GND		