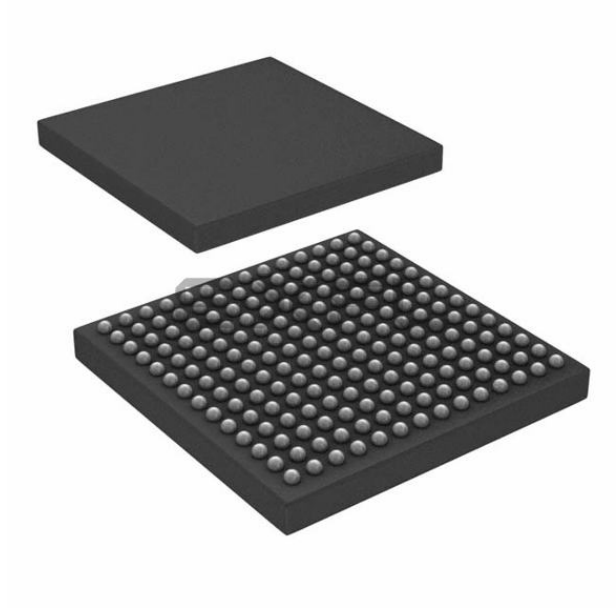


Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Floating Point
Interface	Host Interface, Serial Port
Clock Rate	60MHz
Non-Volatile Memory	External
On-Chip RAM	64kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	0°C ~ 85°C (TC)
Mounting Type	Surface Mount
Package / Case	196-BGA, CSPBGA
Supplier Device Package	196-CSPBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21065lkca-264

ADSP-21065L* PRODUCT PAGE QUICK LINKS

Last Content Update: 04/08/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

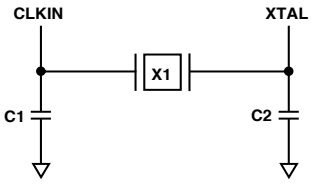
- EE-103: Performing Level Conversion Between 5v and 3.3v IC's
- EE-104: Setting Up Streams with the VisualDSP Debugger
- EE-107: ADSP-21065L EPROM Booting
- EE-109: ADSP2106x : Using 2106x SPORT's as Timers
- EE-110: A Quick Primer on ELF and DWARF File Formats
- EE-112: Class Implementation in Analog C++
- EE-116: SHARC Shortword DMA
- EE-127: The ADSP-21065L On-chip SDRAM Controller
- EE-128: DSP in C++: Calling Assembly Class Member Functions From C++
- EE-132: Placing C Code and Data Modules in SHARC memory using VisualDSP++™
- EE-141: Benchmarking C Code on the ADSP-2106x and the ADSP-2116x Family of DSPs
- EE-159: Initializing DSP System & Control Registers From C and C++
- EE-166: ADSP-2106x EPROM Overlay Support with VisualDSP++ 2.0
- EE-175: Emulator and Evaluation Hardware Troubleshooting Guide for VisualDSP++ Users
- EE-191: Implementing a Glueless UART Using The SHARC® DSP SPORTs
- EE-202: Using the Expert Linker for Multiprocessor LDFs
- EE-219: Connecting Character LCD Panels to ADSP-21262 SHARC® DSPs
- EE-244: Interfacing Gated Clocks to ADSP-21065L SHARC® Processors
- EE-247: Interfacing AD7676 ADCs to ADSP-21065L SHARC® Processors
- EE-253: Power Bypass Decoupling of SHARC® Processors
- EE-261: Understanding Jitter Requirements of PLL-Based Processors
- EE-267: Implementing In-Place FFTs on SISD and SIMD SHARC® Processors
- EE-273: Using the VisualDSP++ Command-Line Installer
- EE-280: In-Circuit Flash Programming on ADSP-2106x SHARC® Processors
- EE-285: Migrating from ADSP-21065L to ADSP-21375 SHARC® Processors

Pin	Type	Function
$\overline{HBR}$	I/A	**Host Bus Request.** Must be asserted by a host processor to request control of the ADSP-21065L's external bus. When $\overline{HBR}$ is asserted in a multiprocessing system, the ADSP-21065L that is bus master will relinquish the bus and assert $\overline{HBG}$. To relinquish the bus, the ADSP-21065L places the address, data, select, and strobe lines in a high impedance state. It does, however, continue to drive the SDRAM control pins. $\overline{HBR}$ has priority over all ADSP-21065L bus requests ($\overline{BR}_{2-1}$) in a multiprocessor system.
$\overline{HBG}$	I/O	**Host Bus Grant**. Acknowledges an $\overline{HBR}$ bus request, indicating that the host processor may take control of the external bus. $\overline{HBG}$ is asserted by the ADSP-21065L until $\overline{HBR}$ is released. In a multiprocessor system, $\overline{HBG}$ is output by the ADSP-21065L bus master.
$\overline{CS}$	I/A	**Chip Select.** Asserted by host processor to select the ADSP-21065L.
REDY (O/D)	O	**Host Bus Acknowledge.** The ADSP-21065L deasserts REDY to add wait states to an asynchronous access of its internal memory or IOP registers by a host. Open drain output (O/D) by default; can be programmed in ADREDY bit of SYSCON register to be active drive (A/D). REDY will only be output if the $\overline{CS}$ and $\overline{HBR}$ inputs are asserted.
$\overline{DMAR}_1$	I/A	**DMA Request 1** (DMA Channel 9).
$\overline{DMAR}_2$	I/A	**DMA Request 2** (DMA Channel 8).
$\overline{DMAG}_1$	O/T	**DMA Grant 1** (DMA Channel 9).
$\overline{DMAG}_2$	O/T	**DMA Grant 2** (DMA Channel 8).
$\overline{BR}_{2-1}$	I/O/S	**Multiprocessing Bus Requests.** Used by multiprocessing ADSP-21065Ls to arbitrate for bus mastership. An ADSP-21065L drives its own $\overline{BR}$x line (corresponding to the value of its ID_{2-0} inputs) only and monitors all others. In a uniprocessor system, tie both $\overline{BR}$x pins to VDD.
ID_{1-0}	I	**Multiprocessing ID.** Determines which multiprocessor bus request ($\overline{BR}_1$–$\overline{BR}_2$) is used by ADSP-21065L. ID = 01 corresponds to $\overline{BR}_1$, ID = 10 corresponds to $\overline{BR}_2$. ID = 00 in single-processor systems. These lines are a system configuration selection which should be hard-wired or changed only at reset.
$\overline{CPA}$ (O/D)	I/O	**Core Priority Access.** Asserting its $\overline{CPA}$ pin allows the core processor of an ADSP-21065L bus slave to interrupt background DMA transfers and gain access to the external bus. $\overline{CPA}$ is an open drain output that is connected to both ADSP-21065Ls in the system. The $\overline{CPA}$ pin has an internal 5 kΩ pull-up resistor. If core access priority is not required in a system, leave the $\overline{CPA}$ pin unconnected.
DTxX	O	**Data Transmit** (Serial Ports 0, 1; Channels A, B). Each DTxX pin has a 50 kΩ internal pull-up resistor.
DRxX	I	**Data Receive** (Serial Ports 0, 1; Channels A, B). Each DRxX pin has a 50 kΩ internal pull-up resistor.
TCLKx	I/O	**Transmit Clock** (Serial Ports 0, 1). Each TCLK pin has a 50 kΩ internal pull-up resistor.
RCLKx	I/O	**Receive Clock** (Serial Ports 0, 1). Each RCLK pin has a 50 kΩ internal pull-up resistor.
TFSx	I/O	**Transmit Frame Sync** (Serial Ports 0, 1).
RFSx	I/O	**Receive Frame Sync** (Serial Ports 0, 1).
BSEL	I	**EPROM Boot Select.** When BSEL is high, the ADSP-21065L is configured for booting from an 8-bit EPROM. When BSEL is low, the BSEL and $\overline{BMS}$ inputs determine booting mode. See $\overline{BMS}$ for details. This signal is a system configuration selection which should be hardwired.

Pin	Type	Function
SDA10	O/T	**SDRAM A10 Pin.** Enables applications to refresh an SDRAM in parallel with a host access.
$\overline{\text{XTAL}}$	O	**Crystal Oscillator Terminal.** Used in conjunction with CLKIN to enable the ADSP-21065L's internal clock generator or to disable it to use an external clock source. See CLKIN.
$\overline{\text{PWM\_EVENT}}_{1-0}$	I/O/A	**PWM Output/Event Capture.** In PWMOUT mode, is an output pin and functions as a timer counter. In WIDTH_CNT mode, is an input pin and functions as a pulse counter/event capture.
VDD	P	**Power Supply;** nominally +3.3 V dc. (33 pins)
GND	G	**Power Supply Return**. (37 pins)
NC		**Do Not Connect.** Reserved pins that must be left open and unconnected. (7 pins)

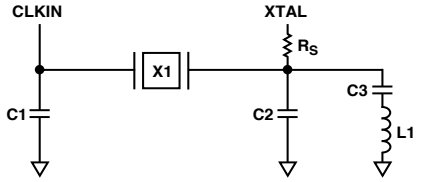
CLOCK SIGNALS

The ADSP-21065L can use an external clock or a crystal. See CLKIN pin description. You can configure the ADSP-21065L to use its internal clock generator by connecting the necessary components to CLKIN and XTAL. You can use either a crystal operating in the fundamental mode or a crystal operating at an overtone. Figure 4 shows the component connections used for a crystal operating in fundamental mode, and Figure 5 shows the component connections used for a crystal operating at an overtone.



SUGGESTED COMPONENTS FOR 30 MHz OPERATION:
ECLIPTEK EC2SM-33-30.000M (SURFACE MOUNT PACKAGE)
ECLIPTEK EC-33-30.000M (THROUGH-HOLE PACKAGE)
C1 = 33pF
C2 = 27pF
NOTE: C1 AND C2 ARE SPECIFIC TO CRYSTAL SPECIFIED FOR X1.
CONTACT CRYSTAL MANUFACTURER FOR DETAILS.

Figure 4. 30 MHz Operation (Fundamental Mode Crystal)



SUGGESTED COMPONENTS FOR 30MHz OPERATION:
ECLIPTEK EC2SM-T-30.000M (SURFACE MOUNT PACKAGE)
ECLIPTEK ECT-30.000M (THROUGH-HOLE PACKAGE)
C1 = 18pF
C2 = 27pF
C3 = 75pF
L_1 = 3300nH
R_S = SEE NOTE.
NOTE: C1, C2, C3, R_S AND L_1 ARE SPECIFIC TO CRYSTAL SPECIFIED FOR X1. CONTACT MANUFACTURER FOR DETAILS.

Figure 5. 30 MHz Operation (3rd Overtone Crystal)

TARGET BOARD CONNECTOR FOR EZ-ICE PROBE

The ADSP-2106x EZ-ICE emulator uses the IEEE 1149.1 JTAG test access port of the ADSP-2106x to monitor and control the target board processor during emulation. The EZ-ICE probe requires the ADSP-2106x's CLKIN, TMS, TCK, $\overline{\text{TRST}}$, TDI, TDO, $\overline{\text{EMU}}$ and GND signals be made accessible on the target system via a 14-pin connector (a 2 row x 7 pin strip header) such as that shown in Figure 6. The EZ-ICE probe plugs directly onto this connector for chip-on-board emulation. You must add this connector to your target board design if you, intend to use the ADSP-2106x EZ-ICE.

The total trace length between the EZ-ICE connector and the furthest device sharing the EZ-ICE JTAG pins should be limited to 15 inches maximum for guaranteed operation. This restriction on length must include EZ-ICE JTAG signals, which are routed to one or more 2106x devices or to a combination of 2106xs and other JTAG devices on the chain.

The 14-pin, 2-row pin strip header is keyed at the Pin 3 location—you must remove Pin 3 from the header. The pins must be 0.025 inch square and at least 0.20 inch in length. Pin spacing should be 0.1 × 0.1 inches. Pin strip headers are available from vendors such as 3M, McKenzie and Samtec.

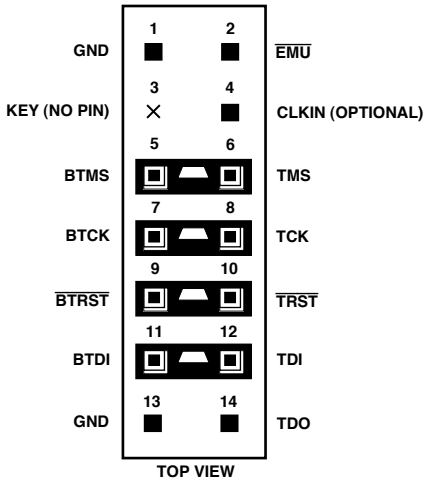


Figure 6. Target Board Connector for ADSP-2106x EZ-ICE (JTAG Header)

ADSP-21065L–SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter		Test Conditions	C Grade Min	C Grade Max	K Grade Min	K Grade Max	Unit
V_{DD}	Supply Voltage		3.13	3.60	3.13	3.60	V
T_{CASE}	Case Operating Temperature		–40	+100	0	+85	°C
V_{IH}	High Level Input Voltage	@ V_{DD} = max	2.0	V_{DD} + 0.5	2.0	V_{DD} + 0.5	V
V_{IL1}	Low Level Input Voltage[1]	@ V_{DD} = min	–0.5	0.8	–0.5	0.8	V
V_{IL2}	Low Level Input Voltage[2]	@ V_{DD} = min	–0.5	0.7	–0.5	0.7	V

NOTE
See Environmental Conditions for information on thermal specifications.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	C and K Grades Min	C and K Grades Max	Unit
V_{OH}	High Level Output Voltage[3]	@ V_{DD} = min, I_{OH} = –2.0 mA[4]	2.4		V
V_{OL}	Low Level Output Voltage[3]	@ V_{DD} = min, I_{OL} = 4.0 mA[4]		0.4	V
I_{IH}	High Level Input Current[5]	@ V_{DD} = max, V_{IN} = V_{DD} max		10	µA
I_{IL}	Low Level Input Current[5]	@ V_{DD} = max, V_{IN} = 0 V		10	µA
I_{ILP}	Low Level Input Current[6]	@ V_{DD} = max, V_{IN} = 0 V		150	µA
I_{OZH}	Three-State Leakage Current[7, 8, 9, 10]	@ V_{DD} = max, V_{IN} = V_{DD} max		10	µA
I_{OZL}	Three-State Leakage Current[7]	@ V_{DD} = max, V_{IN} = 0 V		8	µA
I_{OZLS}	Three-State Leakage Current[8]	@ V_{DD} = max, V_{IN} = 0 V		150	µA
I_{OZLA}	Three-State Leakage Current[11]	@ V_{DD} = max, V_{IN} = 1.5 V		350	µA
I_{OZLAR}	Three-State Leakage Current[10]	@ V_{DD} = max, V_{IN} = 0 V		4	mA
I_{OZLC}	Three-State Leakage Current[9]	@ V_{DD} = max, V_{IN} = 0 V		1.5	mA
C_{IN}	Input Capacitance[12, 13]	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		8	pF

NOTES
[1] Applies to input and bidirectional pins: $DATA_{31-0}$, $ADDR_{23-0}$, BSEL, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $\overline{SBTS}$, $\overline{IRQ}_{2-0}$, $FLAG_{11-0}$, $\overline{HBG}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR}_{2-1}$, $\overline{ID}_{2-0}$, RPBA, $\overline{CPA}$, TFS0, TFS1, RFS0, RFS1, $\overline{BMS}$, TMS, TDI, TCK, $\overline{HBR}$, DR0A, DR1A, DR0B, DR1B, TCLK0, TCLK1, RCLK0, RCLK1, $\overline{RESET}$, $\overline{TRST}$, PWM_EVENT0, PWM_EVENT1, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, $\overline{SDCKE}$.
[2] Applies to input pin CLKIN.
[3] Applies to output and bidirectional pins: $DATA_{31-0}$, $ADDR_{23-0}$, MS_{3-0}, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $FLAG_{11-0}$, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR}_{2-1}$, $\overline{CPA}$, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, DT0A, DT1A, DT0B, DT1B, XTAL, $\overline{BMS}$, TDO, $\overline{EMU}$, BMSTR, PWM_EVENT0, PWM_EVENT1, $\overline{RAS}$, $\overline{CAS}$, DQM, $\overline{SDWE}$, SDCLK0, SDCLK1, $\overline{SDCKE}$, SDA10.
[4] See Output Drive Currents for typical drive current capabilities.
[5] Applies to input pins: ACK, $\overline{SBTS}$, $\overline{IRQ}_{2-0}$, $\overline{HBR}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, ID_{1-0}, BSEL, CLKIN, $\overline{RESET}$, TCK (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID_{1-0} = 01 and another ADSP-21065L is not requesting bus mastership.)
[6] Applies to input pins with internal pull-ups: DR0A, DR1A, DR0B, DR1B, $\overline{TRST}$, TMS, TDI.
[7] Applies to three-statable pins: $DATA_{31-0}$, $ADDR_{23-0}$, $\overline{MS}_{3-0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $FLAG_{11-0}$, REDY, $\overline{HBG}$, $\overline{DMAG}_1$, $\overline{DMAG}_2$, $\overline{BMS}$, TDO, $\overline{RAS}$, $\overline{CAS}$, DQM, $\overline{SDWE}$, SDCLK0, SDCLK1, $\overline{SDCKE}$, SDA10, and $\overline{EMU}$ (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID_{1-0} = 01 and another ADSP-21065L is not requesting bus mastership).
[8] Applies to three-statable pins with internal pull-ups: DT0A, DT1A, DT0B, DT1B, TCLK0, TCLK1, RCLK0, RCLK1.
[9] Applies to $\overline{CPA}$ pin.
[10] Applies to ACK pin when pulled up.
[11] Applies to ACK pin when keeper latch enabled.
[12] Guaranteed but not tested.
[13] Applies to all signal pins.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . –0.3 V to +4.6 V
Input Voltage . . . . . –0.5 V to V_{DD} + 0.5 V
Output Voltage Swing . . . . . –0.5 V to V_{DD} + 0.5 V
Load Capacitance . . . . . 200 pF
Junction Temperature Under Bias . . . . . 130°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (5 seconds) . . . . . 280°C

*Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADSP-21065L features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Switching Characteristics specify how the processor changes its signals. You have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell you what the processor will do in a given circumstance. You can also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing Requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

(O/D) = Open Drain
(A/D) = Active Drive

Parameter		66 MHz Min	66 MHz Max	60 MHz Min	60 MHz Max	Unit
Clock Input						
Timing Requirements:						
t_{CK}	CLKIN Period	30.00	100	33.33	100	ns
t_{CKL}	CLKIN Width Low	7.0		7.0		ns
t_{CKH}	CLKIN Width High	5.0		5.0		ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V–2.0 V)		3.0		3.0	ns

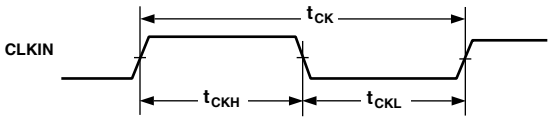


Figure 7. Clock Input

Parameter		Min	Max	Unit
Reset				
Timing Requirements:				
t_{WRST}	$\overline{\text{RESET}}$ Pulsewidth Low[1]	2 t_{CK}		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN High[2]	23.5 + 24 DT	t_{CK}	ns

NOTES
[1]Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 3000 CLKIN cycles while $\overline{\text{RESET}}$ is low, assuming stable V_{DD} and CLKIN (not including start-up time of external clock oscillator).
[2]Only required if multiple ADSP-2106xs must come out of reset synchronous to CLKIN with program counters (PC) equal (i.e., for a SIMD system). Not required for multiple ADSP-2106xs communicating over the shared bus (through the external port), because the bus arbitration logic synchronizes itself automatically after reset.

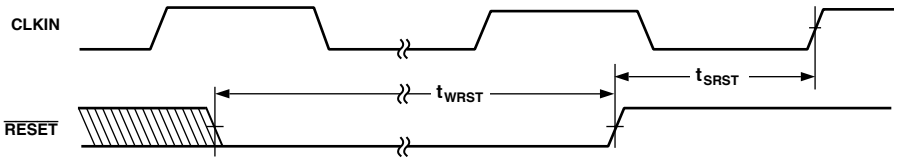


Figure 8. Reset

Parameter		Min	Max	Unit
Interrupts				
Timing Requirements:				
t_{SIR}	$\overline{\text{IRQ}}$2-0 Setup Before CLKIN High or Low[1]	11.0 + 12 DT		ns
t_{HIR}	$\overline{\text{IRQ}}$2-0 Hold Before CLKIN High or Low[1]		0.0 + 12 DT	ns
t_{IPW}	$\overline{\text{IRQ}}$2-0 Pulsewidth[2]	2.0 + t_{CK}/2		ns

NOTES
[1]Only required for $\overline{\text{IRQ}}$x recognition in the following cycle.
[2]Applies only if t_{SIR} and t_{HIR} requirements are not met.

Memory Read—Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the ADSP-21065L is the bus master when accessing external memory space. These switching characteristics also apply for bus master synchronous read/write timing (see Synchronous Read/Write—Bus Master below). If these timing requirements are met, the synchronous read/write timing can be ignored (and vice versa). An exception to this is the ACK pin timing requirements as described in the note below.

Parameter		Min	Max	Unit
Timing Requirements:				
t_{DAD}	Address, Selects Delay to Data Valid[1, 2]		28.0 + 32 DT + W	ns
t_{DRLD}	$\overline{RD}$ Low to Data Valid[1]		24.0 + 26 DT + W	ns
t_{HDA}	Data Hold from Address Selects[3]	0.0		ns
t_{HDRH}	Data Hold from $\overline{RD}$ High[3]	0.0		ns
t_{DAAK}	ACK Delay from Address, Selects[2, 3]		24.0 + 30 DT + W	ns
t_{DSAK}	ACK Delay from $\overline{RD}$ Low[3]		19.5 + 24 DT + W	ns
Switching Characteristics:				
t_{DRHA}	Address, Selects Hold After $\overline{RD}$ High	–1.0 + H		ns
t_{DARL}	Address, Selects to $\overline{RD}$ Low[2]	3.0 + 6 DT		ns
t_{RW}	$\overline{RD}$ Pulsewidth	25.0 + 26 DT + W		ns
t_{RWR}	$\overline{RD}$ High to $\overline{WR}$, $\overline{RD}$ Low	4.5 + 6 DT + HI		ns
t_{RDGL}	$\overline{RD}$ High to $\overline{DMAG}$x Low	11.0 +12 DT + HI		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).
H = t_{CK} (if an address hold cycle occurs as specified in WAIT register; otherwise H = 0).

NOTES
[1]Data Delay/Setup: User must meet t_{DAD} or to t_{DRLD} or synchronous specification t_{SSDATI}.
[2]The falling edge of $\overline{MS}$x, $\overline{SW}$, $\overline{BMS}$, are referenced.
[3]ACK is not sampled on external memory accesses that use the *Internal* wait state mode. For the first CLKIN cycle of a new external memory access, ACK must be valid by t_{DAAK} or t_{DSAK} or synchronous specification t_{SACKC} for wait state modes *External*, *Either*, or *Both* (*Both*, if the internal wait state is zero). For the second and subsequent cycles of a wait stated external memory access, synchronous specifications t_{SACKC} and t_{HACKC} must be met for wait state modes *External*, *Either*, or *Both* (*Both*, after internal wait states have completed).

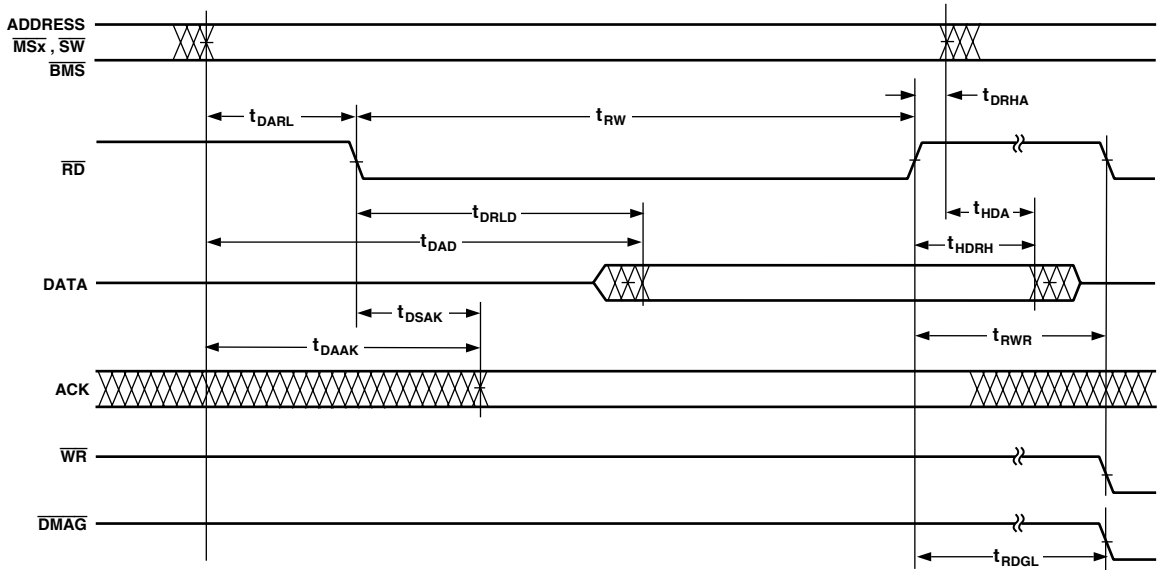


Figure 11. Memory Read—Bus Master

Memory Write—Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the ADSP-21065L is the bus master when accessing external memory space. These switching characteristics also apply for bus master synchronous read/write timing (see Synchronous Read/Write—Bus Master below). If these timing requirements are met, the synchronous read/write timing can be ignored (and vice versa). An exception to this is the ACK pin timing requirements as described in the note below.

Parameter		Min	Max	Unit
Timing Requirements:				
t_{DAAK}	ACK Delay from Address[1, 2]		24.0 + 30 DT + W	ns
t_{DSAK}	ACK Delay from $\overline{WR}$ Low[1]		19.5 + 24 DT + W	ns
Switching Characteristics:				
t_{DAWH}	Address, Selects to $\overline{WR}$ Deasserted[2]	29.0 + 31 DT + W		ns
t_{DAWL}	Address, Selects to $\overline{WR}$ Low[2]	3.5 + 6 DT		ns
t_{WW}	$\overline{WR}$ Pulsewidth	24.5 + 25 DT + W		ns
t_{DDWH}	Data Setup Before $\overline{WR}$ High	15.5 + 19 DT + W		ns
t_{DWHA}	Address Hold After $\overline{WR}$ Deasserted	0.0 + 1 DT + H		ns
t_{DATRWH}	Data Disable After $\overline{WR}$ Deasserted[3]	1.0 + 1 DT + H	4.0 + 1 DT + H	ns
t_{WWR}	$\overline{WR}$ High to $\overline{WR}$, $\overline{RD}$ Low	4.5 + 7 DT + H		ns
t_{WRDGL}	$\overline{WR}$ High to $\overline{DMAG}$x Low	11.0 + 13 DT + H		ns
t_{DDWR}	Data Disable Before $\overline{WR}$ or $\overline{RD}$ Low	3.5 + 6 DT + I		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	4.5 + 6 DT		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
H = t_{CK} (if an address hold cycle occurs, as specified in WAIT register; otherwise H = 0).
I = t_{CK} (if a bus idle cycle occurs, as specified in WAIT register; otherwise I = 0).

NOTES

[1]ACK is not sampled on external memory accesses that use the *Internal* wait state mode. For the first CLKIN cycle of a new external memory access, ACK must be valid by t_{DAAK} or t_{DSAK} or synchronous specification t_{SACKC} for wait state modes *External*, *Either*, or *Both* (*Both*, if the internal wait state is zero). For the second and subsequent cycles of a wait stated external memory access, synchronous specifications t_{SACKC} and t_{HACKC} must be met for wait state modes *External*, *Either*, or *Both* (*Both*, after internal wait states have completed).

[2]The falling edge of $\overline{MS}$x, $\overline{SW}$, and $\overline{BMS}$ is referenced.

[3]See System Hold Time Calculation under Test Conditions for calculation of hold times given capacitive and dc loads.

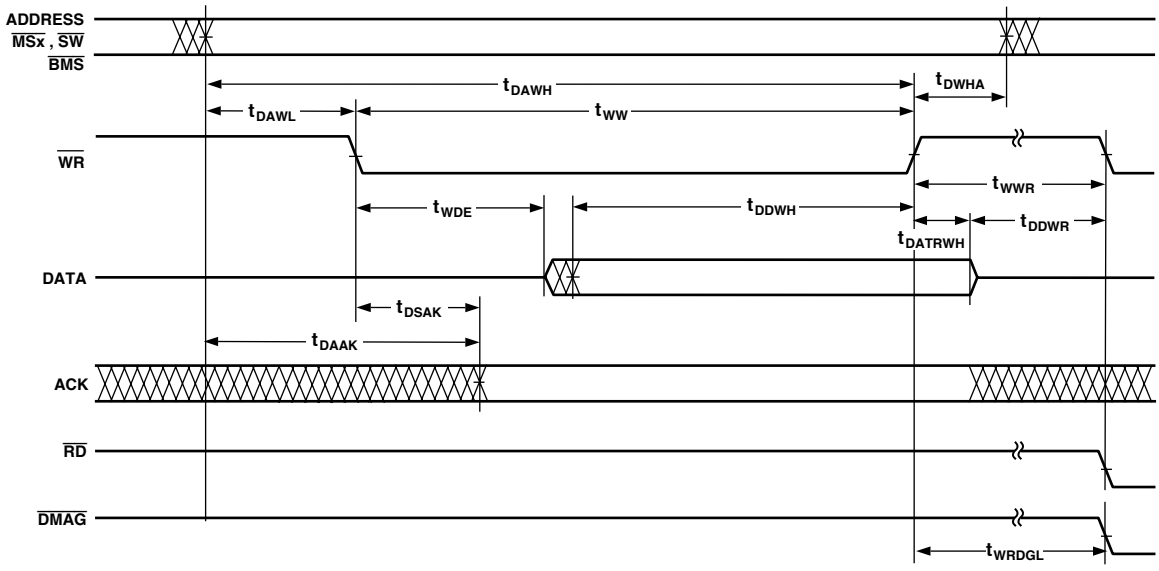


Figure 12. Memory Write—Bus Master

Synchronous Read/Write—Bus Master

Use these specifications for interfacing to external memory systems that require CLKIN-relative timing or for accessing a slave ADSP-21065L (in multiprocessor memory space). These synchronous switching characteristics are also valid during asynchronous memory reads and writes (see Memory Read—Bus Master and Memory Write—Bus Master).

When accessing a slave ADSP-21065L, these switching characteristics must meet the slave's timing requirements for synchronous read/writes (see Synchronous Read/Write—Bus Slave). The slave ADSP-21065L must also meet these (bus master) timing requirements for data and acknowledge setup and hold times.

Parameter		Min	Max	Unit
Timing Requirements:				
t_{SSDATI}	Data Setup Before CLKIN	0.25 + 2 DT		ns
t_{HSDATI}	Data Hold After CLKIN	4.0 – 2 DT		ns
t_{DAAK}	ACK Delay After Address, $\overline{MS}$x, $\overline{SW}$, $\overline{BMS}$[1, 2]		24.0 + 30 DT + W	ns
t_{SACKC}	ACK Setup Before CLKIN[1]	2.75 + 4 DT		ns
t_{HACK}	ACK Hold After CLKIN	2.0 – 4 DT		ns
Switching Characteristics:				
t_{DADRO}	Address, $\overline{MS}$x, $\overline{BMS}$, $\overline{SW}$ Delay After CLKIN[1]		7.0 – 2 DT	ns
t_{HADRO}	Address, $\overline{MS}$x, $\overline{BMS}$, $\overline{SW}$ Hold After CLKIN	0.5 – 2 DT		ns
t_{DRDO}	$\overline{RD}$ High Delay After CLKIN	0.5 – 2 DT	6.0 – 2 DT	ns
t_{DWRO}	$\overline{WR}$ High Delay After CLKIN	0.0 – 3 DT	6.0 – 3 DT	ns
t_{DRWL}	$\overline{RD}$/$\overline{WR}$ Low Delay After CLKIN	7.5 + 4 DT	11.75 + 4 DT	ns
t_{DDATO}	Data Delay After CLKIN		22.0 + 10 DT	ns
t_{DATTR}	Data Disable After CLKIN[3]	1.0 – 2 DT	7.0 – 2 DT	ns
t_{DBM}	BMSTR Delay After CLKIN		3.0	ns
t_{HBM}	BMSTR Hold After CLKIN	–4.0		ns

W = (number of wait states specified in WAIT register) × t_{CK}.

NOTES

[1]Data Hold: User must meet t_{HDA} or t_{HDRH} or synchronous specification t_{HDATI}. See system hold time calculation under test conditions for the calculation of hold times given capacitive and dc loads.

[2]ACK is not sampled on external memory accesses that use the *Internal* wait state mode. For the first CLKIN cycle of a new external memory access, ACK must be valid by t_{DAAK} or t_{DSAK} or synchronous specification t_{SACKC} for wait state modes *External*, *Either*, or *Both* (*Both*, if the internal wait state is zero). For the second and subsequent cycles of a wait stated external memory access, synchronous specifications t_{SACKC} and t_{HACKC} must be met for wait state modes *External*, *Either*, or *Both* (*Both*, after internal wait states have completed).

[3]See System Hold Time Calculation under Test Conditions for calculation of hold times given capacitive and dc loads.

Synchronous Read/Write—Bus Slave

Use these specifications for ADSP-21065L bus master accesses of a slave's IOP registers or internal memory (in multiprocessor memory space). The bus master must meet these (bus slave) timing requirements.

Parameter		Min	Max	Unit
Timing Requirements:				
t_{SADRI}	Address, $\overline{SW}$ Setup Before CLKIN	24.5 + 25 DT		ns
t_{HADRI}	Address, $\overline{SW}$ Hold Before CLKIN		4.0 + 8 DT	ns
t_{SRWLI}	$\overline{RD}/\overline{WR}$ Low Setup Before CLKIN[1]	21.0 + 21 DT		ns
t_{HRWLI}	$\overline{RD}/\overline{WR}$ Low Hold After CLKIN	–2.50 – 5 DT	7.5 + 7 DT	ns
t_{RWHPI}	$\overline{RD}/\overline{WR}$ Pulse High	2.5		ns
t_{SDATWH}	Data Setup Before $\overline{WR}$ High	4.5		ns
t_{HDATWH}	Data Hold After $\overline{WR}$ High	0.0		ns
Switching Characteristics:				
t_{SDDATO}	Data Delay After CLKIN		31.75 + 21 DT	ns
t_{DATTR}	Data Disable After CLKIN[2]	1.0 – 2 DT	7.0 – 2 DT	ns
t_{DACK}	ACK Delay After CLKIN		29.5 + 20 DT	ns
t_{ACKTR}	ACK Disable After CLKIN[2]	1.0 – 2 DT	6.0 – 2 DT	ns

NOTES

[1]t_{SRWLI} is specified when Multiprocessor Memory Space Wait State (MMSWS bit in WAIT register) is disabled; when MMSWS is enabled, t_{SRWLI} (min) = 17.5 + 18 DT.

[2]See System Hold Time Calculation under Test Conditions for calculation of hold times given capacitive and dc loads.

For two ADSP-21065Ls to communicate synchronously as master and slave, certain master and slave specification combinations must be satisfied. Do not compare specification values directly to calculate master/slave clock skew margins for those specifications listed below. The following table shows the appropriate clock skew margin.

Table IV. Bus Master to Slave Skew Margins

Master Specification	Slave Specification	Skew Margin	
t_{SSDATI}	t_{SDDATO}	t_{CK} = 33.3 ns	+ 2.25 ns
		t_{CK} = 30.0 ns	+ 1.50 ns
t_{SACKC}	t_{DACK}	t_{CK} = 33.3 ns	+ 3.00 ns
		t_{CK} = 30.0 ns	+ 2.25 ns
t_{DADRO}	t_{SADRI}	t_{CK} = 33.3 ns	N/A
		t_{CK} = 30.0 ns	+ 2.75 ns
t_{DRWL} (Max)	t_{SRWLI}	t_{CK} = 33.3 ns	+ 1.50 ns
		t_{CK} = 30.0 ns	+ 1.25 ns
t_{DRDO} (Max)	t_{HRWLI} (Max)	t_{CK} = 33.3 ns	N/A
		t_{CK} = 30.0 ns	3.00 ns
t_{DWRO} (Max)	t_{HRWLI} (Max)	t_{CK} = 33.3 ns	N/A
		t_{CK} = 30.0 ns	3.75 ns

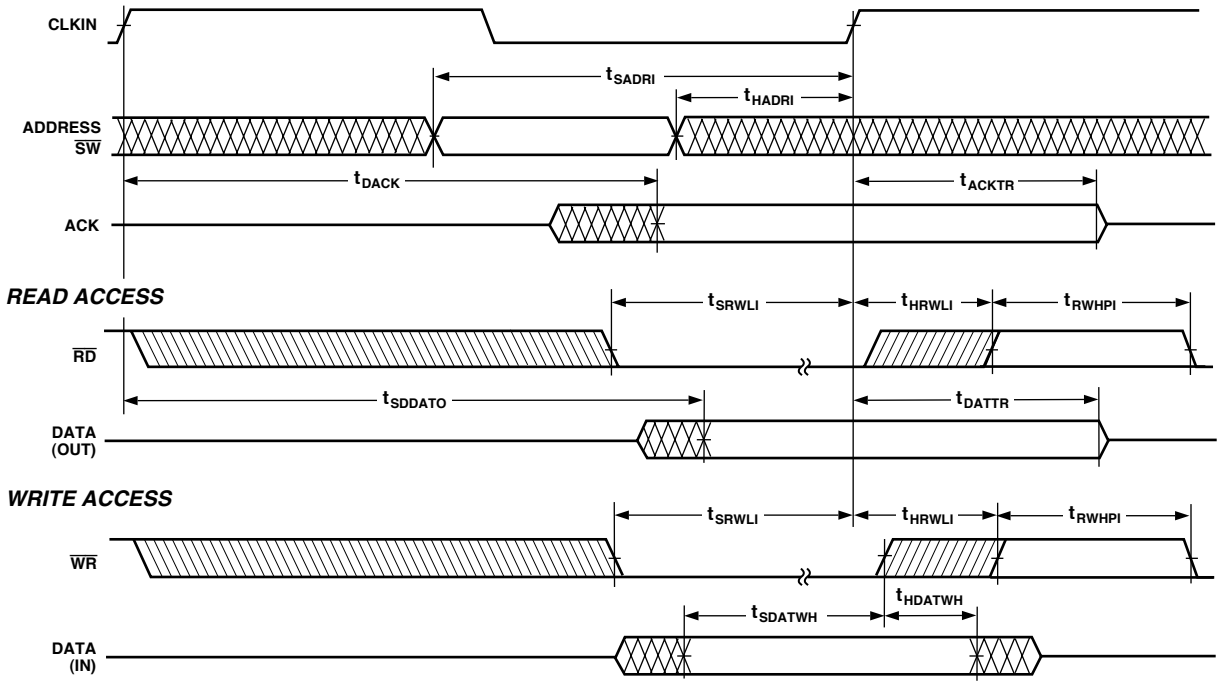


Figure 14. Synchronous Read/Write—Bus Slave

Asynchronous Read/Write—Host to ADSP-21065L

Use these specifications for asynchronous host processor accesses of an ADSP-21065L, after the host has asserted $\overline{CS}$ and $\overline{HBR}$ (low). After the ADSP-21065L returns $\overline{HBG}$, the host can drive the $\overline{RD}$ and $\overline{WR}$ pins to access the ADSP-21065L's IOP registers. $\overline{HBR}$ and $\overline{HBG}$ are assumed low for this timing. Writes can occur at a minimum interval of (1/2) t_{CK}.

Parameter		Min	Max	Unit
Read Cycle				
Timing Requirements:				
t_{SADRDL}	Address Setup/$\overline{CS}$ Low Before $\overline{RD}$ Low*	0.0		ns
t_{HADRDH}	Address Hold/$\overline{CS}$ Hold Low After $\overline{RD}$ High	0.0		ns
t_{WRWH}	$\overline{RD}$/$\overline{WR}$ High Width	6.0		ns
$t_{DRDHRDY}$	$\overline{RD}$ High Delay After REDY (O/D) Disable	0.0		ns
$t_{DRDHRDY}$	$\overline{RD}$ High Delay After REDY (A/D) Disable	0.0		ns
Switching Characteristics:				
$t_{SDATRDY}$	Data Valid Before REDY Disable from Low	1.5		ns
$t_{DRDYRDL}$	REDY (O/D) or (A/D) Low Delay After $\overline{RD}$ Low		13.5	ns
t_{RDYPRD}	REDY (O/D) or (A/D) Low Pulsewidth for Read	28.0 + DT		ns
t_{HDARWH}	Data Disable After $\overline{RD}$ High	2.0	10.0	ns
Write Cycle				
Timing Requirements:				
t_{SCSWRL}	$\overline{CS}$ Low Setup Before $\overline{WR}$ Low	0.0		ns
t_{HCSWRH}	$\overline{CS}$ Low Hold After $\overline{WR}$ High	0.0		ns
t_{SADWRH}	Address Setup Before $\overline{WR}$ High	5.0		ns
t_{HADWRH}	Address Hold After $\overline{WR}$ High	2.0		ns
t_{WWRL}	$\overline{WR}$ Low Width	7.0		ns
t_{WRWH}	$\overline{RD}$/$\overline{WR}$ High Width	6.0		ns
$t_{DWRHRDY}$	$\overline{WR}$ High Delay After REDY (O/D) or (A/D) Disable	0.0		ns
t_{SDATWH}	Data Setup Before $\overline{WR}$ High	5.0		ns
t_{HDATWH}	Data Hold After $\overline{WR}$ High	1.0		ns
Switching Characteristics:				
$t_{DRDYWRL}$	REDY (O/D) or (A/D) Low Delay After $\overline{WR}$/$\overline{CS}$ Low		13.5	ns
t_{RDYPWR}	REDY (O/D) or (A/D) Low Pulsewidth for Write	7.75		ns

NOTE

*Not required if $\overline{RD}$ and address are valid $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. For first access after $\overline{HBR}$ asserted, ADDR23-0 must be a nonMMS value 1/2 t_{CLK} before $\overline{RD}$ or $\overline{WR}$ goes low or by $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. This is easily accomplished by driving an upper address signal high when $\overline{HBG}$ is asserted. See Host Interface, in the *ADSP-21065L SHARC User's Manual*, Second Edition.

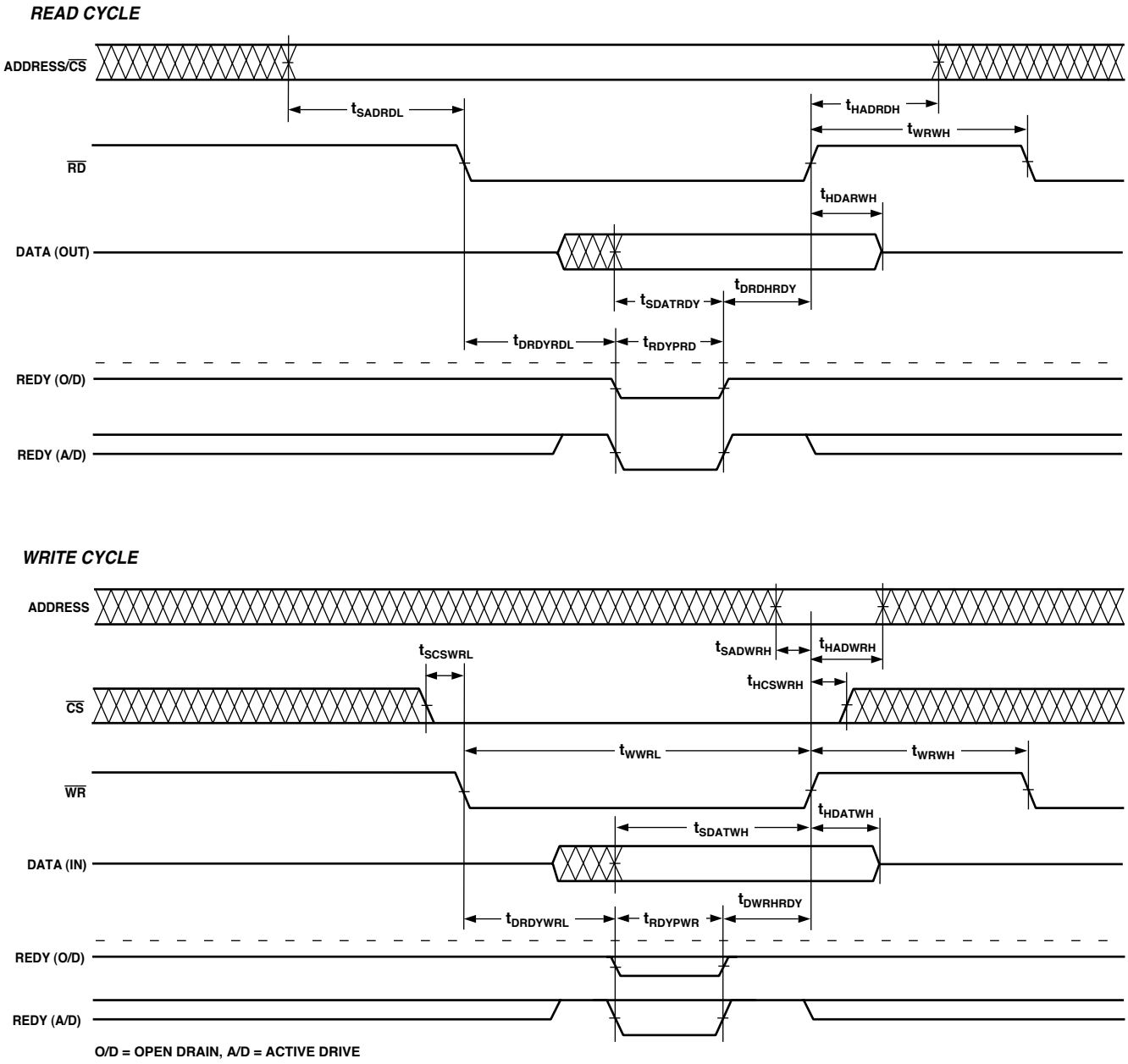


Figure 16. Asynchronous Read/Write—Host to ADSP-21065L

Three-State Timing—Bus Master, Bus Slave, $\overline{\text{HBR}}$, $\overline{\text{SBTS}}$

These specifications show how the memory interface is disabled (stops driving) or enabled (resumes driving) relative to CLKIN and the $\overline{\text{SBTS}}$ pin. This timing is applicable to bus master transition cycles (BTC) and host transition cycles (HTC) as well as the $\overline{\text{SBTS}}$ pin.

Parameter		Min	Max	Unit
Timing Requirements:				
t_{STSCK}	$\overline{\text{SBTS}}$ Setup Before CLKIN	7.0 + 8 DT		ns
t_{HTSCK}	$\overline{\text{SBTS}}$ Hold Before CLKIN		1.0 + 8 DT	ns
Switching Characteristics:				
t_{MIENA}	Address/Select Enable After CLKIN	1.0 – 2 DT		ns
t_{MIENS}	Strobes Enable After CLKIN[1]	–0.5 – 2 DT		ns
t_{MIENHG}	$\overline{\text{HBG}}$ Enable After CLKIN	2.0 – 2 DT		ns
t_{MITRA}	Address/Select Disable After CLKIN		3.0 – 4 DT	ns
t_{MITRS}	Strobes Disable After CLKIN[1]		4.0 – 4 DT	ns
t_{MITRHG}	$\overline{\text{HBG}}$ Disable After CLKIN		5.5 – 4 DT	ns
t_{DATEN}	Data Enable After CLKIN[2]	10.0 + 5 DT		ns
t_{DATTR}	Data Disable After CLKIN[2]	1.0 – 2 DT	7.0 – 2 DT	ns
t_{ACKEN}	ACK Enable After CLKIN[2]	7.5 + 4 DT		ns
t_{ACKTR}	ACK Disable After CLKIN[2]	1.0 – 2 DT	6.0 – 2 DT	ns
t_{MTRHBG}	Memory Interface Disable Before $\overline{\text{HBG}}$ Low[3]	2.0 + 2 DT		ns
t_{MENHBG}	Memory Interface Enable After $\overline{\text{HBG}}$ High[3]	15.75 + DT		ns

NOTES

[1]Strobes = $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{SW}}$, $\overline{\text{DMAG}}$.

[2]In addition to bus master transition cycles, these specs also apply to bus master and bus slave synchronous read/write.

[3]Memory Interface = Address, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS}}$x, $\overline{\text{SW}}$, $\overline{\text{DMAG}}$x, $\overline{\text{BMS}}$ (in EPROM boot mode).

DMA Handshake

These specifications describe the three DMA handshake modes. In all three modes DMAR is used to initiate transfers. For handshake mode, $\overline{\text{DMAG}}$ controls the latching or enabling of data externally. For external handshake mode, the data transfer is controlled by the $\text{ADDR}_{23\text{-}0}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{SW}}$, $\overline{\text{MS}}_{3\text{-}0}$, ACK, and $\overline{\text{DMAG}}$ signals. External mode cannot be used for transfers with SDRAM. For Paced Master mode, the data transfer is controlled by $\text{ADDR}_{23\text{-}0}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS}}_{3\text{-}0}$, and ACK (not $\overline{\text{DMAG}}$). For Paced Master mode, the Memory Read-Bus Master, Memory Write-Bus Master, and Synchronous Read/Write-Bus Master timing specifications for $\text{ADDR}_{23\text{-}0}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS}}_{3\text{-}0}$, $\overline{\text{SW}}$, $\text{DATA}_{31\text{-}0}$, and ACK also apply.

Parameter		Min	Max	Unit
Timing Requirements:				
t_{SDRLC}	$\overline{\text{DMAR}}$x Low Setup Before CLKIN[1]	5.0		ns
t_{SDRHC}	$\overline{\text{DMAR}}$x High Setup Before CLKIN[1]	5.0		ns
t_{WDR}	$\overline{\text{DMAR}}$x Width Low (Nonsynchronous)	6.0		ns
$t_{SDATDGL}$	Data Setup After $\overline{\text{DMAG}}$x Low[2]		15.0 + 20 DT	ns
$t_{HDATIDG}$	Data Hold After $\overline{\text{DMAG}}$x High	0.0		ns
t_{DATDRH}	Data Valid After $\overline{\text{DMAR}}$x High[2]		25.0 + 14 DT	ns
t_{DMARLL}	$\overline{\text{DMAR}}$x Low Edge to Low Edge	18.0 + 14 DT		ns
t_{DMARH}	$\overline{\text{DMAR}}$x Width High	6.0		ns
Switching Characteristics:				
t_{DDGL}	$\overline{\text{DMAG}}$x Low Delay After CLKIN	14.0 + 10 DT	20.0 + 10 DT	ns
t_{WDGH}	$\overline{\text{DMAG}}$x High Width	10.0 + 12 DT + HI		ns
t_{WDGL}	$\overline{\text{DMAG}}$x Low Width	16.0 + 20 DT		ns
t_{HDGC}	$\overline{\text{DMAG}}$x High Delay After CLKIN	0.0 – 2 DT	6.0 – 2 DT	ns
t_{DADGH}	Address Select Valid to $\overline{\text{DMAG}}$x High	28.0 + 16 DT		ns
t_{DDGHA}	Address Select Hold After $\overline{\text{DMAG}}$x High	–1.0		ns
$t_{VDATDGH}$	Data Valid Before $\overline{\text{DMAG}}$x High[3]	16.0 + 20 DT		ns
$t_{DATRDGH}$	Data Disable After $\overline{\text{DMAG}}$x High[4]	0.0	4.0	ns
t_{DGWRL}	$\overline{\text{WR}}$ Low Before $\overline{\text{DMAG}}$x Low	5.0 + 6 DT	8.0 + 6 DT	ns
t_{DGWRH}	$\overline{\text{DMAG}}$x Low Before $\overline{\text{WR}}$ High	18.0 + 19 DT + W		ns
t_{DGWRR}	$\overline{\text{WR}}$ High Before $\overline{\text{DMAG}}$x High	0.75 + 1 DT	3.0 + 1 DT	ns
t_{DGRDL}	$\overline{\text{RD}}$ Low Before $\overline{\text{DMAG}}$x Low	5.0	8.0	ns
t_{DRDGH}	$\overline{\text{RD}}$ Low Before $\overline{\text{DMAG}}$x High	24.0 + 26 DT + W		ns
t_{DGRDR}	$\overline{\text{RD}}$ High Before $\overline{\text{DMAG}}$x High	0.0	2.0	ns
t_{DGWR}	$\overline{\text{DMAG}}$x High to $\overline{\text{WR}}$, $\overline{\text{RD}}$ Low	5.0 + 6 DT + HI		ns

W = (number of wait states specified in WAIT register) × t_{CK}.

HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).

NOTES

[1]Only required for recognition in the current cycle.

[2]$t_{SDATDGL}$ is the data setup requirement if $\overline{\text{DMAR}}$x is not being used to hold off completion of a write. Otherwise, if $\overline{\text{DMAR}}$x low holds off completion of the write, the data can be driven t_{DATDRH} after $\overline{\text{DMAR}}$x is brought high.

[3]$t_{VDATDGH}$ is valid if $\overline{\text{DMAR}}$x is not being used to hold off completion of a read. If $\overline{\text{DMAR}}$x is used to prolong the read, then $t_{VDATDGH}$ = 8 + 9 DT + (n × t_{CK}) where *n* equals the number of extra cycles that the access is prolonged.

[4]See System Hold Time Calculation under Test Conditions for calculation of hold times given capacitive and dc loads.

SDRAM Interface—Bus Master
Use these specifications for ADSP-21065L bus master accesses of SDRAM.

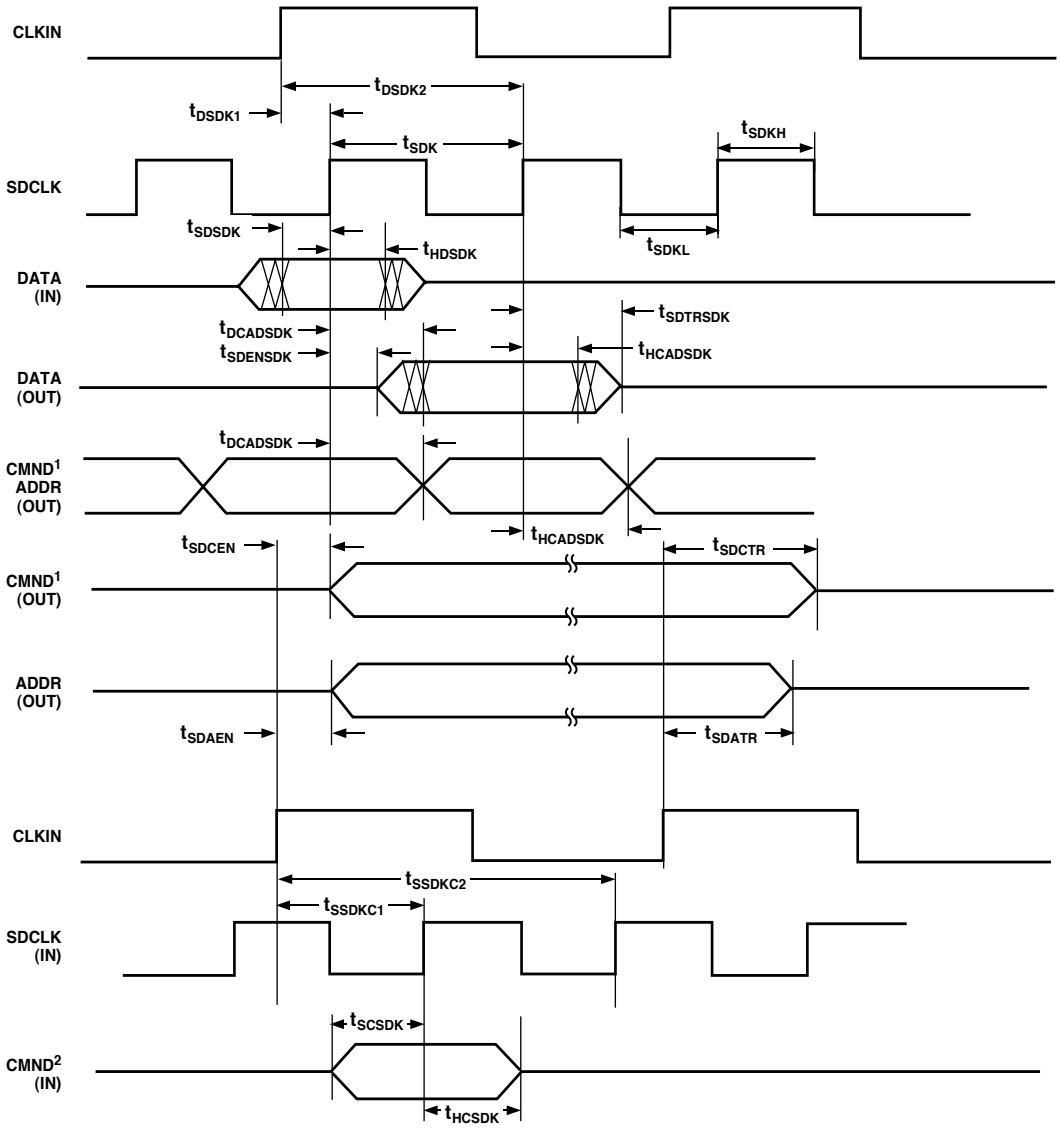
Parameter		Min	Max	Unit
Timing Requirements:				
t_{SDSDK}	Data Setup Before SDCLK	2.0		ns
t_{HDSDK}	Data Hold After SDCLK	1.25		ns
Switching Characteristics:				
t_{DSDK1}	First SDCLK Rise Delay After CLKIN	9.0 + 6 DT	12.75 + 6 DT	ns
t_{DSDK2}	Second SDCLK Rise Delay After CLKIN	25.5 + 22 DT	29.25 + 22 DT	ns
t_{SDK}	SDCLK Period	16.67	$t_{CK}/2$	ns
t_{SDKH}	SDCLK Width High	7.5 + 8 DT		ns
t_{SDKL}	SDCLK Width Low	6.5 + 8 DT		ns
$t_{DCADSDK}$	Command, Address, Data, Delay After SDCLK[1]		10.0 + 5 DT	ns
$t_{HCADSDK}$	Command, Address, Data, Hold After SDCLK[1]	4.5 + 5 DT		ns
$t_{SDTRSDK}$	Data Three-State After SDCLK		9.5 + 5 DT	ns
$t_{SDENSDK}$	Data Enable After SDCLK[2]	6.0 + 5 DT		ns
t_{SDCTR}	SDCLK, Command Three-State After CLKIN[1]	5.0 + 3 DT	9.75 + 3 DT	ns
t_{SDCEN}	SDCLK, Command Enable After CLKIN[1]	5.0 + 2 DT	10.0 + 2 DT	ns
t_{SDATR}	Address Three-State After CLKIN	–1.0 – 4 DT	3.0 – 4 DT	ns
t_{SDAEN}	Address Enable After CLKIN	1.0 – 2 DT	7.0 – 2 DT	ns

NOTES
[1]Command = SDCKE, $\overline{MS}$x, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, DQM, and SDA10.
[2]SDRAM controller adds one SDRAM CLK three-stated cycle delay ($t_{CK}/2$) on a Read followed by a Write.

SDRAM Interface—Bus Slave
These timing requirements allow a bus slave to sample the bus master's SDRAM command and detect when a refresh occurs.

Parameter		Min	Max	Unit
Timing Requirements:				
t_{SSDKC1}	First SDCLK Rise After CLKIN	6.50 + 16 DT	17.5 + 16 DT	ns
t_{SSDKC2}	Second SDCLK Rise After CLKIN	23.25	34.25	ns
t_{SCSDK}	Command Setup Before SDCLK*	0.0		ns
t_{HCSDK}	Command Hold After SDCLK*	2.0		ns

NOTE
*Command = SDCKE, $\overline{RAS}$, $\overline{CAS}$, and $\overline{SDWE}$.



NOTES
[1]COMMAND = SDCKE, $\overline{MS}_X$, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, DQM, AND SDA10.
[2]SDRAM CONTROLLER ADDS ONE SDRAM CLK THREE-STATED CYCLE DELAY ($t_{CK}/2$) ON A READ FOLLOWED BY A WRITE.

Figure 19. SDRAM Interface

OUTPUT DRIVE CURRENT

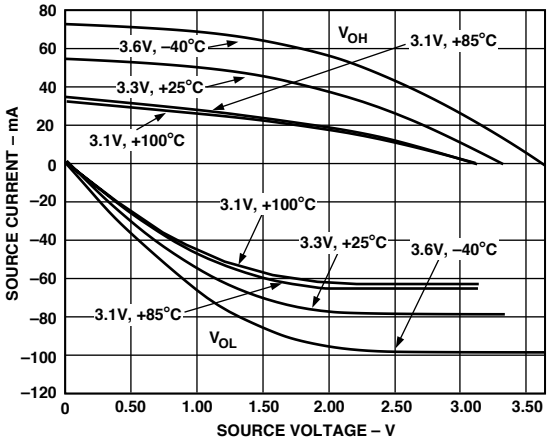


Figure 24. Typical Drive Currents

TEST CONDITIONS

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L and the load current, I_L. This decay time can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times \Delta V}{I_L}$$

The output disable time t_{DIS} is the difference between $t_{MEASURED}$ and t_{DECAY} as shown in Figure 26. The time $t_{MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.5 V.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to when they start driving. The output enable time t_{ENA} is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-21065L's output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (i.e., t_{DATRWH} for the write cycle).

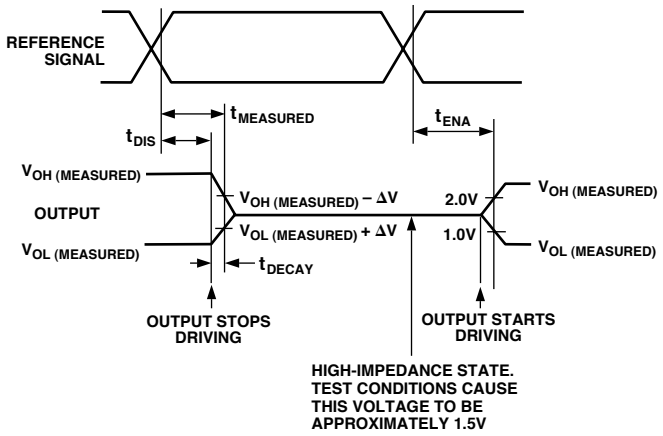


Figure 25. Output Enable

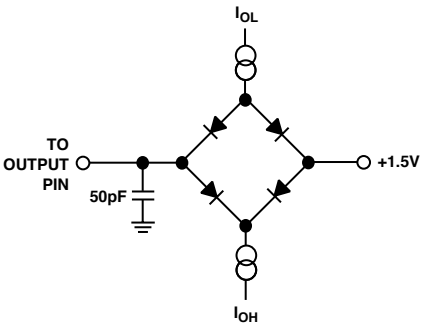


Figure 26. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

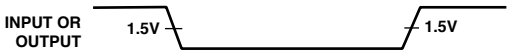


Figure 27. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

208-LEAD MQFP PIN CONFIGURATION

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	VDD	43	$\overline{\text{CAS}}$	85	VDD	127	DATA28	169	ADDR17
2	RFS0	44	$\overline{\text{SDWE}}$	86	DATA3	128	DATA29	170	ADDR16
3	GND	45	VDD	87	DATA4	129	GND	171	ADDR15
4	RCLK0	46	DQM	88	DATA5	130	VDD	172	VDD
5	DR0A	47	SDCKE	89	GND	131	VDD	173	ADDR14
6	DR0B	48	SDA10	90	DATA6	132	DATA30	174	ADDR13
7	TFS0	49	GND	91	DATA7	133	DATA31	175	ADDR12
8	TCLK0	50	$\overline{\text{DMAG}}$1	92	DATA8	134	FLAG7	176	VDD
9	VDD	51	$\overline{\text{DMAG}}$2	93	VDD	135	GND	177	GND
10	GND	52	$\overline{\text{HBG}}$	94	GND	136	FLAG6	178	ADDR11
11	DT0A	53	BMSTR	95	VDD	137	FLAG5	179	ADDR10
12	DT0B	54	VDD	96	DATA9	138	FLAG4	180	ADDR9
13	RFS1	55	$\overline{\text{CS}}$	97	DATA10	139	GND	181	GND
14	GND	56	$\overline{\text{SBTS}}$	98	DATA11	140	VDD	182	VDD
15	RCLK1	57	GND	99	GND	141	VDD	183	ADDR8
16	DR1A	58	$\overline{\text{WR}}$	100	DATA12	142	NC	184	ADDR7
17	DR1B	59	$\overline{\text{RD}}$	101	DATA13	143	ID1	185	ADDR6
18	TFS1	60	GND	102	NC	144	ID0	186	GND
19	TCLK1	61	VDD	103	NC	145	$\overline{\text{EMU}}$	187	GND
20	VDD	62	GND	104	DATA14	146	TDO	188	ADDR5
21	VDD	63	REDY	105	VDD	147	$\overline{\text{TRST}}$	189	ADDR4
22	DT1A	64	$\overline{\text{SW}}$	106	GND	148	TDI	190	ADDR3
23	DT1B	65	$\overline{\text{CPA}}$	107	DATA15	149	TMS	191	VDD
24	PWM_EVENT1	66	VDD	108	DATA16	150	GND	192	VDD
25	GND	67	VDD	109	DATA17	151	TCK	193	ADDR2
26	PWM_EVENT0	68	GND	110	VDD	152	BSEL	194	ADDR1
27	$\overline{\text{BR1}}$	69	ACK	111	DATA18	153	$\overline{\text{BMS}}$	195	ADDR0
28	$\overline{\text{BR2}}$	70	$\overline{\text{MS}}$0	112	DATA19	154	GND	196	GND
29	VDD	71	$\overline{\text{MS}}$1	113	DATA20	155	GND	197	FLAG0
30	CLKIN	72	GND	114	GND	156	VDD	198	FLAG1
31	XTAL	73	GND	115	NC	157	$\overline{\text{RESET}}$	199	FLAG2
32	VDD	74	$\overline{\text{MS}}$2	116	DATA21	158	VDD	200	VDD
33	GND	75	$\overline{\text{MS}}$3	117	DATA22	159	GND	201	FLAG3
34	SDCLK1	76	FLAG11	118	DATA23	160	ADDR23	202	NC
35	GND	77	VDD	119	GND	161	ADDR22	203	NC
36	VDD	78	FLAG10	120	VDD	162	ADDR21	204	GND
37	SDCLK0	79	FLAG9	121	DATA24	163	VDD	205	$\overline{\text{IRQ}}$0
38	$\overline{\text{DMAR}}$1	80	FLAG8	122	DATA25	164	ADDR20	206	$\overline{\text{IRQ}}$1
39	$\overline{\text{DMAR}}$2	81	GND	123	DATA26	165	ADDR19	207	$\overline{\text{IRQ}}$2
40	$\overline{\text{HBR}}$	82	DATA0	124	VDD	166	ADDR18	208	NC
41	GND	83	DATA1	125	GND	167	GND		
42	$\overline{\text{RAS}}$	84	DATA2	126	DATA27	168	GND		

196-BALL MINI-BGA PIN CONFIGURATION

Ball #	Name	Ball #	Name	Ball #	Name	Ball #	Name	Ball #	Name
A1	NC1	B1	DR0A	C1	TCLK0	D1	RCLK1	E1	TFS1
A2	NC2	B2	RFS0	C2	RCLK0	D2	TFS0	E2	DT0B
A3	FLAG2	B3	IRQ0	C3	IRQ2	D3	DR0B	E3	DT0A
A4	ADDR0	B4	FLAG0	C4	FLAG3	D4	IRQ1	E4	RFS1
A5	ADDR3	B5	ADDR2	C5	ADDR1	D5	FLAG1	E5	VDD
A6	ADDR6	B6	ADDR5	C6	ADDR4	D6	VDD	E6	GND
A7	ADDR7	B7	ADDR9	C7	ADDR10	D7	VDD	E7	GND
A8	ADDR8	B8	ADDR12	C8	ADDR13	D8	VDD	E8	GND
A9	ADDR11	B9	ADDR15	C9	ADDR16	D9	VDD	E9	GND
A10	ADDR14	B10	ADDR19	C10	ADDR20	D10	VDD	E10	VDD
A11	ADDR17	B11	ADDR21	C11	ADDR22	D11	BMS	E11	ID0
A12	ADDR18	B12	ADDR23	C12	RESET	D12	TMS	E12	TDI
A13	NC8	B13	GND	C13	BSEL	D13	TRST	E13	ID1
A14	NC7	B14	TCK	C14	TDO	D14	EMU	E14	FLAG4
F1	TCLK1	G1	PWM_ EVENT1	H1	PWM_ EVENT0	J1	CLKIN	K1	DMAR1
F2	DR1B	G2	DT1B	H2	BR1	J2	XTAL	K2	SDCLK0
F3	DR1A	G3	DT1A	H3	BR2	J3	SDCLK1	K3	HBR
F4	VDD	G4	VDD	H4	VDD	J4	VDD	K4	SDWE
F5	GND	G5	GND	H5	GND	J5	GND	K5	VDD
F6	GND	G6	GND	H6	GND	J6	GND	K6	GND
F7	GND	G7	GND	H7	GND	J7	GND	K7	GND
F8	GND	G8	GND	H8	GND	J8	GND	K8	GND
F9	GND	G9	GND	H9	GND	J9	GND	K9	GND
F10	GND	G10	GND	H10	GND	J10	GND	K10	VDD
F11	VDD	G11	VDD	H11	VDD	J11	VDD	K11	DATA19
F12	FLAG6	G12	DATA31	H12	DATA28	J12	DATA24	K12	DATA21
F13	FLAG5	G13	DATA30	H13	DATA27	J13	DATA25	K13	DATA20
F14	FLAG7	G14	DATA29	H14	DATA26	J14	DATA23	K14	DATA22
L1	DMAR2	M1	RAS	N1	DQM	P1	NC3		
L2	CAS	M2	SDCKE	N2	HBG	P2	NC4		
L3	SDA10	M3	DMAG1	N3	BMSTR	P3	GND		
L4	DMAG2	M4	CS	N4	SBTS	P4	WR		
L5	VDD	M5	RD	N5	REDY	P5	SW		
L6	VDD	M6	CPA	N6	GND	P6	MS0		
L7	VDD	M7	ACK	N7	MS1	P7	MS2		
L8	VDD	M8	FLAG10	N8	FLAG11	P8	MS3		
L9	VDD	M9	DATA2	N9	DATA1	P9	FLAG9		
L10	DATA8	M10	DATA5	N10	DATA4	P10	FLAG8		
L11	DATA13	M11	DATA9	N11	DATA7	P11	DATA0		
L12	DATA16	M12	DATA12	N12	DATA10	P12	DATA3		
L13	DATA17	M13	DATA14	N13	DATA11	P13	DATA6		
L14	DATA18	M14	DATA15	N14	NC6	P14	NC5		

196-BALL MINI-BGA PIN CONFIGURATION

14	13	12	11	10	9	8	7	6	5	4	3	2	1	
NC7	NC8	ADDR18	ADDR17	ADDR14	ADDR11	ADDR8	ADDR7	ADDR6	ADDR3	ADDR0	FLAG2	NC2	NC1	A
TCK	GND	ADDR23	ADDR21	ADDR19	ADDR15	ADDR12	ADDR9	ADDR5	ADDR2	FLAG0	$\overline{\text{IRQ0}}$	RFS0	DR0A	B
TDO	BSEL	$\overline{\text{RESET}}$	ADDR22	ADDR20	ADDR16	ADDR13	ADDR10	ADDR4	ADDR1	FLAG3	$\overline{\text{IRQ2}}$	RCLK0	TCLK0	C
$\overline{\text{EMU}}$	$\overline{\text{TRST}}$	TMS	$\overline{\text{BMS}}$	VDD	VDD	VDD	VDD	VDD	FLAG1	$\overline{\text{IRQ1}}$	DR0B	TFS0	RCLK1	D
FLAG4	ID1	TDI	ID0	VDD	GND	GND	GND	GND	VDD	RFS1	DT0A	DT0B	TFS1	E
FLAG7	FLAG5	FLAG6	VDD	GND	GND	GND	GND	GND	GND	VDD	DR1A	DR1B	TCLK1	F
DATA29	DATA30	DATA31	VDD	GND	GND	GND	GND	GND	GND	VDD	DT1A	DT1B	PWM_ EVENT1	G
DATA26	DATA27	DATA28	VDD	GND	GND	GND	GND	GND	GND	VDD	$\overline{\text{BR2}}$	$\overline{\text{BR1}}$	PWM_ EVENT0	H
DATA23	DATA25	DATA24	VDD	GND	GND	GND	GND	GND	GND	VDD	SDCLK1	XTAL	CLKIN	J
DATA22	DATA20	DATA21	DATA19	VDD	GND	GND	GND	GND	VDD	$\overline{\text{SDWE}}$	$\overline{\text{HBR}}$	SDCLK0	$\overline{\text{DMAR1}}$	K
DATA18	DATA17	DATA16	DATA13	DATA8	VDD	VDD	VDD	VDD	VDD	$\overline{\text{DMAG2}}$	SDA10	$\overline{\text{CAS}}$	$\overline{\text{DMAR2}}$	L
DATA15	DATA14	DATA12	DATA9	DATA5	DATA2	FLAG10	ACK	$\overline{\text{CPA}}$	$\overline{\text{RD}}$	$\overline{\text{CS}}$	$\overline{\text{DMAG1}}$	SDCKE	$\overline{\text{RAS}}$	M
NC6	DATA11	DATA10	DATA7	DATA4	DATA1	FLAG11	$\overline{\text{MS1}}$	GND	REDY	$\overline{\text{SBTS}}$	BMSTR	$\overline{\text{HBG}}$	DQM	N
NC5	DATA6	DATA3	DATA0	FLAG8	FLAG9	$\overline{\text{MS3}}$	$\overline{\text{MS2}}$	$\overline{\text{MS0}}$	$\overline{\text{SW}}$	$\overline{\text{WR}}$	GND	NC4	NC3	P