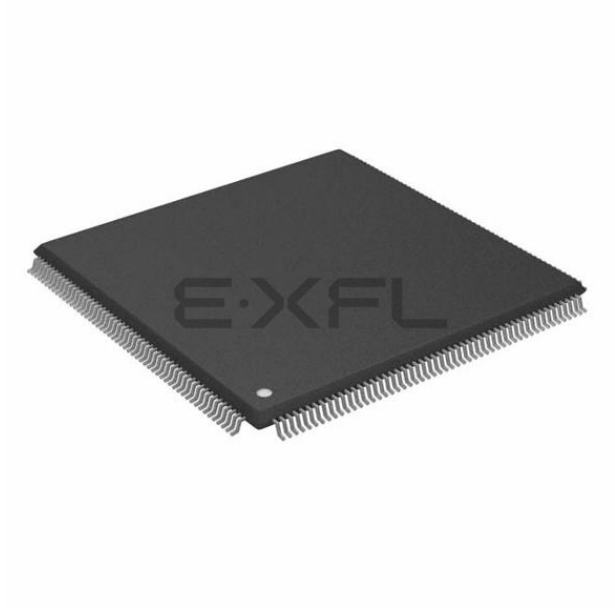

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Floating Point
Interface	Host Interface, Serial Port
Clock Rate	60MHz
Non-Volatile Memory	External
On-Chip RAM	64kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	0°C ~ 85°C (TC)
Mounting Type	Surface Mount
Package / Case	208-BFQFP
Supplier Device Package	208-MQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21065lksz-240

- EE-305: Designing and Debugging Systems with SHARC Processors
- EE-323: Implementing Dynamically Loaded Software Modules
- EE-328: Migrating from ADSP-2106x/2116x to ADSP-2126x/2136x/2137x SHARC® Processors
- EE-330: Windows Vista Compatibility in VisualDSP++ 5.0 Development Tools
- EE-332: Cycle Counting and Profiling
- EE-340: Connecting SHARC® and Blackfin® Processors over SPI
- EE-42: C-Programs on the ADSP-2106x
- EE-45: Using the ADSP-2106x/21020 EZ-ICE DBWIN Utility
- EE-46: SHARC Internal Power Measurements
- EE-47: ADSP-2106x Link Ports - Maximum Throughput
- EE-56: Tips and Tricks on SHARC® EPROM and Host Boot Loader
- EE-62: Accessing Short Word Memory In C
- EE-68: Analog Devices JTAG Emulation Technical Reference
- EE-69: Understanding and Using Linker Description Files on SHARC Processors
- EE-70: ADSP-2106x SPORT DTx pins: Is There Potential MCM Data Contention Between Different SHARCs
- EE-74: Analog Devices Serial Port Development and Troubleshooting Guide
- EE-84: External Port DMA Modes of Operation for SHARC Processors
- EE-85: Recommended Handling of Unused SHARC Pins
- EE-86: Interfacing SHARC 2106x DSPs to PLX 9080 PCI Bridge Chips
- EE-98: Using External Bus Arbitration to Group More Than Two ADSP-21065L into a Multiprocessing Cluster
- Interfacing the ADSP21065L SHARC DSP to the AD1819A AC-97 Soundport Codec
- TN: Interfacing I2S Compatible Audio Devices to the ADSP-21065L
- TN: Using the Low Cost, High Performance ADSP21065L DSP for Digital Audio Applications

Data Sheet

- ADSP-21065L: SHARC, 198 MFLOPS, 3.3v Data Sheet

Evaluation Kit Manuals

- ADSP-21061, 21065L and the 21160M EZ-KIT Lite® Installation Procedure

Integrated Circuit Anomalies

- ADSP-21065L Anomaly List for Revision 0.0, 0.1, 0.2, 0.3

Processor Manuals

- ADSP-21065L Technical Reference
- ADSP-21065L User's Manual
- Getting Started with SHARC
- SHARC Processors: Manuals

Product Highlight

- ADSP-21065L SHARC DSP 32-Bit Floating Point Performance Product Highlight
- EZ-KIT Lite for ADSP-21065L SHARC DSP Product Highlight
- SHARC Processor Family

SOFTWARE AND SYSTEMS REQUIREMENTS

- Software and Tools Anomalies Search

TOOLS AND SIMULATIONS

- ADSP-21065L: MBGA Package
- ADSP-21065L: PQFP package
- Designing with BGA
- ADSP-21065L IBIS Datafile (QFP Package)

REFERENCE MATERIALS

Product Selection Guide

- ADI Complementary Parts Guide - Supervisory Devices and DSP Processors

Technical Articles

- An Efficient Asynchronous Sampling-rate Conversion Algorithm for Multi-channel Audio Applications

DESIGN RESOURCES

- ADSP-21065L Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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SAMPLE AND BUY

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544 Kbits Configurable On-Chip SRAM

Dual-Ported for Independent Access by Core Processor and DMA

Configurable in Combinations of 16-, 32-, 48-Bit Data and Program Words in Block 0 and Block 1

DMA Controller

Ten DMA Channels—Two Dedicated to the External Port and Eight Dedicated to the Serial Ports

Background DMA Transfers at up to 66 MHz, in Parallel with Full Speed Processor Execution

Performs Transfers Between:

- **Internal RAM and Host**
- **Internal RAM and Serial Ports**
- **Internal RAM and Master or Slave SHARC**
- **Internal RAM and External Memory or I/O Devices**
- **External Memory and External Devices**

Host Processor Interface

Efficient Interface to 8-, 16-, and 32-Bit Microprocessors

Host Can Directly Read/Write ADSP-21065L IOP Registers

Multiprocessing

Distributed On-Chip Bus Arbitration for Glueless, Parallel Bus Connect Between Two ADSP-21065Ls Plus Host

132 Mbytes/s Transfer Rate Over Parallel Bus

Serial Ports

Independent Transmit and Receive Functions

Programmable 3-Bit to 32-Bit Serial Word Width

I^2S Support Allowing Eight Transmit and Eight Receive Channels

Glueless Interface to Industry Standard Codecs

TDM Multichannel Mode with μ-Law/A-Law Hardware Companding

Multichannel Signaling Protocol

structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The ADSP-21065L's two DAGs contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reducing overhead, increasing performance, and simplifying implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set
The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the ADSP-21065L can conditionally execute a multiply, an add, a subtract and a branch, all in a single instruction.

ADSP-21065L FEATURES

The ADSP-21065L is designed to achieve the highest system throughput to enable maximum system performance. It can be clocked by either a crystal or a TTL-compatible clock signal. The ADSP-21065L uses an input clock with a frequency equal to half the instruction rate—a 33 MHz input clock yields a 15 ns processor cycle (which is equivalent to 66 MHz). Interfaces on the ADSP-21065L operate as shown below. Hereafter in this document, 1x = input clock frequency, and 2x = processor's instruction rate.

The following clock operation ratings are based on 1x = 33 MHz (instruction rate/core = 66 MHz):

SDRAM	66 MHz
External SRAM	33 MHz
Serial Ports	33 MHz
Multiprocessing	33 MHz
Host (Asynchronous)	33 MHz

Augmenting the ADSP-21000 family core, the ADSP-21065L adds the following architectural features:

Dual-Ported On-Chip Memory
The ADSP-21065L contains 544 Kbits of on-chip SRAM, organized into two banks: Bank 0 has 288 Kbits, and Bank 1 has 256 Kbits. Bank 0 is configured with 9 columns of 2K × 16 bits, and Bank 1 is configured with 8 columns of 2K × 16 bits. Each memory block is dual-ported for single-cycle, independent accesses by the core processor and I/O processor or DMA controller. The dual-ported memory and separate on-chip buses allow two data transfers from the core and one from I/O, all in a single cycle (see Figure 4 for the ADSP-21065L Memory Map).

On the ADSP-21065L, the memory can be configured as a maximum of 16K words of 32-bit data, 34K words for 16-bit data, 10K words of 48-bit instructions (and 40-bit data) or combinations of different word sizes up to 544 Kbits. All the memory can be accessed as 16-bit, 32-bit or 48-bit.

While each memory block can store combinations of code and data, accesses are most efficient when one block stores data, using the DM bus for transfers, and the other block stores instructions and data, using the PM bus for transfers. Using the DM and PM busses in this way, with one dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache. Single-cycle execution is also maintained when one of the data operands is transferred to or from off-chip, via the ADSP-21065L's external port.

Off-Chip Memory and Peripherals Interface
The ADSP-21065L's external port provides the processor's interface to off-chip memory and peripherals. The 64M words, off-chip address space is included in the ADSP-21065L's unified address space. The separate on-chip buses—for program memory, data memory and I/O—are multiplexed at the external port to create an external system bus with a single 24-bit address bus, four memory selects, and a single 32-bit data bus. The on-chip Super Harvard Architecture provides three bus performance, while the off-chip unified address space gives flexibility to the designer.

SDRAM Interface
The SDRAM interface enables the ADSP-21065L to transfer data to and from synchronous DRAM (SDRAM) at 2x clock frequency. The synchronous approach coupled with 2x clock frequency supports data transfer at a high throughput—up to 220 Mbytes/sec.

The SDRAM interface provides a glueless interface with standard SDRAMs—16 Mb, 64 Mb, and 128 Mb—and includes options to support additional buffers between the ADSP-21065L and SDRAM. The SDRAM interface is extremely flexible and provides capability for connecting SDRAMs to any one of the ADSP-21065L's four external memory banks.

Systems with several SDRAM devices connected in parallel may require buffering to meet overall system timing requirements. The ADSP-21065L supports pipelining of the address and control signals to enable such buffering between itself and multiple SDRAM devices.

Host Processor Interface
The ADSP-21065L's host interface provides easy connection to standard microprocessor buses—8-, 16-, and 32-bit—requiring little additional hardware. Supporting asynchronous transfers at speeds up to 1x clock frequency, the host interface is accessed through the ADSP-21065L's external port. Two channels of DMA are available for the host interface; code and data transfers are accomplished with low software overhead.

The host processor requests the ADSP-21065L's external bus with the host bus request ($\overline{\text{HBR}}$), host bus grant ($\overline{\text{HBG}}$), and ready (REDY) signals. The host can directly read and write the IOP registers of the ADSP-21065L and can access the DMA channel setup and mailbox registers. Vector interrupt support enables efficient execution of host commands.

DMA Controller
The ADSP-21065L's on-chip DMA controller allows zero-overhead, nonintrusive data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions.

DMA transfers can occur between the ADSP-21065L's internal memory and either external memory, external peripherals, or a host processor. DMA transfers can also occur between the ADSP-21065L's internal memory and its serial ports. DMA transfers between external memory and external peripheral devices are another option. External bus packing to 16-, 32-, or 48-bit internal words is performed during DMA transfers.

Ten channels of DMA are available on the ADSP-21065L—eight via the serial ports, and two via the processor's external port (for either host processor, other ADSP-21065L, memory or

I/O transfers). Programs can be downloaded to the ADSP-21065L using DMA transfers. Asynchronous off-chip peripherals can control two DMA channels using DMA Request/Grant lines ($\overline{DMAR}_{1-2}$, $\overline{DMAG}_{1-2}$). Other DMA features include interrupt generation on completion of DMA transfers and DMA chaining for automatically linked DMA transfers.

Serial Ports
The ADSP-21065L features two synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices. The serial ports can operate at 1x clock frequency, providing each with a maximum data rate of 33 Mbit/s. Each serial port has a primary and a secondary set of transmit and receive channels. Independent transmit and receive functions provide greater flexibility for serial communications. Serial port data can be automatically transferred to and from on-chip memory via DMA. Each of the serial ports supports three operation modes: DSP serial port mode, I^2S mode (an interface commonly used by audio codecs), and TDM (Time Division Multiplex) multichannel mode.

The serial ports can operate with little-endian or big-endian transmission formats, with selectable word lengths of 3 bits to 32 bits. They offer selectable synchronization and transmit modes and optional μ-law or A-law companding. Serial port clocks and frame syncs can be internally or externally generated. The serial ports also include keyword and keymask features to enhance interprocessor communication.

Programmable Timers and General-Purpose I/O Ports
The ADSP-21065L has two independent timer blocks, each of which performs two functions—Pulsewidth Generation and Pulse Count and Capture.

In Pulsewidth Generation mode, the ADSP-21065L can generate a modulated waveform with an arbitrary pulsewidth within a maximum period of 71.5 secs.

In Pulse Counter mode, the ADSP-21065L can measure either the high or low pulsewidth and the period of an input waveform.

The ADSP-21065L also contains twelve programmable, general purpose I/O pins that can function as either input or output. As output, these pins can signal peripheral devices; as input, these pins can provide the test for conditional branching.

Program Booting
The internal memory of the ADSP-21065L can be booted at system power-up from an 8-bit EPROM, a host processor, or external memory. Selection of the boot source is controlled by the $\overline{BMS}$ (Boot Memory Select) and BSEL (EPROM Boot) pins. Either 8-, 16-, or 32-bit host processors can be used for booting. For details, see the descriptions of the $\overline{BMS}$ and BSEL pins in the Pin Descriptions section of this data sheet.

Multiprocessing
The ADSP-21065L offers powerful features tailored to multiprocessing DSP systems. The unified address space allows direct interprocessor accesses of both ADSP-21065L's IOP registers. Distributed bus arbitration logic is included on-chip for simple, glueless connection of systems containing a maximum of two ADSP-21065Ls and a host processor. Master processor changeover incurs only one cycle of overhead. Bus lock allows indivisible read-modify-write sequences for semaphores. A vector interrupt is provided for interprocessor commands. Maximum throughput for interprocessor data transfer is 132 Mbytes/sec over the external port.

DEVELOPMENT TOOLS
The ADSP-21065L is supported with a complete set of software and hardware development tools, including the EZ-ICE® In-Circuit Emulator and development software.

The same EZ-ICE hardware that you use for the ADSP-21060/ ADSP-21062 also fully emulates the ADSP-21065L.

Both the SHARC Development Tools family and the VisualDSP® integrated project management and debugging environment support the ADSP-21065L. The VisualDSP project management environment enables you to develop and debug an application from within a single integrated program.

The SHARC Development Tools include an easy to use Assembler that is based on an algebraic syntax; an Assembly library/ librarian; a linker; a loader; a cycle-accurate, instruction-level simulator; a C compiler; and a C run-time library that includes DSP and mathematical functions.

Debugging both C and Assembly programs with the Visual DSP debugger, you can:

- View Mixed C and Assembly Code
- Insert Break Points
- Set Watch Points
- Trace Bus Activity
- Profile Program Execution
- Fill and Dump Memory
- Create Custom Debugger Windows

The Visual IDE enables you to define and manage multiuser projects. Its dialog boxes and property pages enable you to configure and manage all of the SHARC Development Tools. This capability enables you to:

- Control how the development tools process inputs and generate outputs.
- Maintain a one-to-one correspondence with the tool's command line switches.

The EZ-ICE Emulator uses the IEEE 1149.1 JTAG test access port of the ADSP-21065L processor to monitor and control the target board processor during emulation. The EZ-ICE provides full-speed emulation, allowing inspection and modification of memory, registers, and processor stacks. Nonintrusive in-circuit emulation is assured by the use of the processor's JTAG interface—the emulator does not affect target system loading or timing.

In addition to the software and hardware development tools available from Analog Devices, third parties provide a wide range of tools supporting the SHARC processor family. Hardware tools include SHARC PC plug-in cards multiprocessor SHARC VME boards, and daughter and modules with multiple SHARCs and additional memory. These modules are based on the SHARCPAC™ module specification. Third Party software tools include an Ada compiler, DSP libraries, operating systems, and block diagram design tools.

Additional Information
For detailed information on the ADSP-21065L instruction set and architecture, see the *ADSP-21065L SHARC User's Manual*, Third Edition, and the *ADSP-21065L SHARC Technical Reference.*

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PIN DESCRIPTIONS

ADSP-21065L pin definitions are listed below. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$).

Unused inputs should be tied or pulled to VDD or GND, except for $\text{ADDR}_{23\text{-}0}$, $\text{DATA}_{31\text{-}0}$, $\text{FLAG}_{11\text{-}0}$, $\overline{\text{SW}}$, and inputs that have internal pull-up or pull-down resistors ($\overline{\text{CPA}}$, ACK, DTxX, DRxX, TCLKx, RCLKx, TMS, and TDI)—these pins can be left floating. These pins have a logic-level hold circuit that prevents the input from floating internally.

I = Input S = Synchronous P = Power Supply (O/D) = Open Drain
O = Output A = Asynchronous G = Ground (A/D) = Active Drive
T = Three-state (when $\overline{\text{SBTS}}$ is asserted, or when the ADSP-2106x is a bus slave)

Pin	Type	Function
$\text{ADDR}_{23\text{-}0}$	I/O/T	**External Bus Address**. The ADSP-21065L outputs addresses for external memory and peripherals on these pins. In a multiprocessor system the bus master outputs addresses for read/writes of the IOP registers of the other ADSP-21065L. The ADSP-21065L inputs addresses when a host processor or multiprocessing bus master is reading or writing its IOP registers.
$\text{DATA}_{31\text{-}0}$	I/O/T	**External Bus Data**. The ADSP-21065L inputs and outputs data and instructions on these pins. The external data bus transfers 32-bit single-precision floating-point data and 32-bit fixed-point data over bits 31-0. 16-bit short word data is transferred over bits 15-0 of the bus. Pull-up resistors on unused DATA pins are not necessary.
$\overline{\text{MS}}_{3\text{-}0}$	I/O/T	**Memory Select Lines**. These lines are asserted as chip selects for the corresponding banks of external memory. Internal $\text{ADDR}_{25\text{-}24}$ are decoded into $\overline{\text{MS}}_{3\text{-}0}$. The $\overline{\text{MS}}_{3\text{-}0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the $\overline{\text{MS}}_{3\text{-}0}$ lines are inactive; they are active, however, when a conditional memory access instruction is executed, whether or not the condition is true. Additionally, an $\overline{\text{MS}}_{3\text{-}0}$ line which is mapped to SDRAM may be asserted even when no SDRAM access is active. In a multiprocessor system, the $\overline{\text{MS}}_{3\text{-}0}$ lines are output by the bus master.
$\overline{\text{RD}}$	I/O/T	**Memory Read Strobe**. This pin is asserted when the ADSP-21065L reads from external memory devices or from the IOP register of another ADSP-21065L. External devices (including another ADSP-21065L) must assert $\overline{\text{RD}}$ to read from the ADSP-21065L's IOP registers. In a multiprocessor system, $\overline{\text{RD}}$ is output by the bus master and is input by another ADSP-21065L.
$\overline{\text{WR}}$	I/O/T	**Memory Write Strobe.** This pin is asserted when the ADSP-21065L writes to external memory devices or to the IOP register of another ADSP-21065L. External devices must assert $\overline{\text{WR}}$ to write to the ADSP-21065L's IOP registers. In a multiprocessor system, $\overline{\text{WR}}$ is output by the bus master and is input by the other ADSP-21065L.
$\overline{\text{SW}}$	I/O/T	**Synchronous Write Select.** This signal interfaces the ADSP-21065L to synchronous memory devices (including another ADSP-21065L). The ADSP-21065L asserts $\overline{\text{SW}}$ to provide an early indication of an impending write cycle, which can be aborted if $\overline{\text{WR}}$ is not later asserted (e.g., in a conditional write instruction). In a multiprocessor system, $\overline{\text{SW}}$ is output by the bus master and is input by the other ADSP-21065L to determine if the multiprocessor access is a read or write. $\overline{\text{SW}}$ is asserted at the same time as the address output.
ACK	I/O/S	**Memory Acknowledge**. External devices can deassert ACK to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access. The ADSP-21065L deasserts ACK as an output to add wait states to a synchronous access of its IOP registers. In a multiprocessor system, a slave ADSP-21065L deasserts the bus master's ACK input to add wait state(s) to an access of its IOP registers. The bus master has a keeper latch on its ACK pin that maintains the input at the level to which it was last driven.
$\overline{\text{SBTS}}$	I/S	**Suspend Bus Three-State.** External devices can assert $\overline{\text{SBTS}}$ to place the external bus address, data, selects, and strobes—but not SDRAM control pins—in a high impedance state for the following cycle. If the ADSP-21065L attempts to access external memory while $\overline{\text{SBTS}}$ is asserted, the processor will halt and the memory access will not finish until $\overline{\text{SBTS}}$ is deasserted. $\overline{\text{SBTS}}$ should only be used to recover from host processor/ADSP-21065L deadlock.
$\overline{\text{IRQ}}_{2\text{-}0}$	I/A	Interrupt Request Lines. May be either edge-triggered or level-sensitive.
$\text{FLAG}_{11\text{-}0}$	I/O/A	Flag Pins. Each is configured via control bits as either an input or an output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals.

Pin	Type	Function
$\overline{\text{BMS}}$	I/O/T*	**Boot Memory Select.** Output: used as chip select for boot EPROM devices (when BSEL = 1). In a multiprocessor system, $\overline{\text{BMS}}$ is output by the bus master. Input: When low, indicates that no booting will occur and that the ADSP-21065L will begin executing instructions from external memory. See following table. This input is a system configuration selection which should be hardwired. *Three-statable only in EPROM boot mode (when $\overline{\text{BMS}}$ is an output). **BSEL** / **$\overline{\text{BMS}}$** / **Booting Mode** 1 / Output / EPROM (connect $\overline{\text{BMS}}$ to EPROM chip select). 0 / 1 (Input) / Host processor (HBW [SYSCON] bit selects host bus width). 0 / 0 (Input) / No booting. Processor executes from external memory.
CLKIN	I	**Clock In.** Used in conjunction with XTAL, configures the ADSP-21065L to use either its internal clock generator or an external clock source. The external crystal should be rated at 1x frequency. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. The ADSP-21065L's internal clock generator multiplies the 1x clock to generate 2x clock for its core and SDRAM. It drives 2x clock out on the SDCLKx pins for the SDRAM interface to use. See also SDCLKx. Connecting the 1x external clock to CLKIN while leaving XTAL unconnected configures the ADSP-21065L to use the external clock source. The instruction cycle rate is equal to 2x CLKIN. CLKIN may not be halted, changed, or operated below the specified frequency.
$\overline{\text{RESET}}$	I/A	**Processor Reset.** Resets the ADSP-21065L to a known state and begins execution at the program memory location specified by the hardware reset vector address. This input must be asserted at power-up.
TCK	I	**Test Clock (JTAG).** Provides an asynchronous clock for JTAG boundary scan.
TMS	I/S	**Test Mode Select (JTAG).** Used to control the test state machine. TMS has a 20 kΩ internal pull-up resistor.
TDI	I/S	**Test Data Input (JTAG).** Provides serial data for the boundary scan logic. TDI has a 20 kΩ internal pull-up resistor.
TDO	O	**Test Data Output (JTAG).** Serial scan output of the boundary scan path.
$\overline{\text{TRST}}$	I/A	**Test Reset (JTAG).** Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-21065L. $\overline{\text{TRST}}$ has a 20 kΩ internal pull-up resistor.
$\overline{\text{EMU}}$ (O/D)	O	**Emulation Status.** Must be connected to the ADSP-21065L EZ-ICE target board connector only.
BMSTR	O	**Bus Master Output.** In a multiprocessor system, indicates whether the ADSP-21065L is current bus master of the shared external bus. The ADSP-21065L drives BMSTR high only while it is the bus master. In a single-processor system (ID = 00), the processor drives this pin high.
$\overline{\text{CAS}}$	I/O/T	**SDRAM Column Access Strobe.** Provides the column address. In conjunction with $\overline{\text{RAS}}$, $\overline{\text{MS}}$x, $\overline{\text{SDWE}}$, SDCLKx, and sometimes SDA10, defines the operation for the SDRAM to perform.
$\overline{\text{RAS}}$	I/O/T	**SDRAM Row Access Strobe.** Provides the row address. In conjunction with $\overline{\text{CAS}}$, $\overline{\text{MS}}$x, $\overline{\text{SDWE}}$, SDCLKx, and sometimes SDA10, defines the operation for the SDRAM to perform.
$\overline{\text{SDWE}}$	I/O/T	**SDRAM Write Enable.** In conjunction with $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, $\overline{\text{MS}}$x, SDCLKx, and sometimes SDA10, defines the operation for the SDRAM to perform.
DQM	O/T	**SDRAM Data Mask.** In write mode, DQM has a latency of zero and is used to block write operations.
$\text{SDCLK}_{1\text{-}0}$	I/O/S/T	**SDRAM 2x Clock Output.** In systems with multiple SDRAM devices connected in parallel, supports the corresponding increased clock load requirements, eliminating need of off-chip clock buffers. Either SDCLK_1 or both SDCLKx pins can be three-stated.
SDCKE	I/O/T	**SDRAM Clock Enable.** Enables and disables the CLK signal. For details, see the data sheet supplied with your SDRAM device.

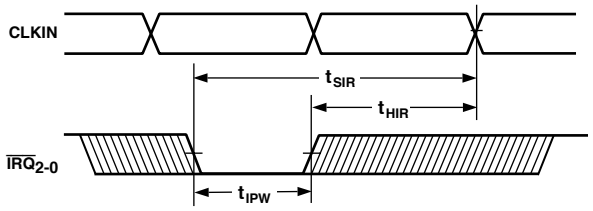


Figure 9. Interrupts

Parameter		Min	Max	Unit
Timer				
Timing Requirements:				
t_{STI}	Timer Setup Before SDCLK High	0.0		ns
t_{HTI}	Timer Hold After SDCLK High	6.0		ns
Switching Characteristics:				
t_{DTEX}	Timer Delay After SDCLK High		1.0	ns
t_{HTEX}	Timer Hold After SDCLK High	–5.0		ns

Parameter		Min	Max	Unit
Flags				
Timing Requirements:				
t_{SFI}	$FLAG_{11-0}$IN Setup Before SDCLK High[1]	–2.0		ns
t_{HFI}	$FLAG_{11-0}$IN Hold After SDCLK High[1]	6.0		ns
Switching Characteristics:				
t_{DFO}	$FLAG_{11-0}$OUT Delay After SDCLK High		1.0	ns
t_{HFO}	$FLAG_{11-0}$OUT Hold After SDCLK High	–4.0		ns
t_{DFOE}	SDCLK High to $FLAG_{11-0}$OUT Enable	–4.0		ns
t_{DFOD}	SDCLK High to $FLAG_{11-0}$OUT Disable		–1.75	ns

NOTE
[1]Flag inputs meeting these setup and hold times will affect conditional instructions in the following instruction cycle.

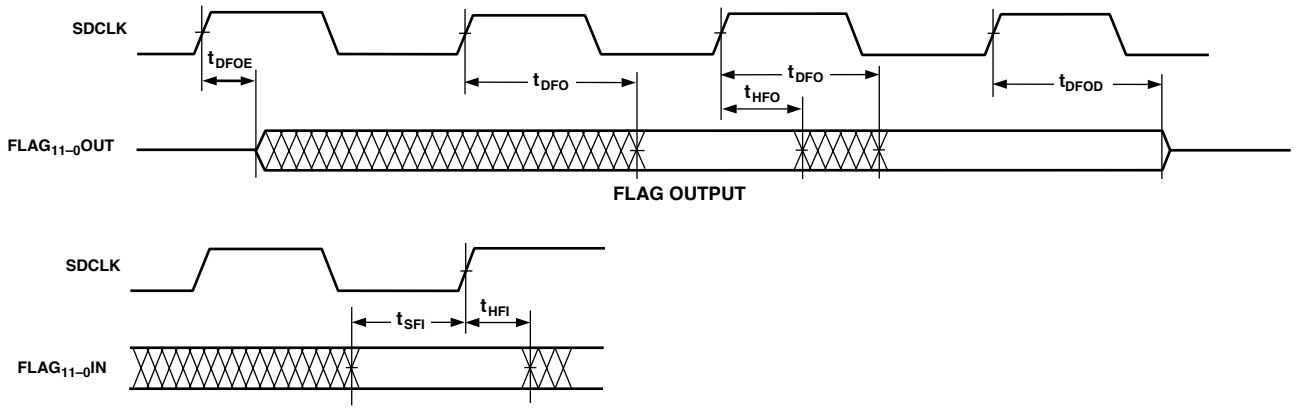


Figure 10. Flags

Memory Write—Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the ADSP-21065L is the bus master when accessing external memory space. These switching characteristics also apply for bus master synchronous read/write timing (see Synchronous Read/Write—Bus Master below). If these timing requirements are met, the synchronous read/write timing can be ignored (and vice versa). An exception to this is the ACK pin timing requirements as described in the note below.

Parameter		Min	Max	Unit
Timing Requirements:				
t_{DAAK}	ACK Delay from Address[1, 2]		24.0 + 30 DT + W	ns
t_{DSAK}	ACK Delay from $\overline{WR}$ Low[1]		19.5 + 24 DT + W	ns
Switching Characteristics:				
t_{DAWH}	Address, Selects to $\overline{WR}$ Deasserted[2]	29.0 + 31 DT + W		ns
t_{DAWL}	Address, Selects to $\overline{WR}$ Low[2]	3.5 + 6 DT		ns
t_{WW}	$\overline{WR}$ Pulsewidth	24.5 + 25 DT + W		ns
t_{DDWH}	Data Setup Before $\overline{WR}$ High	15.5 + 19 DT + W		ns
t_{DWHA}	Address Hold After $\overline{WR}$ Deasserted	0.0 + 1 DT + H		ns
t_{DATRWH}	Data Disable After $\overline{WR}$ Deasserted[3]	1.0 + 1 DT + H	4.0 + 1 DT + H	ns
t_{WWR}	$\overline{WR}$ High to $\overline{WR}$, $\overline{RD}$ Low	4.5 + 7 DT + H		ns
t_{WRDGL}	$\overline{WR}$ High to $\overline{DMAG}$x Low	11.0 + 13 DT + H		ns
t_{DDWR}	Data Disable Before $\overline{WR}$ or $\overline{RD}$ Low	3.5 + 6 DT + I		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	4.5 + 6 DT		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
H = t_{CK} (if an address hold cycle occurs, as specified in WAIT register; otherwise H = 0).
I = t_{CK} (if a bus idle cycle occurs, as specified in WAIT register; otherwise I = 0).

NOTES

[1]ACK is not sampled on external memory accesses that use the *Internal* wait state mode. For the first CLKIN cycle of a new external memory access, ACK must be valid by t_{DAAK} or t_{DSAK} or synchronous specification t_{SACKC} for wait state modes *External*, *Either*, or *Both* (*Both*, if the internal wait state is zero). For the second and subsequent cycles of a wait stated external memory access, synchronous specifications t_{SACKC} and t_{HACKC} must be met for wait state modes *External*, *Either*, or *Both* (*Both*, after internal wait states have completed).

[2]The falling edge of $\overline{MS}$x, $\overline{SW}$, and $\overline{BMS}$ is referenced.

[3]See System Hold Time Calculation under Test Conditions for calculation of hold times given capacitive and dc loads.

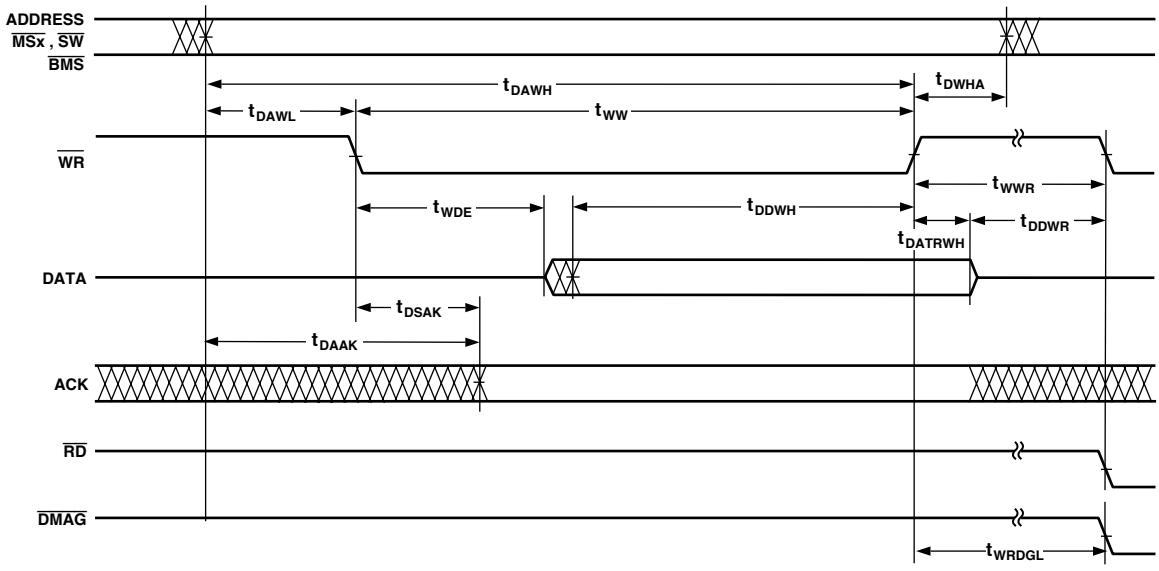


Figure 12. Memory Write—Bus Master

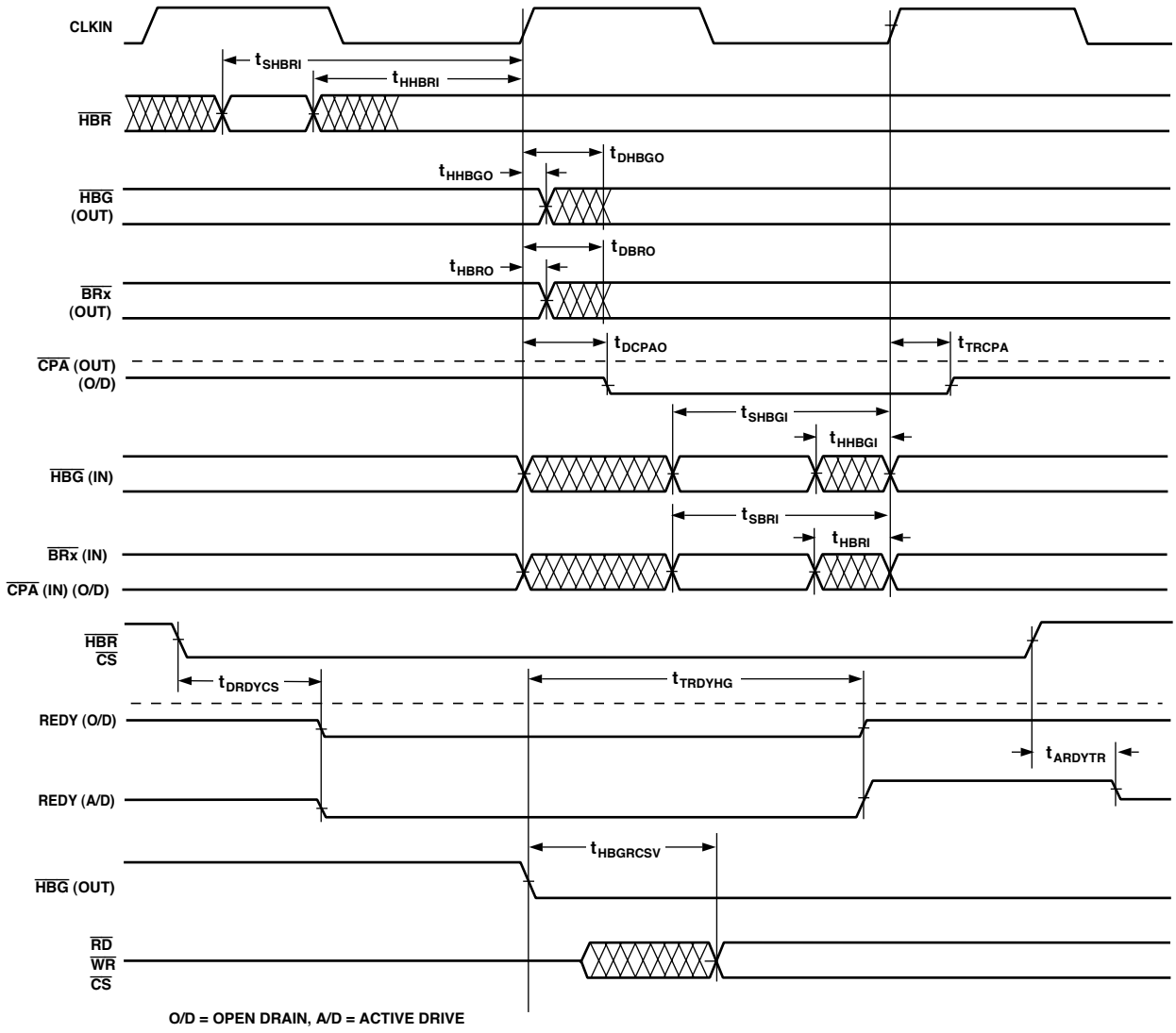


Figure 15. Multiprocessor Bus Request and Host Bus Request

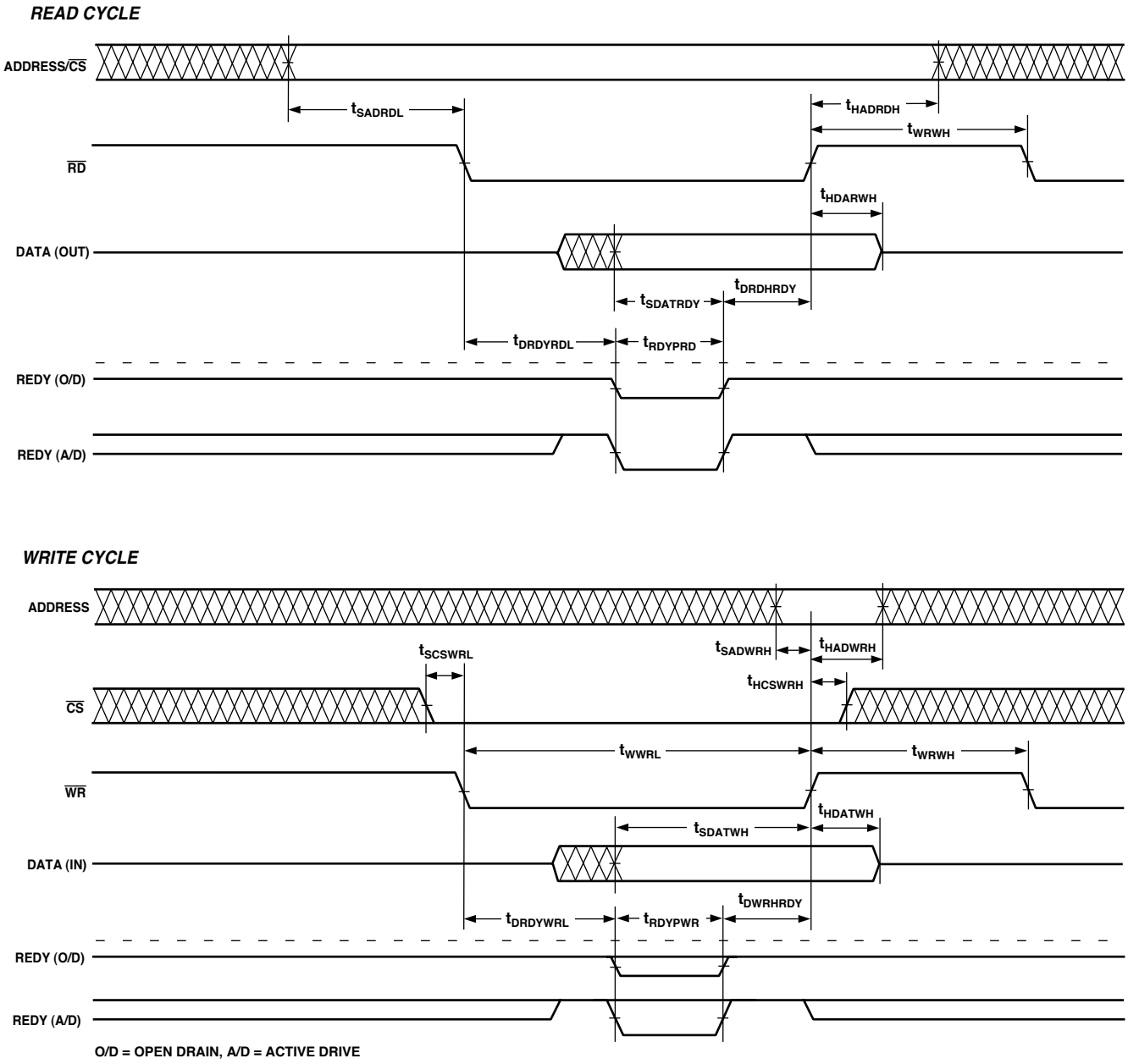


Figure 16. Asynchronous Read/Write—Host to ADSP-21065L

SDRAM Interface—Bus Master
Use these specifications for ADSP-21065L bus master accesses of SDRAM.

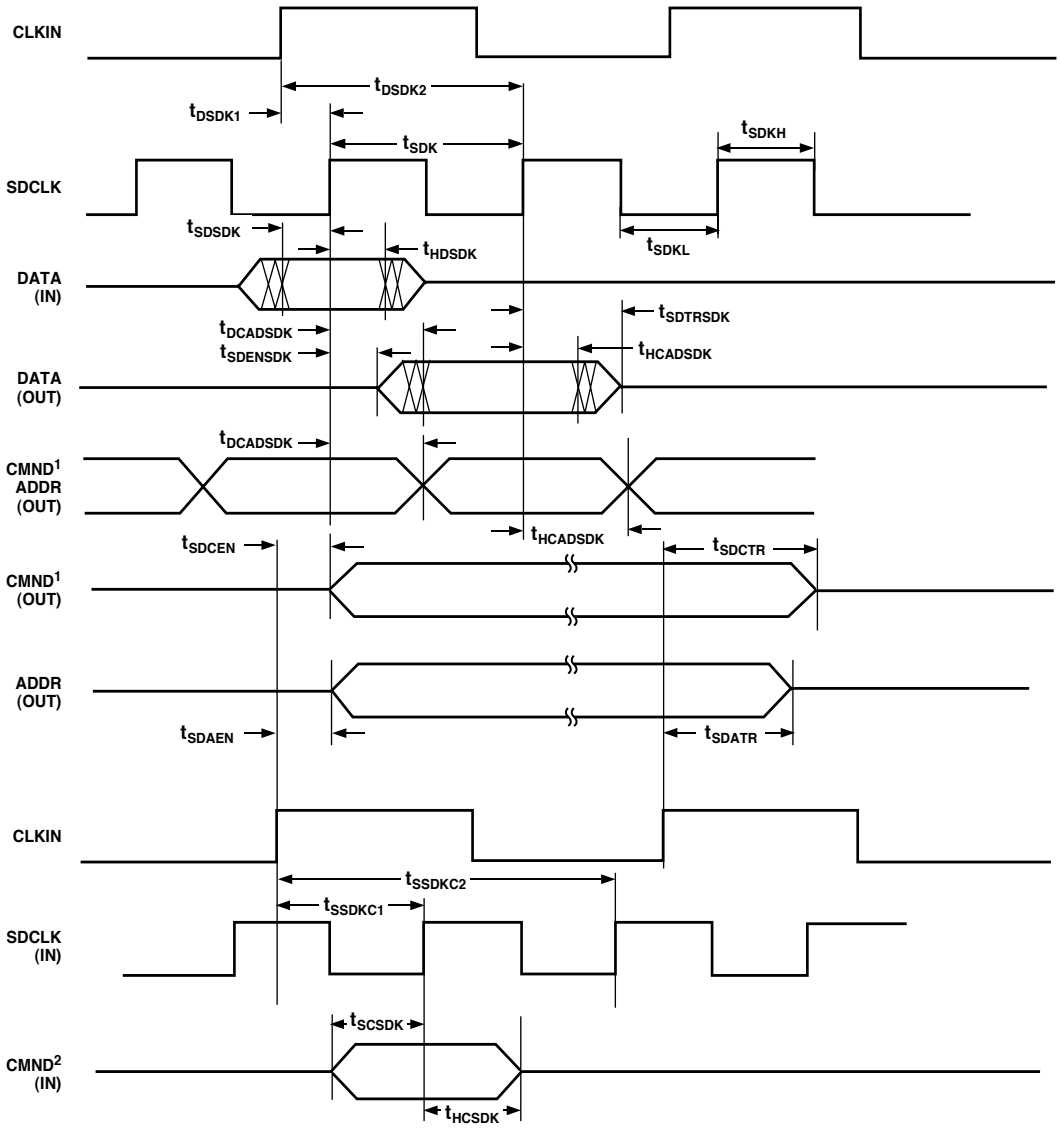
Parameter		Min	Max	Unit
Timing Requirements:				
t_{SDSDK}	Data Setup Before SDCLK	2.0		ns
t_{HDSDK}	Data Hold After SDCLK	1.25		ns
Switching Characteristics:				
t_{DSDK1}	First SDCLK Rise Delay After CLKIN	9.0 + 6 DT	12.75 + 6 DT	ns
t_{DSDK2}	Second SDCLK Rise Delay After CLKIN	25.5 + 22 DT	29.25 + 22 DT	ns
t_{SDK}	SDCLK Period	16.67	$t_{CK}/2$	ns
t_{SDKH}	SDCLK Width High	7.5 + 8 DT		ns
t_{SDKL}	SDCLK Width Low	6.5 + 8 DT		ns
$t_{DCADSDK}$	Command, Address, Data, Delay After SDCLK[1]		10.0 + 5 DT	ns
$t_{HCADSDK}$	Command, Address, Data, Hold After SDCLK[1]	4.5 + 5 DT		ns
$t_{SDTRSDK}$	Data Three-State After SDCLK		9.5 + 5 DT	ns
$t_{SDENSDK}$	Data Enable After SDCLK[2]	6.0 + 5 DT		ns
t_{SDCTR}	SDCLK, Command Three-State After CLKIN[1]	5.0 + 3 DT	9.75 + 3 DT	ns
t_{SDCEN}	SDCLK, Command Enable After CLKIN[1]	5.0 + 2 DT	10.0 + 2 DT	ns
t_{SDATR}	Address Three-State After CLKIN	–1.0 – 4 DT	3.0 – 4 DT	ns
t_{SDAEN}	Address Enable After CLKIN	1.0 – 2 DT	7.0 – 2 DT	ns

NOTES
[1]Command = SDCKE, $\overline{MS}$x, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, DQM, and SDA10.
[2]SDRAM controller adds one SDRAM CLK three-stated cycle delay ($t_{CK}/2$) on a Read followed by a Write.

SDRAM Interface—Bus Slave
These timing requirements allow a bus slave to sample the bus master's SDRAM command and detect when a refresh occurs.

Parameter		Min	Max	Unit
Timing Requirements:				
t_{SSDKC1}	First SDCLK Rise After CLKIN	6.50 + 16 DT	17.5 + 16 DT	ns
t_{SSDKC2}	Second SDCLK Rise After CLKIN	23.25	34.25	ns
t_{SCSDK}	Command Setup Before SDCLK*	0.0		ns
t_{HCSDK}	Command Hold After SDCLK*	2.0		ns

NOTE
*Command = SDCKE, $\overline{RAS}$, $\overline{CAS}$, and $\overline{SDWE}$.



NOTES
[1]COMMAND = SDCKE, $\overline{MS}_X$, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, DQM, AND SDA10.
[2]SDRAM CONTROLLER ADDS ONE SDRAM CLK THREE-STATED CYCLE DELAY ($t_{CK}/2$) ON A READ FOLLOWED BY A WRITE.

Figure 19. SDRAM Interface

Serial Ports

Parameter		Min	Max	Unit
External Clock				
Timing Requirements:				
t_{SFSE}	TFS/RFS Setup Before TCLK/RCLK[1]	4.0		ns
t_{HFSE}	TFS/RFS Hold After TCLK/RCLK[1]	4.0		ns
t_{SDRE}	Receive Data Setup Before RCLK[1]	1.5		ns
t_{HDRE}	Receive Data Hold After RCLK[1]	4.0		ns
t_{SCLKW}	TCLK/RCLK Width	9.0		ns
t_{SCLK}	TCLK/RCLK Period	t_{CK}		ns
Internal Clock				
Timing Requirements:				
t_{SFSI}	TFS Setup Before TCLK[2]; RFS Setup Before RCLK[1]	8.0		ns
t_{HFSI}	TFS/RFS Hold After TCLK/RCLK[1]	1.0		ns
t_{SDRI}	Receive Data Setup Before RCLK[1]	3.0		ns
t_{HDRI}	Receive Data Hold After RCLK[1]	3.0		ns
External or Internal Clock				
Switching Characteristics:				
t_{DFSE}	RFS Delay After RCLK (Internally Generated RFS)[2]		13.0	ns
t_{HOFSE}	RFS Hold After RCLK (Internally Generated RFS)[2]	3.0		ns
External Clock				
Switching Characteristics:				
t_{DFSE}	TFS Delay After TCLK (Internally Generated TFS)[2]		13.0	ns
t_{HOFSE}	TFS Hold After TCLK (Internally Generated TFS)[2]	3.0		ns
t_{DDTE}	Transmit Data Delay After TCLK[2]		12.5	ns
t_{HDTE}	Transmit Data Hold After TCLK[2]	4.0		ns
Internal Clock				
Switching Characteristics:				
t_{DFSI}	TFS Delay After TCLK (Internally Generated TFS)[2]		4.5	ns
t_{HOFSI}	TFS Hold After TCLK (Internally Generated TFS)[2]	–1.5		ns
t_{DDTI}	Transmit Data Delay After TCLK[2]		7.5	ns
t_{HDTI}	Transmit Data Hold After TCLK[2]	0.0		ns
t_{SCLKIW}	TCLK/RCLK Width	$(t_{SCLK}/2) - 2.5$	$(t_{SCLK}/2) + 2.5$	ns
Enable and Three-State				
Switching Characteristics:				
t_{DTENE}	Data Enable from External TCLK[2]	5.0		ns
t_{DDTTE}	Data Disable from External RCLK[2]		10.0	ns
t_{DTENI}	Data Enable from Internal TCLK[2]	0.0		ns
t_{DDTTI}	Data Disable from Internal TCLK[2]		3.0	ns
t_{DCLK}	TCLK/RCLK Delay from CLKIN		18.0 + 6 DT	ns
t_{DPTR}	SPORT Disable After CLKIN		14.0	ns
External Late Frame Sync				
$t_{DDTLFSE}$	Data Delay from Late External TFS or External RFS with MCE = 1, MFD = 0[3, 4]		10.5	ns
$t_{DTENLFSE}$	Data Enable from late FS or MCE = 1, MFD = 0[3, 4]	3.5		ns
$t_{DDTLSCK}$	Data Delay from TCLK/RCLK for Late External TFS or External RFS with MCE = 1, MFD = 0[3, 4]		12.0	ns
$t_{DTENLSCK}$	Data Enable from RCLK/TCLK for Late External FS or MCE = 1, MFD = 0[3, 4]	4.5		ns

NOTES

To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup-and-hold, 2) data delay and data setup-and-hold, and 3) SCLK width.

[1]Referenced to sample edge.

[2]Referenced to drive edge.

[3]MCE = 1, TFS enable and TFS valid follow $t_{DDTENFS}$ and $t_{DDTLFSE}$.

[4]If external RFS/TFS setup to RCLK/TCLK > $t_{SCLK}/2$ then $t_{DDTLSCK}$ and $t_{DTENLSCK}$ apply; otherwise $t_{DDTLFSE}$ and $t_{DTENLFS}$ apply.

*Word selected timing for I^2S mode is the same as TFS/RFS timing (normal framing only).

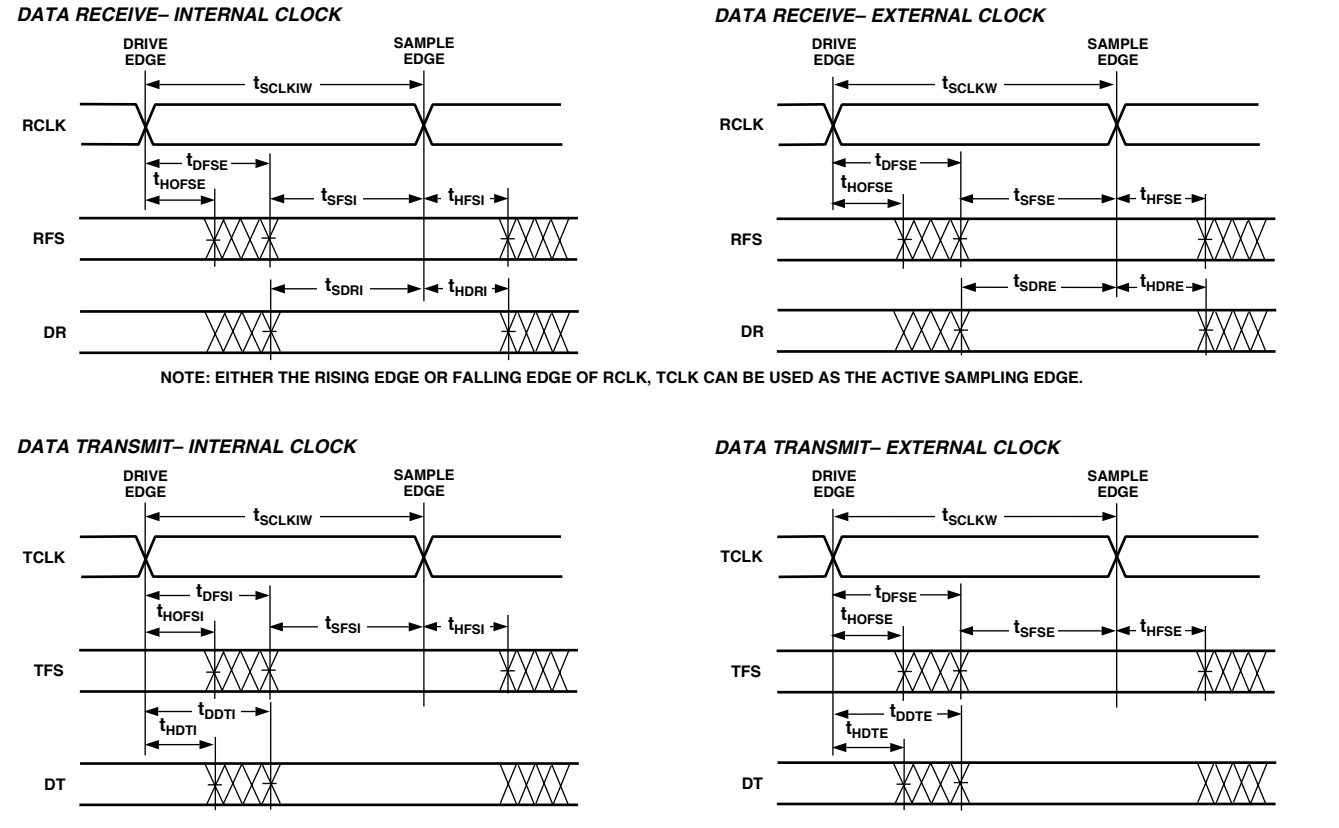


Figure 20. Serial Ports

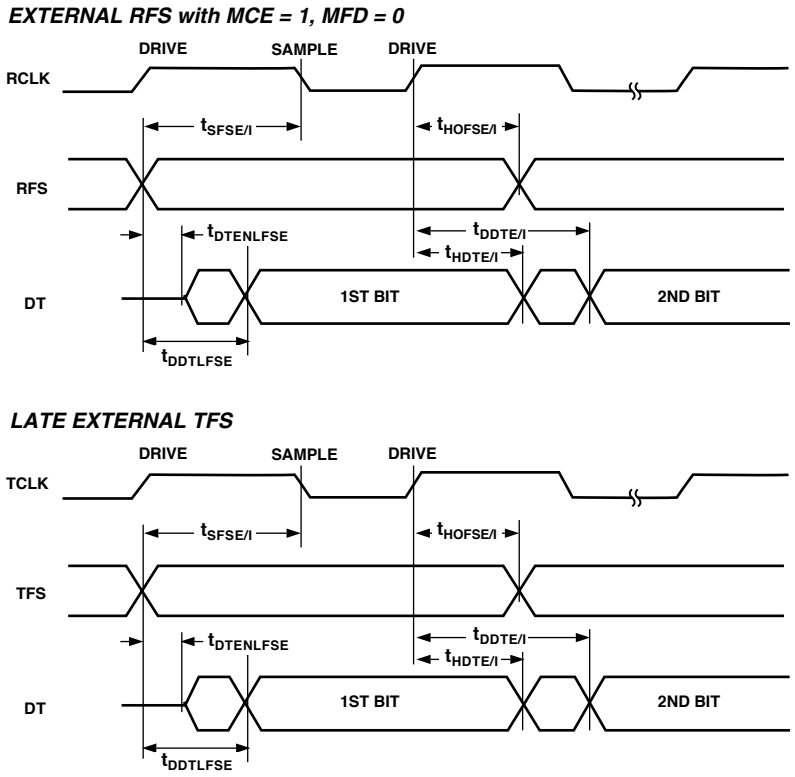


Figure 21. External Late Frame Sync (Frame Sync Setup < $t_{SCLK}/2$)

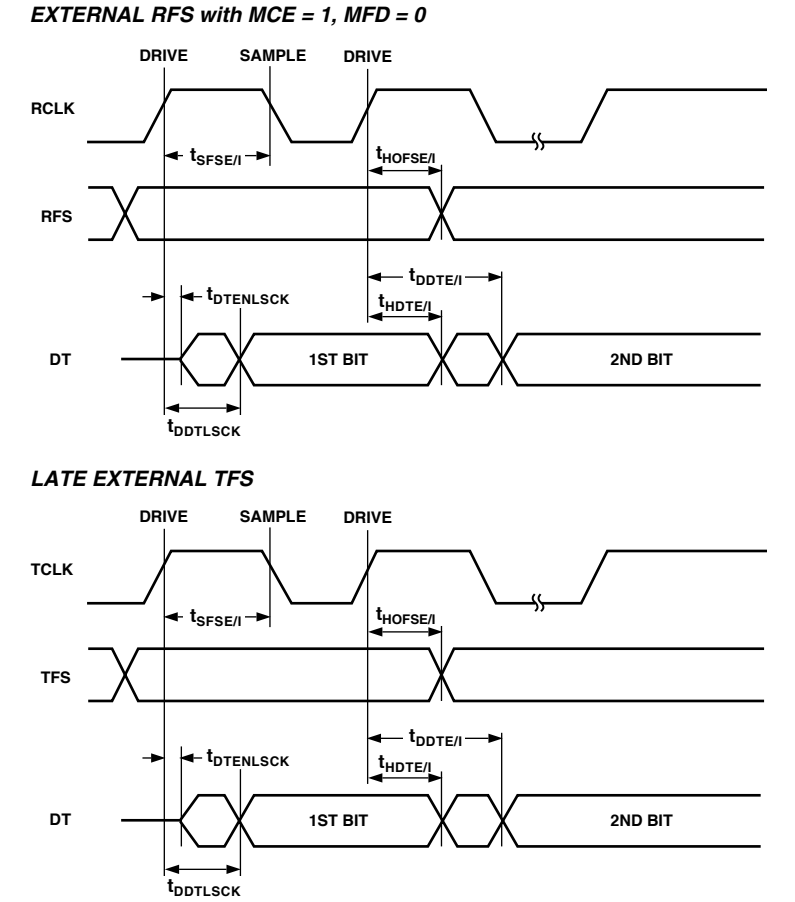


Figure 22. External Late Frame Sync (Frame Sync Setup > $t_{SCLK}/2$)

OUTPUT DRIVE CURRENT

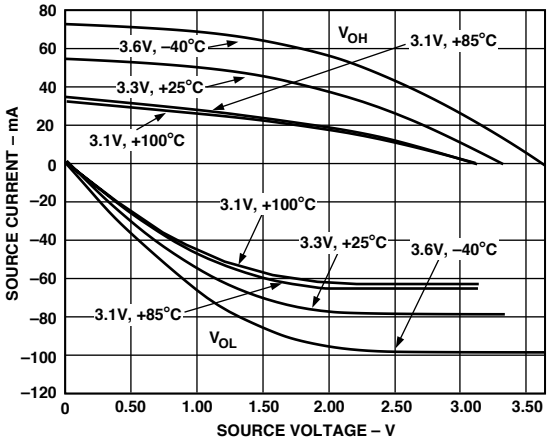


Figure 24. Typical Drive Currents

TEST CONDITIONS

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L and the load current, I_L. This decay time can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times \Delta V}{I_L}$$

The output disable time t_{DIS} is the difference between $t_{MEASURED}$ and t_{DECAY} as shown in Figure 26. The time $t_{MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.5 V.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to when they start driving. The output enable time t_{ENA} is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-21065L's output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (i.e., t_{DATRWH} for the write cycle).

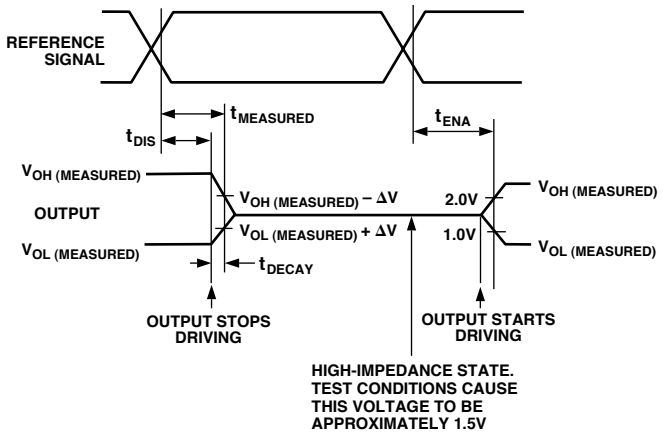


Figure 25. Output Enable

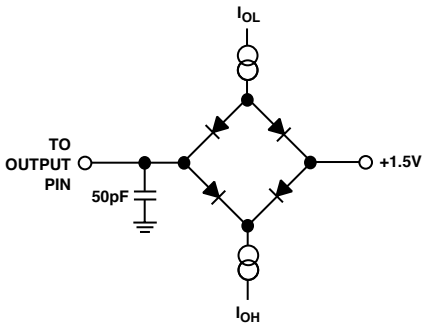


Figure 26. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

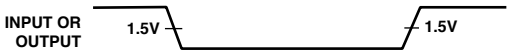


Figure 27. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 50 pF on all pins. The delay and hold specifications given should be derated by a factor of l.8 ns/50 pF for loads other than the nominal value of 50 pF. Figure 28 and Figure 29 show how output rise time varies with capacitance. Figure 30 shows graphically how output delays and hold vary with load capacitance. (Note that this graph or derating does not apply to output disable delays; see the previous section Output Disable time under Test Conditions.) The graphs of Figure 28, Figure 29, and Figure 30 may not be linear outside the ranges shown.

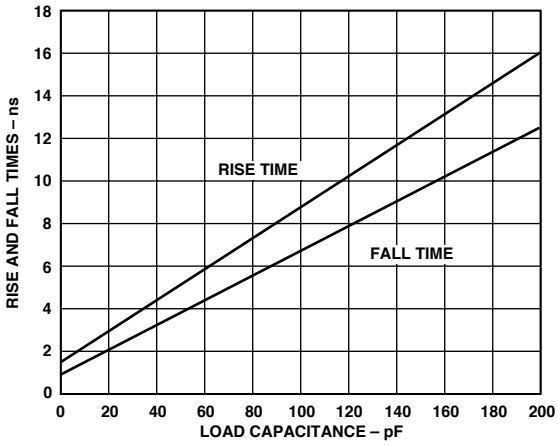


Figure 28. Typical Rise and Fall Time (10%–90% V_{DD})

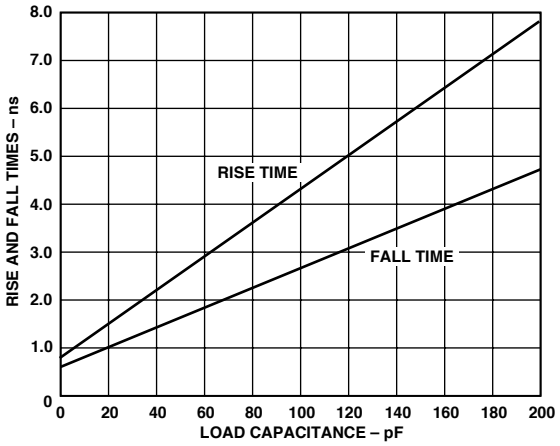


Figure 29. Typical Rise and Fall Time (0.8 V–2.0 V)

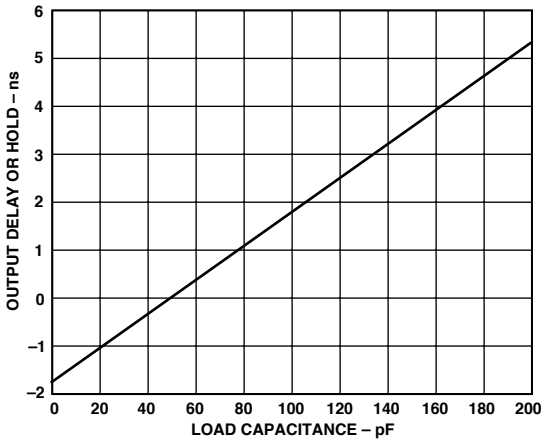
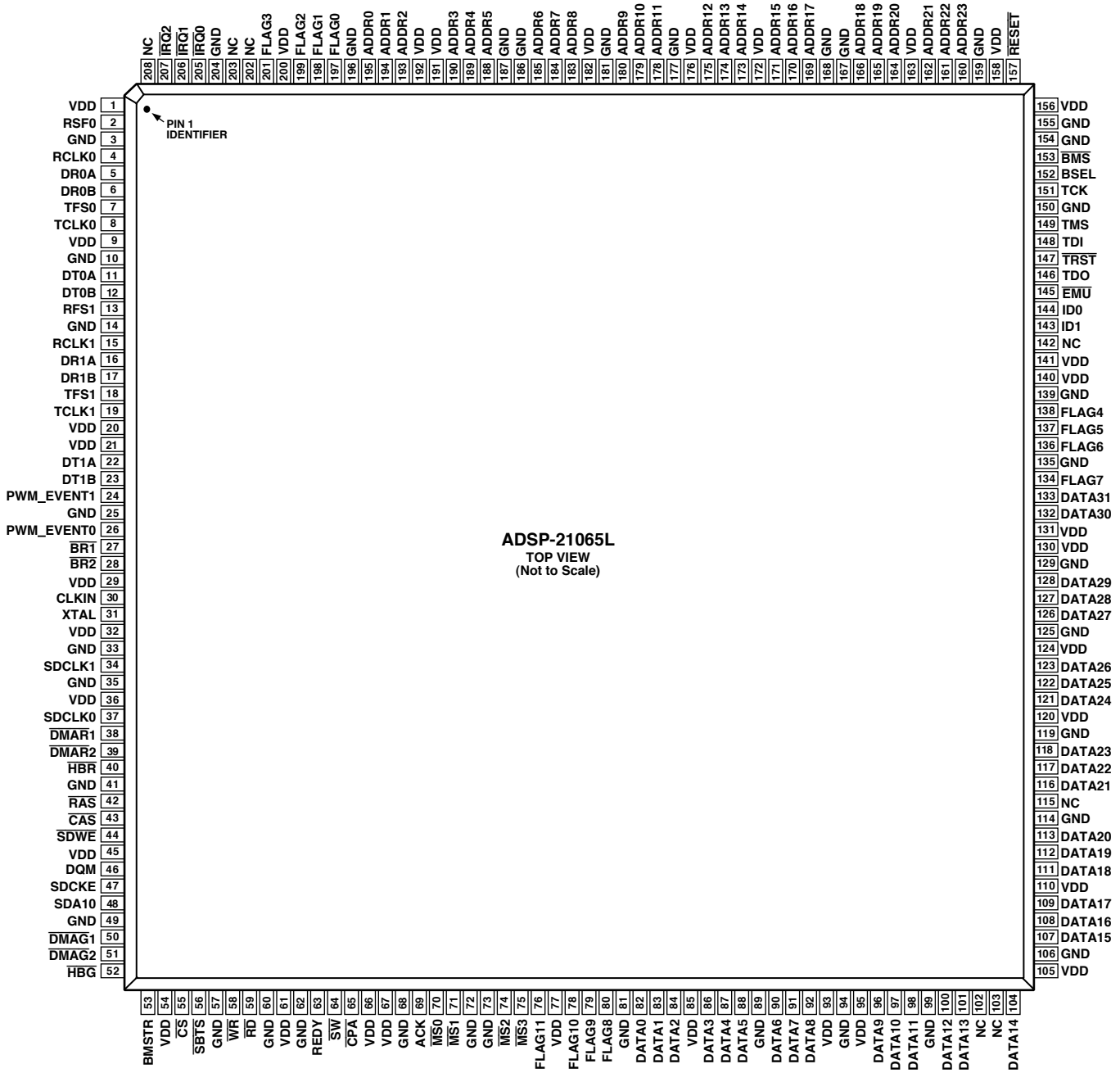


Figure 30. Typical Output Delay or Hold

208-LEAD MQFP PIN

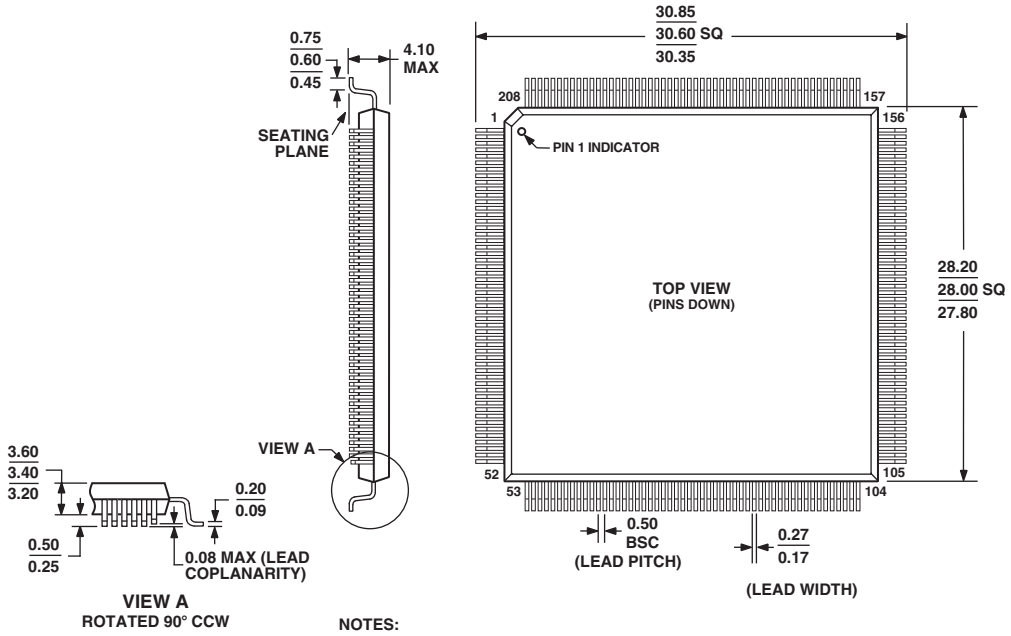


NC = NO CONNECT

OUTLINE DIMENSIONS

208-Lead Metric Quad Flat Package [MQFP]
(S-208-2)

Dimensions shown in millimeters



NOTES:
1. THE ACTUAL POSITION OF EACH LEAD IS WITHIN 0.08 FROM ITS IDEAL POSITION WHEN MEASURED IN THE LATERAL DIRECTION.
2. CENTER DIMENSIONS ARE NOMINAL.
3. DIMENSIONS ARE IN MILLIMETERS AND COMPLY WITH JEDEC STANDARD MS-029, FA-1.

196-BALL MINI-BGA PIN CONFIGURATION

14	13	12	11	10	9	8	7	6	5	4	3	2	1	
NC7	NC8	ADDR18	ADDR17	ADDR14	ADDR11	ADDR8	ADDR7	ADDR6	ADDR3	ADDR0	FLAG2	NC2	NC1	A
TCK	GND	ADDR23	ADDR21	ADDR19	ADDR15	ADDR12	ADDR9	ADDR5	ADDR2	FLAG0	$\overline{\text{IRQ0}}$	RFS0	DR0A	B
TDO	BSEL	$\overline{\text{RESET}}$	ADDR22	ADDR20	ADDR16	ADDR13	ADDR10	ADDR4	ADDR1	FLAG3	$\overline{\text{IRQ2}}$	RCLK0	TCLK0	C
$\overline{\text{EMU}}$	$\overline{\text{TRST}}$	TMS	$\overline{\text{BMS}}$	VDD	VDD	VDD	VDD	VDD	FLAG1	$\overline{\text{IRQ1}}$	DR0B	TFS0	RCLK1	D
FLAG4	ID1	TDI	ID0	VDD	GND	GND	GND	GND	VDD	RFS1	DT0A	DT0B	TFS1	E
FLAG7	FLAG5	FLAG6	VDD	GND	GND	GND	GND	GND	GND	VDD	DR1A	DR1B	TCLK1	F
DATA29	DATA30	DATA31	VDD	GND	GND	GND	GND	GND	GND	VDD	DT1A	DT1B	PWM_ EVENT1	G
DATA26	DATA27	DATA28	VDD	GND	GND	GND	GND	GND	GND	VDD	$\overline{\text{BR2}}$	$\overline{\text{BR1}}$	PWM_ EVENT0	H
DATA23	DATA25	DATA24	VDD	GND	GND	GND	GND	GND	GND	VDD	SDCLK1	XTAL	CLKIN	J
DATA22	DATA20	DATA21	DATA19	VDD	GND	GND	GND	GND	VDD	$\overline{\text{SDWE}}$	$\overline{\text{HBR}}$	SDCLK0	$\overline{\text{DMAR1}}$	K
DATA18	DATA17	DATA16	DATA13	DATA8	VDD	VDD	VDD	VDD	VDD	$\overline{\text{DMAG2}}$	SDA10	$\overline{\text{CAS}}$	$\overline{\text{DMAR2}}$	L
DATA15	DATA14	DATA12	DATA9	DATA5	DATA2	FLAG10	ACK	$\overline{\text{CPA}}$	$\overline{\text{RD}}$	$\overline{\text{CS}}$	$\overline{\text{DMAG1}}$	SDCKE	$\overline{\text{RAS}}$	M
NC6	DATA11	DATA10	DATA7	DATA4	DATA1	FLAG11	$\overline{\text{MS1}}$	GND	REDY	$\overline{\text{SBTS}}$	BMSTR	$\overline{\text{HBG}}$	DQM	N
NC5	DATA6	DATA3	DATA0	FLAG8	FLAG9	$\overline{\text{MS3}}$	$\overline{\text{MS2}}$	$\overline{\text{MS0}}$	$\overline{\text{SW}}$	$\overline{\text{WR}}$	GND	NC4	NC3	P