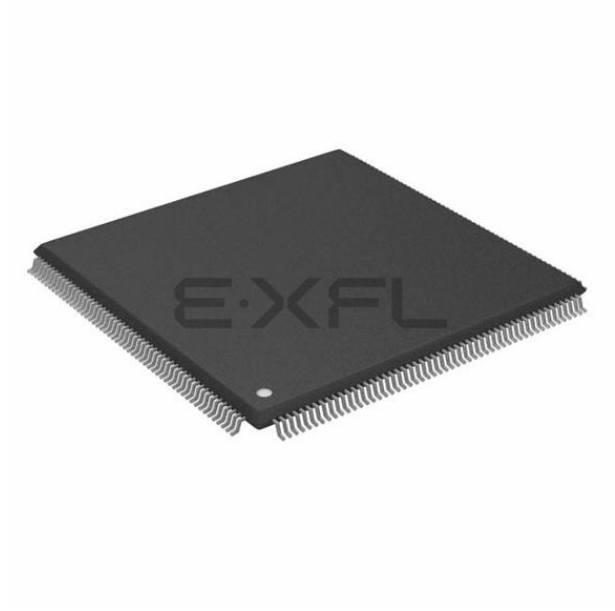

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	Host Interface, Serial Port
Clock Rate	60MHz
Non-Volatile Memory	External
On-Chip RAM	64kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	0°C ~ 85°C (TC)
Mounting Type	Surface Mount
Package / Case	208-BFQFP
Supplier Device Package	208-MQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21065lksz-264

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

GENERAL DESCRIPTION

The ADSP-21065L is a powerful member of the SHARC family of 32-bit processors optimized for cost sensitive applications. The SHARC—Super Harvard Architecture—offers the highest levels of performance and memory integration of any 32-bit DSP in the industry—they are also the only DSP in the industry that offer both fixed and floating-point capabilities, without compromising precision or performance.

The ADSP-21065L is fabricated in a high speed, low power CMOS process, 0.35 µm technology. With its on-chip instruction cache, the processor can execute every instruction in a single cycle. Table I lists the performance benchmarks for the ADSP-21065L.

The ADSP-21065L SHARC combines a floating-point DSP core with integrated, on-chip system features, including a 544 Kbit SRAM memory, host processor interface, DMA controller, SDRAM controller, and enhanced serial ports.

Figure 1 shows a block diagram of the ADSP-21065L, illustrating the following architectural features:

- Computation Units (ALU, Multiplier, and Shifter) with a Shared Data Register File
- Data Address Generators (DAG1, DAG2)
- Program Sequencer with Instruction Cache
- Timers with Event Capture Modes
- On-Chip, dual-ported SRAM
- External Port for Interfacing to Off-Chip Memory and Peripherals
- Host Port and SDRAM Interface
- DMA Controller
- Enhanced Serial Ports
- JTAG Test Access Port

Table I. Performance Benchmarks

Benchmark	Timing	Cycles
Cycle Time	15.00 ns	1
1024-Pt. Complex FFT (Radix 4, with Digit Reverse)	0.274 ns	18221
Matrix Multiply (Pipelined)		
$[3 \times 3] \times [3 \times 1]$	135 ns	9
$[4 \times 4] \times [4 \times 1]$	240 ns	16
FIR Filter (per Tap)	15 ns	1
IIR Filter (per Biquad)	60 ns	4
Divide Y/X	90 ns	6
Inverse Square Root ($1/\sqrt{x}$)	135 ns	9
DMA Transfers	264 Mbytes/sec.	

ADSP-21000 FAMILY CORE ARCHITECTURE

The ADSP-21065L is code and function compatible with the ADSP-21060/ADSP-21061/ADSP-21062. The ADSP-21065L includes the following architectural features of the SHARC family core.

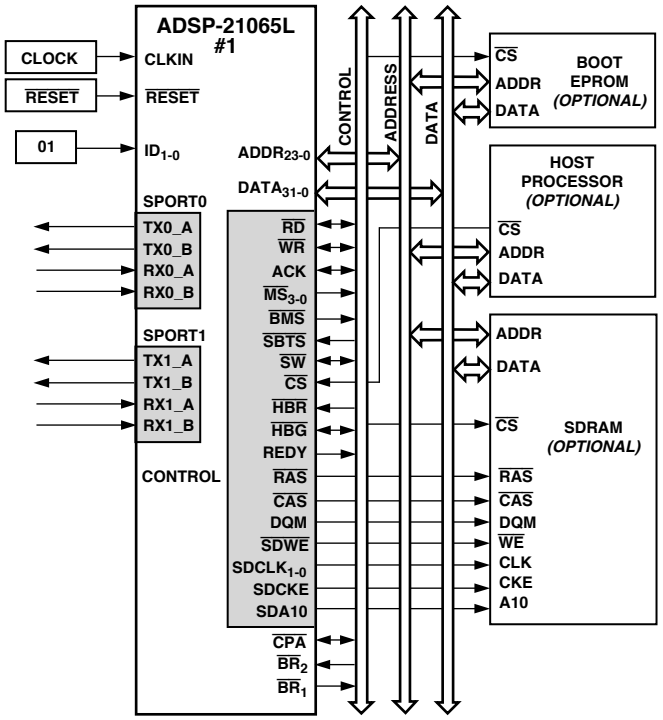


Figure 2. ADSP-21065L Single-Processor System

Independent, Parallel Computation Units
The arithmetic/logic unit (ALU), multiplier, and shifter all perform single-cycle instructions. The three units are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. These computation units support IEEE 32-bit single-precision floating-point, extended precision 40-bit floating-point, and 32-bit fixed-point data formats.

Data Register File
A general-purpose data register file is used for transferring data between the computation units and the data buses, and for storing intermediate results. This 10-port, 32-register (16 primary, 16 secondary) register file, combined with the ADSP-21000 Harvard architecture, allows unconstrained data flow between computation units and internal memory.

Single-Cycle Fetch of Instruction and Two Operands
The ADSP-21065L features an enhanced Super Harvard Architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (see Figure 1). With its separate program and data memory buses, and on-chip instruction cache, the processor can simultaneously fetch two operands and an instruction (from the cache), all in a single cycle.

Instruction Cache
The ADSP-21065L includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and two data values. The cache is selective—only the instructions that fetches conflict with PM bus data accesses are cached. This allows full-speed execution of core, looped operations such as digital filter multiply-accumulates and FFT butterfly processing.

Data Address Generators with Hardware Circular Buffers
The ADSP-21065L's two data address generators (DAGs) implement circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data

structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The ADSP-21065L's two DAGs contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reducing overhead, increasing performance, and simplifying implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set
The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the ADSP-21065L can conditionally execute a multiply, an add, a subtract and a branch, all in a single instruction.

ADSP-21065L FEATURES

The ADSP-21065L is designed to achieve the highest system throughput to enable maximum system performance. It can be clocked by either a crystal or a TTL-compatible clock signal. The ADSP-21065L uses an input clock with a frequency equal to half the instruction rate—a 33 MHz input clock yields a 15 ns processor cycle (which is equivalent to 66 MHz). Interfaces on the ADSP-21065L operate as shown below. Hereafter in this document, 1x = input clock frequency, and 2x = processor's instruction rate.

The following clock operation ratings are based on 1x = 33 MHz (instruction rate/core = 66 MHz):

SDRAM	66 MHz
External SRAM	33 MHz
Serial Ports	33 MHz
Multiprocessing	33 MHz
Host (Asynchronous)	33 MHz

Augmenting the ADSP-21000 family core, the ADSP-21065L adds the following architectural features:

Dual-Ported On-Chip Memory
The ADSP-21065L contains 544 Kbits of on-chip SRAM, organized into two banks: Bank 0 has 288 Kbits, and Bank 1 has 256 Kbits. Bank 0 is configured with 9 columns of 2K × 16 bits, and Bank 1 is configured with 8 columns of 2K × 16 bits. Each memory block is dual-ported for single-cycle, independent accesses by the core processor and I/O processor or DMA controller. The dual-ported memory and separate on-chip buses allow two data transfers from the core and one from I/O, all in a single cycle (see Figure 4 for the ADSP-21065L Memory Map).

On the ADSP-21065L, the memory can be configured as a maximum of 16K words of 32-bit data, 34K words for 16-bit data, 10K words of 48-bit instructions (and 40-bit data) or combinations of different word sizes up to 544 Kbits. All the memory can be accessed as 16-bit, 32-bit or 48-bit.

While each memory block can store combinations of code and data, accesses are most efficient when one block stores data, using the DM bus for transfers, and the other block stores instructions and data, using the PM bus for transfers. Using the DM and PM busses in this way, with one dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache. Single-cycle execution is also maintained when one of the data operands is transferred to or from off-chip, via the ADSP-21065L's external port.

Off-Chip Memory and Peripherals Interface
The ADSP-21065L's external port provides the processor's interface to off-chip memory and peripherals. The 64M words, off-chip address space is included in the ADSP-21065L's unified address space. The separate on-chip buses—for program memory, data memory and I/O—are multiplexed at the external port to create an external system bus with a single 24-bit address bus, four memory selects, and a single 32-bit data bus. The on-chip Super Harvard Architecture provides three bus performance, while the off-chip unified address space gives flexibility to the designer.

SDRAM Interface
The SDRAM interface enables the ADSP-21065L to transfer data to and from synchronous DRAM (SDRAM) at 2x clock frequency. The synchronous approach coupled with 2x clock frequency supports data transfer at a high throughput—up to 220 Mbytes/sec.

The SDRAM interface provides a glueless interface with standard SDRAMs—16 Mb, 64 Mb, and 128 Mb—and includes options to support additional buffers between the ADSP-21065L and SDRAM. The SDRAM interface is extremely flexible and provides capability for connecting SDRAMs to any one of the ADSP-21065L's four external memory banks.

Systems with several SDRAM devices connected in parallel may require buffering to meet overall system timing requirements. The ADSP-21065L supports pipelining of the address and control signals to enable such buffering between itself and multiple SDRAM devices.

Host Processor Interface
The ADSP-21065L's host interface provides easy connection to standard microprocessor buses—8-, 16-, and 32-bit—requiring little additional hardware. Supporting asynchronous transfers at speeds up to 1x clock frequency, the host interface is accessed through the ADSP-21065L's external port. Two channels of DMA are available for the host interface; code and data transfers are accomplished with low software overhead.

The host processor requests the ADSP-21065L's external bus with the host bus request ($\overline{\text{HBR}}$), host bus grant ($\overline{\text{HBG}}$), and ready (REDY) signals. The host can directly read and write the IOP registers of the ADSP-21065L and can access the DMA channel setup and mailbox registers. Vector interrupt support enables efficient execution of host commands.

DMA Controller
The ADSP-21065L's on-chip DMA controller allows zero-overhead, nonintrusive data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions.

DMA transfers can occur between the ADSP-21065L's internal memory and either external memory, external peripherals, or a host processor. DMA transfers can also occur between the ADSP-21065L's internal memory and its serial ports. DMA transfers between external memory and external peripheral devices are another option. External bus packing to 16-, 32-, or 48-bit internal words is performed during DMA transfers.

Ten channels of DMA are available on the ADSP-21065L—eight via the serial ports, and two via the processor's external port (for either host processor, other ADSP-21065L, memory or

PIN DESCRIPTIONS

ADSP-21065L pin definitions are listed below. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$).

Unused inputs should be tied or pulled to VDD or GND, except for $\text{ADDR}_{23\text{-}0}$, $\text{DATA}_{31\text{-}0}$, $\text{FLAG}_{11\text{-}0}$, $\overline{\text{SW}}$, and inputs that have internal pull-up or pull-down resistors ($\overline{\text{CPA}}$, ACK, DTxX, DRxX, TCLKx, RCLKx, TMS, and TDI)—these pins can be left floating. These pins have a logic-level hold circuit that prevents the input from floating internally.

I = Input S = Synchronous P = Power Supply (O/D) = Open Drain
O = Output A = Asynchronous G = Ground (A/D) = Active Drive
T = Three-state (when $\overline{\text{SBTS}}$ is asserted, or when the ADSP-2106x is a bus slave)

Pin	Type	Function
$\text{ADDR}_{23\text{-}0}$	I/O/T	**External Bus Address**. The ADSP-21065L outputs addresses for external memory and peripherals on these pins. In a multiprocessor system the bus master outputs addresses for read/writes of the IOP registers of the other ADSP-21065L. The ADSP-21065L inputs addresses when a host processor or multiprocessing bus master is reading or writing its IOP registers.
$\text{DATA}_{31\text{-}0}$	I/O/T	**External Bus Data**. The ADSP-21065L inputs and outputs data and instructions on these pins. The external data bus transfers 32-bit single-precision floating-point data and 32-bit fixed-point data over bits 31-0. 16-bit short word data is transferred over bits 15-0 of the bus. Pull-up resistors on unused DATA pins are not necessary.
$\overline{\text{MS}}_{3\text{-}0}$	I/O/T	**Memory Select Lines**. These lines are asserted as chip selects for the corresponding banks of external memory. Internal $\text{ADDR}_{25\text{-}24}$ are decoded into $\overline{\text{MS}}_{3\text{-}0}$. The $\overline{\text{MS}}_{3\text{-}0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the $\overline{\text{MS}}_{3\text{-}0}$ lines are inactive; they are active, however, when a conditional memory access instruction is executed, whether or not the condition is true. Additionally, an $\overline{\text{MS}}_{3\text{-}0}$ line which is mapped to SDRAM may be asserted even when no SDRAM access is active. In a multiprocessor system, the $\overline{\text{MS}}_{3\text{-}0}$ lines are output by the bus master.
$\overline{\text{RD}}$	I/O/T	**Memory Read Strobe**. This pin is asserted when the ADSP-21065L reads from external memory devices or from the IOP register of another ADSP-21065L. External devices (including another ADSP-21065L) must assert $\overline{\text{RD}}$ to read from the ADSP-21065L's IOP registers. In a multiprocessor system, $\overline{\text{RD}}$ is output by the bus master and is input by another ADSP-21065L.
$\overline{\text{WR}}$	I/O/T	**Memory Write Strobe.** This pin is asserted when the ADSP-21065L writes to external memory devices or to the IOP register of another ADSP-21065L. External devices must assert $\overline{\text{WR}}$ to write to the ADSP-21065L's IOP registers. In a multiprocessor system, $\overline{\text{WR}}$ is output by the bus master and is input by the other ADSP-21065L.
$\overline{\text{SW}}$	I/O/T	**Synchronous Write Select.** This signal interfaces the ADSP-21065L to synchronous memory devices (including another ADSP-21065L). The ADSP-21065L asserts $\overline{\text{SW}}$ to provide an early indication of an impending write cycle, which can be aborted if $\overline{\text{WR}}$ is not later asserted (e.g., in a conditional write instruction). In a multiprocessor system, $\overline{\text{SW}}$ is output by the bus master and is input by the other ADSP-21065L to determine if the multiprocessor access is a read or write. $\overline{\text{SW}}$ is asserted at the same time as the address output.
ACK	I/O/S	**Memory Acknowledge**. External devices can deassert ACK to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access. The ADSP-21065L deasserts ACK as an output to add wait states to a synchronous access of its IOP registers. In a multiprocessor system, a slave ADSP-21065L deasserts the bus master's ACK input to add wait state(s) to an access of its IOP registers. The bus master has a keeper latch on its ACK pin that maintains the input at the level to which it was last driven.
$\overline{\text{SBTS}}$	I/S	**Suspend Bus Three-State.** External devices can assert $\overline{\text{SBTS}}$ to place the external bus address, data, selects, and strobes—but not SDRAM control pins—in a high impedance state for the following cycle. If the ADSP-21065L attempts to access external memory while $\overline{\text{SBTS}}$ is asserted, the processor will halt and the memory access will not finish until $\overline{\text{SBTS}}$ is deasserted. $\overline{\text{SBTS}}$ should only be used to recover from host processor/ADSP-21065L deadlock.
$\overline{\text{IRQ}}_{2\text{-}0}$	I/A	Interrupt Request Lines. May be either edge-triggered or level-sensitive.
$\text{FLAG}_{11\text{-}0}$	I/O/A	Flag Pins. Each is configured via control bits as either an input or an output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals.

Pin	Type	Function
$\overline{HBR}$	I/A	**Host Bus Request.** Must be asserted by a host processor to request control of the ADSP-21065L's external bus. When $\overline{HBR}$ is asserted in a multiprocessing system, the ADSP-21065L that is bus master will relinquish the bus and assert $\overline{HBG}$. To relinquish the bus, the ADSP-21065L places the address, data, select, and strobe lines in a high impedance state. It does, however, continue to drive the SDRAM control pins. $\overline{HBR}$ has priority over all ADSP-21065L bus requests ($\overline{BR}_{2-1}$) in a multiprocessor system.
$\overline{HBG}$	I/O	**Host Bus Grant**. Acknowledges an $\overline{HBR}$ bus request, indicating that the host processor may take control of the external bus. $\overline{HBG}$ is asserted by the ADSP-21065L until $\overline{HBR}$ is released. In a multiprocessor system, $\overline{HBG}$ is output by the ADSP-21065L bus master.
$\overline{CS}$	I/A	**Chip Select.** Asserted by host processor to select the ADSP-21065L.
REDY (O/D)	O	**Host Bus Acknowledge.** The ADSP-21065L deasserts REDY to add wait states to an asynchronous access of its internal memory or IOP registers by a host. Open drain output (O/D) by default; can be programmed in ADREDY bit of SYSCON register to be active drive (A/D). REDY will only be output if the $\overline{CS}$ and $\overline{HBR}$ inputs are asserted.
$\overline{DMAR}_1$	I/A	**DMA Request 1** (DMA Channel 9).
$\overline{DMAR}_2$	I/A	**DMA Request 2** (DMA Channel 8).
$\overline{DMAG}_1$	O/T	**DMA Grant 1** (DMA Channel 9).
$\overline{DMAG}_2$	O/T	**DMA Grant 2** (DMA Channel 8).
$\overline{BR}_{2-1}$	I/O/S	**Multiprocessing Bus Requests.** Used by multiprocessing ADSP-21065Ls to arbitrate for bus mastership. An ADSP-21065L drives its own $\overline{BR}$x line (corresponding to the value of its ID_{2-0} inputs) only and monitors all others. In a uniprocessor system, tie both $\overline{BR}$x pins to VDD.
ID_{1-0}	I	**Multiprocessing ID.** Determines which multiprocessor bus request ($\overline{BR}_1$–$\overline{BR}_2$) is used by ADSP-21065L. ID = 01 corresponds to $\overline{BR}_1$, ID = 10 corresponds to $\overline{BR}_2$. ID = 00 in single-processor systems. These lines are a system configuration selection which should be hard-wired or changed only at reset.
$\overline{CPA}$ (O/D)	I/O	**Core Priority Access.** Asserting its $\overline{CPA}$ pin allows the core processor of an ADSP-21065L bus slave to interrupt background DMA transfers and gain access to the external bus. $\overline{CPA}$ is an open drain output that is connected to both ADSP-21065Ls in the system. The $\overline{CPA}$ pin has an internal 5 kΩ pull-up resistor. If core access priority is not required in a system, leave the $\overline{CPA}$ pin unconnected.
DTxX	O	**Data Transmit** (Serial Ports 0, 1; Channels A, B). Each DTxX pin has a 50 kΩ internal pull-up resistor.
DRxX	I	**Data Receive** (Serial Ports 0, 1; Channels A, B). Each DRxX pin has a 50 kΩ internal pull-up resistor.
TCLKx	I/O	**Transmit Clock** (Serial Ports 0, 1). Each TCLK pin has a 50 kΩ internal pull-up resistor.
RCLKx	I/O	**Receive Clock** (Serial Ports 0, 1). Each RCLK pin has a 50 kΩ internal pull-up resistor.
TFSx	I/O	**Transmit Frame Sync** (Serial Ports 0, 1).
RFSx	I/O	**Receive Frame Sync** (Serial Ports 0, 1).
BSEL	I	**EPROM Boot Select.** When BSEL is high, the ADSP-21065L is configured for booting from an 8-bit EPROM. When BSEL is low, the BSEL and $\overline{BMS}$ inputs determine booting mode. See $\overline{BMS}$ for details. This signal is a system configuration selection which should be hardwired.

Pin	Type	Function
$\overline{\text{BMS}}$	I/O/T*	**Boot Memory Select.** Output: used as chip select for boot EPROM devices (when BSEL = 1). In a multiprocessor system, $\overline{\text{BMS}}$ is output by the bus master. Input: When low, indicates that no booting will occur and that the ADSP-21065L will begin executing instructions from external memory. See following table. This input is a system configuration selection which should be hardwired. *Three-statable only in EPROM boot mode (when $\overline{\text{BMS}}$ is an output). **BSEL** / **$\overline{\text{BMS}}$** / **Booting Mode** 1 / Output / EPROM (connect $\overline{\text{BMS}}$ to EPROM chip select). 0 / 1 (Input) / Host processor (HBW [SYSCON] bit selects host bus width). 0 / 0 (Input) / No booting. Processor executes from external memory.
CLKIN	I	**Clock In.** Used in conjunction with XTAL, configures the ADSP-21065L to use either its internal clock generator or an external clock source. The external crystal should be rated at 1x frequency. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. The ADSP-21065L's internal clock generator multiplies the 1x clock to generate 2x clock for its core and SDRAM. It drives 2x clock out on the SDCLKx pins for the SDRAM interface to use. See also SDCLKx. Connecting the 1x external clock to CLKIN while leaving XTAL unconnected configures the ADSP-21065L to use the external clock source. The instruction cycle rate is equal to 2x CLKIN. CLKIN may not be halted, changed, or operated below the specified frequency.
$\overline{\text{RESET}}$	I/A	**Processor Reset.** Resets the ADSP-21065L to a known state and begins execution at the program memory location specified by the hardware reset vector address. This input must be asserted at power-up.
TCK	I	**Test Clock (JTAG).** Provides an asynchronous clock for JTAG boundary scan.
TMS	I/S	**Test Mode Select (JTAG).** Used to control the test state machine. TMS has a 20 kΩ internal pull-up resistor.
TDI	I/S	**Test Data Input (JTAG).** Provides serial data for the boundary scan logic. TDI has a 20 kΩ internal pull-up resistor.
TDO	O	**Test Data Output (JTAG).** Serial scan output of the boundary scan path.
$\overline{\text{TRST}}$	I/A	**Test Reset (JTAG).** Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-21065L. $\overline{\text{TRST}}$ has a 20 kΩ internal pull-up resistor.
$\overline{\text{EMU}}$ (O/D)	O	**Emulation Status.** Must be connected to the ADSP-21065L EZ-ICE target board connector only.
BMSTR	O	**Bus Master Output.** In a multiprocessor system, indicates whether the ADSP-21065L is current bus master of the shared external bus. The ADSP-21065L drives BMSTR high only while it is the bus master. In a single-processor system (ID = 00), the processor drives this pin high.
$\overline{\text{CAS}}$	I/O/T	**SDRAM Column Access Strobe.** Provides the column address. In conjunction with $\overline{\text{RAS}}$, $\overline{\text{MS}}$x, $\overline{\text{SDWE}}$, SDCLKx, and sometimes SDA10, defines the operation for the SDRAM to perform.
$\overline{\text{RAS}}$	I/O/T	**SDRAM Row Access Strobe.** Provides the row address. In conjunction with $\overline{\text{CAS}}$, $\overline{\text{MS}}$x, $\overline{\text{SDWE}}$, SDCLKx, and sometimes SDA10, defines the operation for the SDRAM to perform.
$\overline{\text{SDWE}}$	I/O/T	**SDRAM Write Enable.** In conjunction with $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, $\overline{\text{MS}}$x, SDCLKx, and sometimes SDA10, defines the operation for the SDRAM to perform.
DQM	O/T	**SDRAM Data Mask.** In write mode, DQM has a latency of zero and is used to block write operations.
$\text{SDCLK}_{1\text{-}0}$	I/O/S/T	**SDRAM 2x Clock Output.** In systems with multiple SDRAM devices connected in parallel, supports the corresponding increased clock load requirements, eliminating need of off-chip clock buffers. Either SDCLK_1 or both SDCLKx pins can be three-stated.
SDCKE	I/O/T	**SDRAM Clock Enable.** Enables and disables the CLK signal. For details, see the data sheet supplied with your SDRAM device.

ADSP-21065L–SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter		Test Conditions	C Grade Min	C Grade Max	K Grade Min	K Grade Max	Unit
V_{DD}	Supply Voltage		3.13	3.60	3.13	3.60	V
T_{CASE}	Case Operating Temperature		–40	+100	0	+85	°C
V_{IH}	High Level Input Voltage	@ V_{DD} = max	2.0	V_{DD} + 0.5	2.0	V_{DD} + 0.5	V
V_{IL1}	Low Level Input Voltage[1]	@ V_{DD} = min	–0.5	0.8	–0.5	0.8	V
V_{IL2}	Low Level Input Voltage[2]	@ V_{DD} = min	–0.5	0.7	–0.5	0.7	V

NOTE
See Environmental Conditions for information on thermal specifications.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	C and K Grades Min	C and K Grades Max	Unit
V_{OH}	High Level Output Voltage[3]	@ V_{DD} = min, I_{OH} = –2.0 mA[4]	2.4		V
V_{OL}	Low Level Output Voltage[3]	@ V_{DD} = min, I_{OL} = 4.0 mA[4]		0.4	V
I_{IH}	High Level Input Current[5]	@ V_{DD} = max, V_{IN} = V_{DD} max		10	µA
I_{IL}	Low Level Input Current[5]	@ V_{DD} = max, V_{IN} = 0 V		10	µA
I_{ILP}	Low Level Input Current[6]	@ V_{DD} = max, V_{IN} = 0 V		150	µA
I_{OZH}	Three-State Leakage Current[7, 8, 9, 10]	@ V_{DD} = max, V_{IN} = V_{DD} max		10	µA
I_{OZL}	Three-State Leakage Current[7]	@ V_{DD} = max, V_{IN} = 0 V		8	µA
I_{OZLS}	Three-State Leakage Current[8]	@ V_{DD} = max, V_{IN} = 0 V		150	µA
I_{OZLA}	Three-State Leakage Current[11]	@ V_{DD} = max, V_{IN} = 1.5 V		350	µA
I_{OZLAR}	Three-State Leakage Current[10]	@ V_{DD} = max, V_{IN} = 0 V		4	mA
I_{OZLC}	Three-State Leakage Current[9]	@ V_{DD} = max, V_{IN} = 0 V		1.5	mA
C_{IN}	Input Capacitance[12, 13]	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		8	pF

NOTES
[1] Applies to input and bidirectional pins: $DATA_{31-0}$, $ADDR_{23-0}$, BSEL, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $\overline{SBTS}$, $\overline{IRQ}_{2-0}$, $FLAG_{11-0}$, $\overline{HBG}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR}_{2-1}$, $\overline{ID}_{2-0}$, RPBA, $\overline{CPA}$, TFS0, TFS1, RFS0, RFS1, $\overline{BMS}$, TMS, TDI, TCK, $\overline{HBR}$, DR0A, DR1A, DR0B, DR1B, TCLK0, TCLK1, RCLK0, RCLK1, $\overline{RESET}$, $\overline{TRST}$, PWM_EVENT0, PWM_EVENT1, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, $\overline{SDCKE}$.
[2] Applies to input pin CLKIN.
[3] Applies to output and bidirectional pins: $DATA_{31-0}$, $ADDR_{23-0}$, MS_{3-0}, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $FLAG_{11-0}$, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR}_{2-1}$, $\overline{CPA}$, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, DT0A, DT1A, DT0B, DT1B, XTAL, $\overline{BMS}$, TDO, $\overline{EMU}$, BMSTR, PWM_EVENT0, PWM_EVENT1, $\overline{RAS}$, $\overline{CAS}$, DQM, $\overline{SDWE}$, SDCLK0, SDCLK1, $\overline{SDCKE}$, SDA10.
[4] See Output Drive Currents for typical drive current capabilities.
[5] Applies to input pins: ACK, $\overline{SBTS}$, $\overline{IRQ}_{2-0}$, $\overline{HBR}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, ID_{1-0}, BSEL, CLKIN, $\overline{RESET}$, TCK (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID_{1-0} = 01 and another ADSP-21065L is not requesting bus mastership.)
[6] Applies to input pins with internal pull-ups: DR0A, DR1A, DR0B, DR1B, $\overline{TRST}$, TMS, TDI.
[7] Applies to three-statable pins: $DATA_{31-0}$, $ADDR_{23-0}$, $\overline{MS}_{3-0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $FLAG_{11-0}$, REDY, $\overline{HBG}$, $\overline{DMAG}_1$, $\overline{DMAG}_2$, $\overline{BMS}$, TDO, $\overline{RAS}$, $\overline{CAS}$, DQM, $\overline{SDWE}$, SDCLK0, SDCLK1, $\overline{SDCKE}$, SDA10, and $\overline{EMU}$ (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID_{1-0} = 01 and another ADSP-21065L is not requesting bus mastership).
[8] Applies to three-statable pins with internal pull-ups: DT0A, DT1A, DT0B, DT1B, TCLK0, TCLK1, RCLK0, RCLK1.
[9] Applies to $\overline{CPA}$ pin.
[10] Applies to ACK pin when pulled up.
[11] Applies to ACK pin when keeper latch enabled.
[12] Guaranteed but not tested.
[13] Applies to all signal pins.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . –0.3 V to +4.6 V
Input Voltage . . . . . –0.5 V to V_{DD} + 0.5 V
Output Voltage Swing . . . . . –0.5 V to V_{DD} + 0.5 V
Load Capacitance . . . . . 200 pF
Junction Temperature Under Bias . . . . . 130°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (5 seconds) . . . . . 280°C

*Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADSP-21065L features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

POWER DISSIPATION ADSP-21065L

These specifications apply to the internal power portion of V_{DD} only. See the Power Dissipation section of this data sheet for calculation of external supply current and total supply current. For a complete discussion of the code used to measure power dissipation, see the technical note SHARC Power Dissipation Measurements.

Specifications are based on the following operating scenarios:

Table II. Internal Current Measurements

Operation	Peak Activity ($I_{DDINPEAK}$)	High Activity ($I_{DDINHIGH}$)	Low Activity ($I_{DDINLOW}$)
Instruction Type	Multifunction	Multifunction	Single Function
Instruction Fetch	Cache	Internal Memory	Internal Memory
Core Memory Access	2 per Cycle (DM and PM)	1 per Cycle (DM)	None
Internal Memory DMA	1 per Cycle	1 per 2 Cycles	1 per 2 Cycles

To estimate power consumption for a specific application, use the following equation where % is the amount of time your program spends in that state:

$\%PEAK \times I_{DDINPEAK} + \%HIGH \times I_{DDINHIGH} + \%LOW \times I_{DDINLOW} + \%IDLE \times I_{DDIDLE} = POWER\ CONSUMPTION$
(See note 4 below Table III.)

OR $\%PEAK \times I_{DDINPEAK} + \%HIGH \times I_{DDINHIGH} + \%LOW \times I_{DDINLOW} + \%IDLE16 \times I_{DDIDLE16} = POWER\ CONSUMPTION$
(See note 5 below Table III.)

Table III. Internal Current Measurement Scenarios

Parameter		Test Conditions	Max	Unit
$I_{DDINPEAK}$	Supply Current (Internal)[1]	t_{CK} = 33 ns, V_{DD} = max	470	mA
		t_{CK} = 30 ns, V_{DD} = max	510	mA
$I_{DDINHIGH}$	Supply Current (Internal)[2]	t_{CK} = 33 ns, V_{DD} = max	275	mA
		t_{CK} = 30 ns, V_{DD} = max	300	mA
$I_{DDINLOW}$	Supply Current (Internal)[3]	t_{CK} = 33 ns, V_{DD} = max	240	mA
		t_{CK} = 30 ns, V_{DD} = max	260	mA
I_{DDIDLE}	Supply Current (IDLE)[4]	t_{CK} = 33 ns, V_{DD} = max	150	mA
		t_{CK} = 30 ns, V_{DD} = max	155	mA
$I_{DDIDLE16}$	Supply Current (IDLE16)[5]	V_{DD} = max	50	mA

NOTES
[1]The test program used to measure $I_{DDINPEAK}$ represents worst-case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified.
[2]$I_{DDINHIGH}$ is a composite average based on a range of high activity code.
[3]$I_{DDINLOW}$ is a composite average based on a range of low activity code.
[4]IDLE denotes ADSP-21065L state during execution of IDLE instruction.
[5]IDLE16 denotes ADSP-21065L state during execution of IDLE16 instruction.

TIMING SPECIFICATIONS

General Notes

Two speed grades of the ADSP-21065L are offered, 60 MHz and 66 MHz instruction rates. The specifications shown are based on a CLKIN frequency of 30 MHz (t_{CK} = 33.3 ns). The DT derating allows specifications at other CLKIN frequencies (within the min–max range of the t_{CK} specification; see Clock Input below). DT is the difference between the actual CLKIN period and a CLKIN period of 33.3 ns:

$$DT = (t_{CK} - 33.3)/32$$

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add parameters to derive longer times.

See Figure 27 in Equivalent Device Loading for AC Measurements (Includes All Fixtures) for voltage reference levels.

Switching Characteristics specify how the processor changes its signals. You have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell you what the processor will do in a given circumstance. You can also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing Requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

(O/D) = Open Drain
(A/D) = Active Drive

Parameter		66 MHz Min	66 MHz Max	60 MHz Min	60 MHz Max	Unit
Clock Input						
Timing Requirements:						
t_{CK}	CLKIN Period	30.00	100	33.33	100	ns
t_{CKL}	CLKIN Width Low	7.0		7.0		ns
t_{CKH}	CLKIN Width High	5.0		5.0		ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V–2.0 V)		3.0		3.0	ns

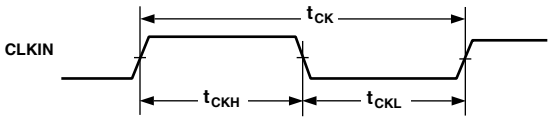


Figure 7. Clock Input

Parameter		Min	Max	Unit
Reset				
Timing Requirements:				
t_{WRST}	$\overline{\text{RESET}}$ Pulsewidth Low[1]	2 t_{CK}		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN High[2]	23.5 + 24 DT	t_{CK}	ns

NOTES
[1]Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 3000 CLKIN cycles while $\overline{\text{RESET}}$ is low, assuming stable V_{DD} and CLKIN (not including start-up time of external clock oscillator).
[2]Only required if multiple ADSP-2106xs must come out of reset synchronous to CLKIN with program counters (PC) equal (i.e., for a SIMD system). Not required for multiple ADSP-2106xs communicating over the shared bus (through the external port), because the bus arbitration logic synchronizes itself automatically after reset.

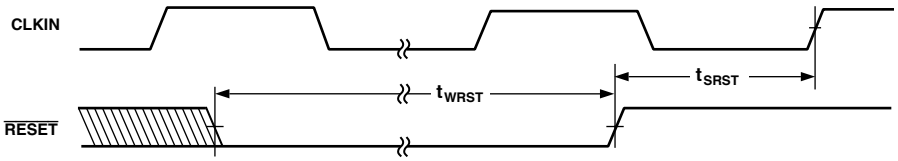


Figure 8. Reset

Parameter		Min	Max	Unit
Interrupts				
Timing Requirements:				
t_{SIR}	$\overline{\text{IRQ}}$2-0 Setup Before CLKIN High or Low[1]	11.0 + 12 DT		ns
t_{HIR}	$\overline{\text{IRQ}}$2-0 Hold Before CLKIN High or Low[1]		0.0 + 12 DT	ns
t_{IPW}	$\overline{\text{IRQ}}$2-0 Pulsewidth[2]	2.0 + t_{CK}/2		ns

NOTES
[1]Only required for $\overline{\text{IRQ}}$x recognition in the following cycle.
[2]Applies only if t_{SIR} and t_{HIR} requirements are not met.

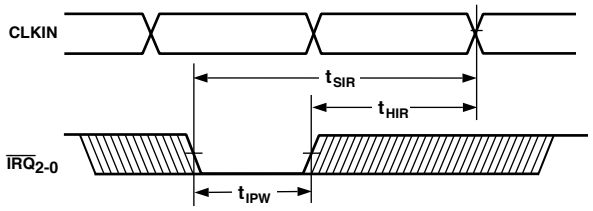


Figure 9. Interrupts

Parameter		Min	Max	Unit
Timer				
Timing Requirements:				
t_{STI}	Timer Setup Before SDCLK High	0.0		ns
t_{HTI}	Timer Hold After SDCLK High	6.0		ns
Switching Characteristics:				
t_{DTEX}	Timer Delay After SDCLK High		1.0	ns
t_{HTEX}	Timer Hold After SDCLK High	–5.0		ns

Parameter		Min	Max	Unit
Flags				
Timing Requirements:				
t_{SFI}	$FLAG_{11-0}$IN Setup Before SDCLK High[1]	–2.0		ns
t_{HFI}	$FLAG_{11-0}$IN Hold After SDCLK High[1]	6.0		ns
Switching Characteristics:				
t_{DFO}	$FLAG_{11-0}$OUT Delay After SDCLK High		1.0	ns
t_{HFO}	$FLAG_{11-0}$OUT Hold After SDCLK High	–4.0		ns
t_{DFOE}	SDCLK High to $FLAG_{11-0}$OUT Enable	–4.0		ns
t_{DFOD}	SDCLK High to $FLAG_{11-0}$OUT Disable		–1.75	ns

NOTE
[1]Flag inputs meeting these setup and hold times will affect conditional instructions in the following instruction cycle.

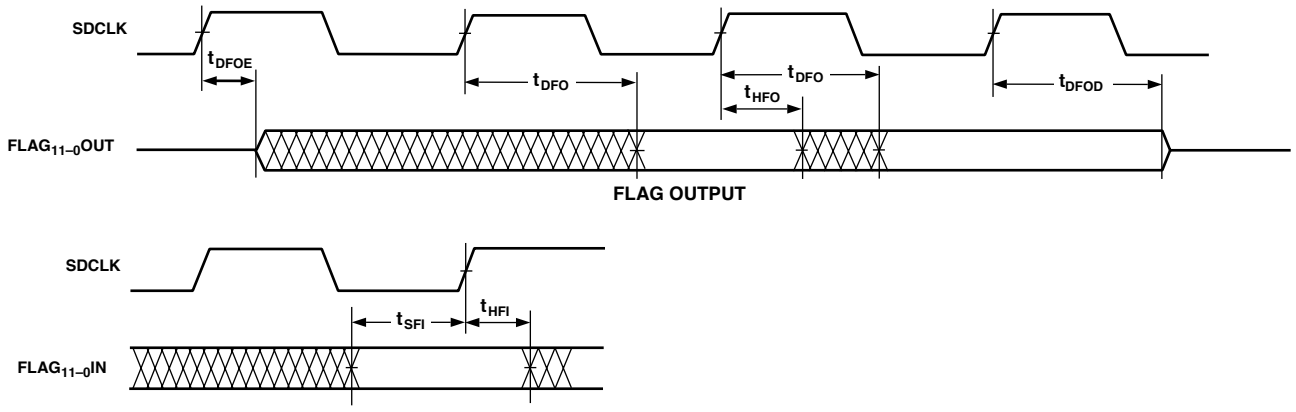


Figure 10. Flags

Synchronous Read/Write—Bus Slave

Use these specifications for ADSP-21065L bus master accesses of a slave's IOP registers or internal memory (in multiprocessor memory space). The bus master must meet these (bus slave) timing requirements.

Parameter		Min	Max	Unit
Timing Requirements:				
t_{SADRI}	Address, $\overline{SW}$ Setup Before CLKIN	24.5 + 25 DT		ns
t_{HADRI}	Address, $\overline{SW}$ Hold Before CLKIN		4.0 + 8 DT	ns
t_{SRWLI}	$\overline{RD}/\overline{WR}$ Low Setup Before CLKIN[1]	21.0 + 21 DT		ns
t_{HRWLI}	$\overline{RD}/\overline{WR}$ Low Hold After CLKIN	–2.50 – 5 DT	7.5 + 7 DT	ns
t_{RWHPI}	$\overline{RD}/\overline{WR}$ Pulse High	2.5		ns
t_{SDATWH}	Data Setup Before $\overline{WR}$ High	4.5		ns
t_{HDATWH}	Data Hold After $\overline{WR}$ High	0.0		ns
Switching Characteristics:				
t_{SDDATO}	Data Delay After CLKIN		31.75 + 21 DT	ns
t_{DATTR}	Data Disable After CLKIN[2]	1.0 – 2 DT	7.0 – 2 DT	ns
t_{DACK}	ACK Delay After CLKIN		29.5 + 20 DT	ns
t_{ACKTR}	ACK Disable After CLKIN[2]	1.0 – 2 DT	6.0 – 2 DT	ns

NOTES

[1]t_{SRWLI} is specified when Multiprocessor Memory Space Wait State (MMSWS bit in WAIT register) is disabled; when MMSWS is enabled, t_{SRWLI} (min) = 17.5 + 18 DT.

[2]See System Hold Time Calculation under Test Conditions for calculation of hold times given capacitive and dc loads.

For two ADSP-21065Ls to communicate synchronously as master and slave, certain master and slave specification combinations must be satisfied. Do not compare specification values directly to calculate master/slave clock skew margins for those specifications listed below. The following table shows the appropriate clock skew margin.

Table IV. Bus Master to Slave Skew Margins

Master Specification	Slave Specification	Skew Margin	
t_{SSDATI}	t_{SDDATO}	t_{CK} = 33.3 ns	+ 2.25 ns
		t_{CK} = 30.0 ns	+ 1.50 ns
t_{SACKC}	t_{DACK}	t_{CK} = 33.3 ns	+ 3.00 ns
		t_{CK} = 30.0 ns	+ 2.25 ns
t_{DADRO}	t_{SADRI}	t_{CK} = 33.3 ns	N/A
		t_{CK} = 30.0 ns	+ 2.75 ns
t_{DRWL} (Max)	t_{SRWLI}	t_{CK} = 33.3 ns	+ 1.50 ns
		t_{CK} = 30.0 ns	+ 1.25 ns
t_{DRDO} (Max)	t_{HRWLI} (Max)	t_{CK} = 33.3 ns	N/A
		t_{CK} = 30.0 ns	3.00 ns
t_{DWRO} (Max)	t_{HRWLI} (Max)	t_{CK} = 33.3 ns	N/A
		t_{CK} = 30.0 ns	3.75 ns

Multiprocessor Bus Request and Host Bus Request

Use these specifications for passing of bus mastership between multiprocessing ADSP-21065Ls ($\overline{BR}$x) or a host processor ($\overline{HBR}$, $\overline{HBG}$).

Parameter		Min	Max	Unit
Timing Requirements:				
$t_{HBGRCSV}$	$\overline{HBG}$ Low to $\overline{RD}$/$\overline{WR}$/$\overline{CS}$ Valid[1]		20.0 + 36 DT	ns
t_{SHBRI}	$\overline{HBR}$ Setup Before CLKIN[2]	12.0 + 12 DT		ns
t_{HHBRI}	$\overline{HBR}$ Hold Before CLKIN[2]		6.0 + 12 DT	ns
t_{SHBGI}	$\overline{HBG}$ Setup Before CLKIN	6.0 + 8 DT		ns
t_{HHBGI}	$\overline{HBG}$ Hold Before CLKIN High		1.0 + 8 DT	ns
t_{SBRI}	$\overline{BR}$x, $\overline{CPA}$ Setup Before CLKIN[3]	7.0 + 8 DT		ns
t_{HBRI}	$\overline{BR}$x, $\overline{CPA}$ Hold Before CLKIN High		1.0 + 8 DT	ns
Switching Characteristics:				
t_{DHBGO}	$\overline{HBG}$ Delay After CLKIN		8.0 – 2 DT	ns
t_{HHBGO}	$\overline{HBG}$ Hold After CLKIN	1.0 – 2 DT		ns
t_{DBRO}	$\overline{BR}$x Delay After CLKIN		7.0 – 2 DT	ns
t_{HBRO}	$\overline{BR}$x Hold After CLKIN	1.0 – 2 DT		ns
t_{DCPAO}	$\overline{CPA}$ Low Delay After CLKIN		11.5 – 2 DT	ns
t_{TRCPA}	$\overline{CPA}$ Disable After CLKIN	1.0 – 2 DT	5.5 – 2 DT	ns
t_{DRDYCS}	REDY (O/D) or (A/D) Low from $\overline{CS}$ and $\overline{HBR}$ Low[4]		13.0	ns
t_{TRDYHG}	REDY (O/D) Disable or REDY (A/D) High from $\overline{HBG}$[4]	44.0 + 43 DT		ns
t_{ARDYTR}	REDY (A/D) Disable from $\overline{CS}$ or $\overline{HBR}$ High[4]		10.0	ns

NOTES

[1]For first asynchronous access after $\overline{HBR}$ and $\overline{CS}$ asserted, $ADDR_{23-0}$ must be a nonMMS value 1/2 t_{CK} before $\overline{RD}$ or $\overline{WR}$ goes low or by $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. This is easily accomplished by driving an upper address signal high when $\overline{HBG}$ is asserted. See the Host Processor Control of the ADSP-21065L section of the *ADSP-21065L SHARC User's Manual*, Second Edition.

[2]Only required for recognition in the current cycle.

[3]$\overline{CPA}$ assertion must meet the setup to CLKIN; deassertion does not need to meet the setup to CLKIN.

[4](O/D) = open drain, (A/D) = active drive.

Asynchronous Read/Write—Host to ADSP-21065L

Use these specifications for asynchronous host processor accesses of an ADSP-21065L, after the host has asserted $\overline{CS}$ and $\overline{HBR}$ (low). After the ADSP-21065L returns $\overline{HBG}$, the host can drive the $\overline{RD}$ and $\overline{WR}$ pins to access the ADSP-21065L's IOP registers. $\overline{HBR}$ and $\overline{HBG}$ are assumed low for this timing. Writes can occur at a minimum interval of (1/2) t_{CK}.

Parameter		Min	Max	Unit
Read Cycle				
Timing Requirements:				
t_{SADRDL}	Address Setup/$\overline{CS}$ Low Before $\overline{RD}$ Low*	0.0		ns
t_{HADRDH}	Address Hold/$\overline{CS}$ Hold Low After $\overline{RD}$ High	0.0		ns
t_{WRWH}	$\overline{RD}$/$\overline{WR}$ High Width	6.0		ns
$t_{DRDHRDY}$	$\overline{RD}$ High Delay After REDY (O/D) Disable	0.0		ns
$t_{DRDHRDY}$	$\overline{RD}$ High Delay After REDY (A/D) Disable	0.0		ns
Switching Characteristics:				
$t_{SDATRDY}$	Data Valid Before REDY Disable from Low	1.5		ns
$t_{DRDYRDL}$	REDY (O/D) or (A/D) Low Delay After $\overline{RD}$ Low		13.5	ns
t_{RDYPRD}	REDY (O/D) or (A/D) Low Pulsewidth for Read	28.0 + DT		ns
t_{HDARWH}	Data Disable After $\overline{RD}$ High	2.0	10.0	ns
Write Cycle				
Timing Requirements:				
t_{SCSWRL}	$\overline{CS}$ Low Setup Before $\overline{WR}$ Low	0.0		ns
t_{HCSWRH}	$\overline{CS}$ Low Hold After $\overline{WR}$ High	0.0		ns
t_{SADWRH}	Address Setup Before $\overline{WR}$ High	5.0		ns
t_{HADWRH}	Address Hold After $\overline{WR}$ High	2.0		ns
t_{WWRL}	$\overline{WR}$ Low Width	7.0		ns
t_{WRWH}	$\overline{RD}$/$\overline{WR}$ High Width	6.0		ns
$t_{DWRHRDY}$	$\overline{WR}$ High Delay After REDY (O/D) or (A/D) Disable	0.0		ns
t_{SDATWH}	Data Setup Before $\overline{WR}$ High	5.0		ns
t_{HDATWH}	Data Hold After $\overline{WR}$ High	1.0		ns
Switching Characteristics:				
$t_{DRDYWRL}$	REDY (O/D) or (A/D) Low Delay After $\overline{WR}$/$\overline{CS}$ Low		13.5	ns
t_{RDYPWR}	REDY (O/D) or (A/D) Low Pulsewidth for Write	7.75		ns

NOTE

*Not required if $\overline{RD}$ and address are valid $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. For first access after $\overline{HBR}$ asserted, ADDR23-0 must be a nonMMS value 1/2 t_{CLK} before $\overline{RD}$ or $\overline{WR}$ goes low or by $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. This is easily accomplished by driving an upper address signal high when $\overline{HBG}$ is asserted. See Host Interface, in the *ADSP-21065L SHARC User's Manual*, Second Edition.

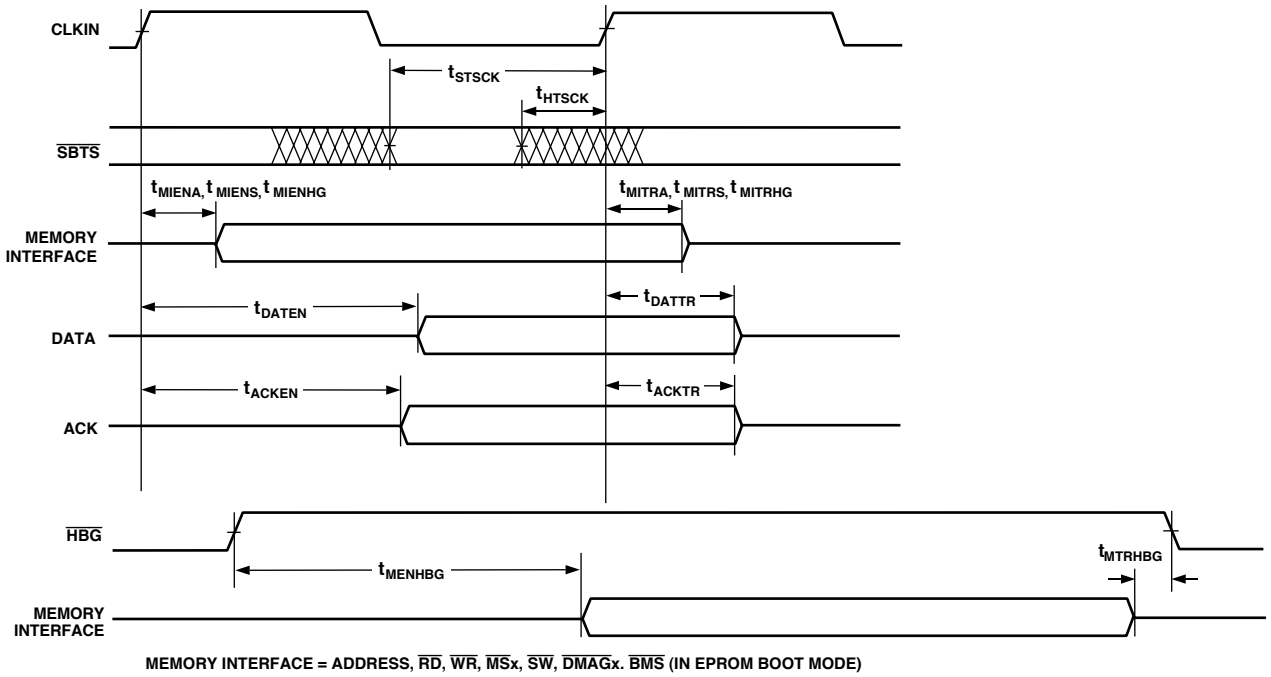


Figure 17. Three-State Timing

DMA Handshake

These specifications describe the three DMA handshake modes. In all three modes DMAR is used to initiate transfers. For handshake mode, $\overline{\text{DMAG}}$ controls the latching or enabling of data externally. For external handshake mode, the data transfer is controlled by the $\text{ADDR}_{23\text{-}0}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{SW}}$, $\overline{\text{MS}}_{3\text{-}0}$, ACK, and $\overline{\text{DMAG}}$ signals. External mode cannot be used for transfers with SDRAM. For Paced Master mode, the data transfer is controlled by $\text{ADDR}_{23\text{-}0}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS}}_{3\text{-}0}$, and ACK (not $\overline{\text{DMAG}}$). For Paced Master mode, the Memory Read-Bus Master, Memory Write-Bus Master, and Synchronous Read/Write-Bus Master timing specifications for $\text{ADDR}_{23\text{-}0}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS}}_{3\text{-}0}$, $\overline{\text{SW}}$, $\text{DATA}_{31\text{-}0}$, and ACK also apply.

Parameter		Min	Max	Unit
Timing Requirements:				
t_{SDRLC}	$\overline{\text{DMAR}}$x Low Setup Before CLKIN[1]	5.0		ns
t_{SDRHC}	$\overline{\text{DMAR}}$x High Setup Before CLKIN[1]	5.0		ns
t_{WDR}	$\overline{\text{DMAR}}$x Width Low (Nonsynchronous)	6.0		ns
$t_{SDATDGL}$	Data Setup After $\overline{\text{DMAG}}$x Low[2]		15.0 + 20 DT	ns
$t_{HDATIDG}$	Data Hold After $\overline{\text{DMAG}}$x High	0.0		ns
t_{DATDRH}	Data Valid After $\overline{\text{DMAR}}$x High[2]		25.0 + 14 DT	ns
t_{DMARLL}	$\overline{\text{DMAR}}$x Low Edge to Low Edge	18.0 + 14 DT		ns
t_{DMARH}	$\overline{\text{DMAR}}$x Width High	6.0		ns
Switching Characteristics:				
t_{DDGL}	$\overline{\text{DMAG}}$x Low Delay After CLKIN	14.0 + 10 DT	20.0 + 10 DT	ns
t_{WDGH}	$\overline{\text{DMAG}}$x High Width	10.0 + 12 DT + HI		ns
t_{WDGL}	$\overline{\text{DMAG}}$x Low Width	16.0 + 20 DT		ns
t_{HDGC}	$\overline{\text{DMAG}}$x High Delay After CLKIN	0.0 – 2 DT	6.0 – 2 DT	ns
t_{DADGH}	Address Select Valid to $\overline{\text{DMAG}}$x High	28.0 + 16 DT		ns
t_{DDGHA}	Address Select Hold After $\overline{\text{DMAG}}$x High	–1.0		ns
$t_{VDATDGH}$	Data Valid Before $\overline{\text{DMAG}}$x High[3]	16.0 + 20 DT		ns
$t_{DATRDGH}$	Data Disable After $\overline{\text{DMAG}}$x High[4]	0.0	4.0	ns
t_{DGWRL}	$\overline{\text{WR}}$ Low Before $\overline{\text{DMAG}}$x Low	5.0 + 6 DT	8.0 + 6 DT	ns
t_{DGWRH}	$\overline{\text{DMAG}}$x Low Before $\overline{\text{WR}}$ High	18.0 + 19 DT + W		ns
t_{DGWRR}	$\overline{\text{WR}}$ High Before $\overline{\text{DMAG}}$x High	0.75 + 1 DT	3.0 + 1 DT	ns
t_{DGRDL}	$\overline{\text{RD}}$ Low Before $\overline{\text{DMAG}}$x Low	5.0	8.0	ns
t_{DRDGH}	$\overline{\text{RD}}$ Low Before $\overline{\text{DMAG}}$x High	24.0 + 26 DT + W		ns
t_{DGRDR}	$\overline{\text{RD}}$ High Before $\overline{\text{DMAG}}$x High	0.0	2.0	ns
t_{DGWR}	$\overline{\text{DMAG}}$x High to $\overline{\text{WR}}$, $\overline{\text{RD}}$ Low	5.0 + 6 DT + HI		ns

W = (number of wait states specified in WAIT register) × t_{CK}.

HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).

NOTES

[1]Only required for recognition in the current cycle.

[2]$t_{SDATDGL}$ is the data setup requirement if $\overline{\text{DMAR}}$x is not being used to hold off completion of a write. Otherwise, if $\overline{\text{DMAR}}$x low holds off completion of the write, the data can be driven t_{DATDRH} after $\overline{\text{DMAR}}$x is brought high.

[3]$t_{VDATDGH}$ is valid if $\overline{\text{DMAR}}$x is not being used to hold off completion of a read. If $\overline{\text{DMAR}}$x is used to prolong the read, then $t_{VDATDGH}$ = 8 + 9 DT + (n × t_{CK}) where *n* equals the number of extra cycles that the access is prolonged.

[4]See System Hold Time Calculation under Test Conditions for calculation of hold times given capacitive and dc loads.

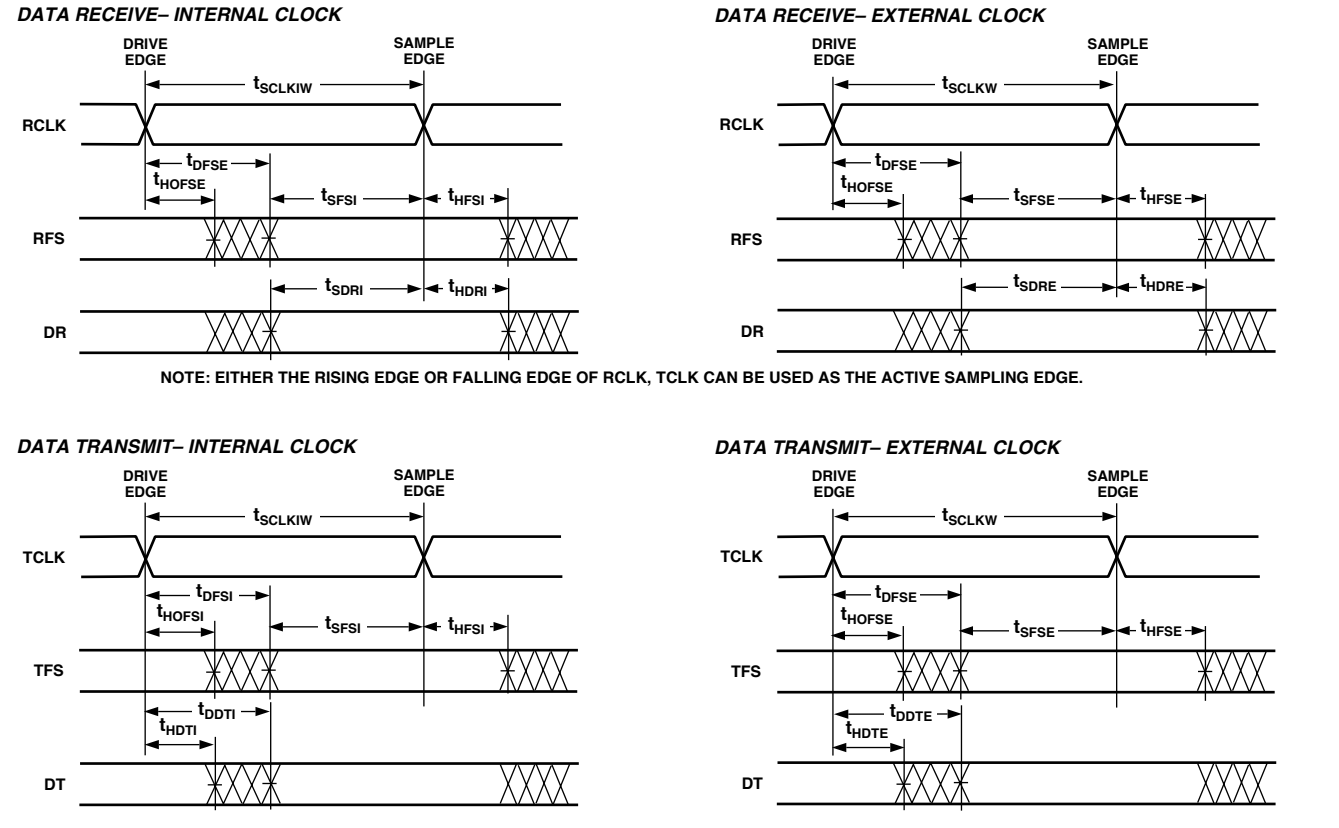


Figure 20. Serial Ports

OUTPUT DRIVE CURRENT

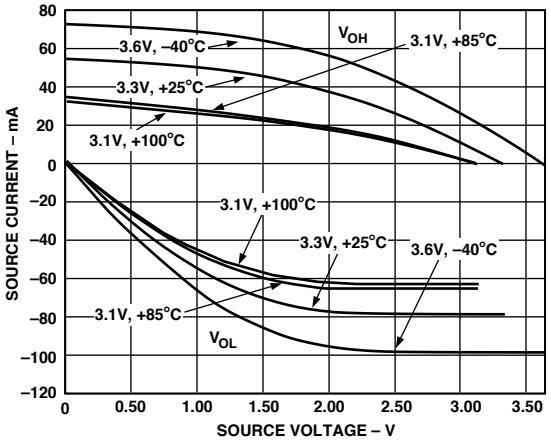


Figure 24. Typical Drive Currents

TEST CONDITIONS

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L and the load current, I_L. This decay time can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times \Delta V}{I_L}$$

The output disable time t_{DIS} is the difference between $t_{MEASURED}$ and t_{DECAY} as shown in Figure 26. The time $t_{MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.5 V.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to when they start driving. The output enable time t_{ENA} is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-21065L's output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (i.e., t_{DATRWH} for the write cycle).

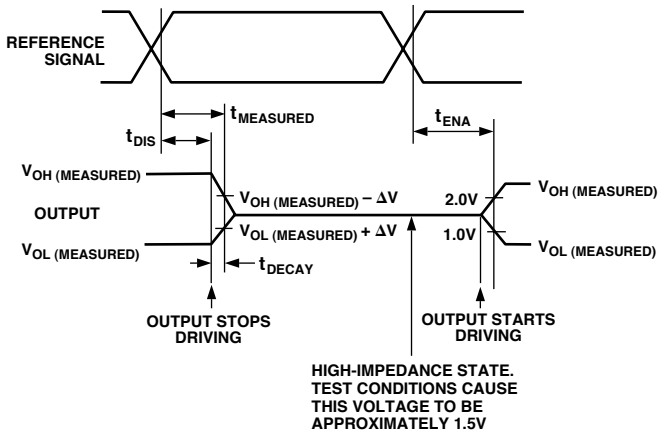


Figure 25. Output Enable

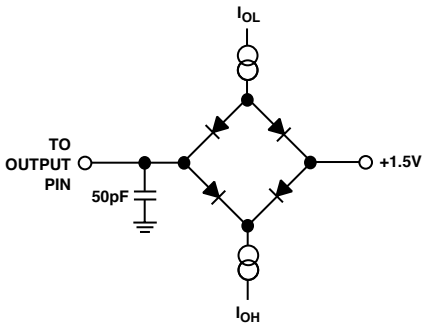


Figure 26. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

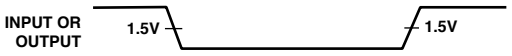


Figure 27. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

POWER DISSIPATION

Total power dissipation has two components: one due to internal circuitry and one due to the switching of external output drivers. Internal power dissipation depends on the sequence in which instructions execute and the data operands involved. See I_{DDIN} calculation in Electrical Characteristics section. Internal power dissipation is calculated this way:

$$P_{INT} = I_{DDIN} \times V_{DD}$$

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

– the number of output pins that switch during each cycle (O)
– the maximum frequency at which the pins can switch (f)
– the load capacitance of the pins (C)
– the voltage swing of the pins (V_{DD}).

The external component is calculated using:

$$P_{EXT} = O \times C \times V_{DD}^2 \times f$$

The load capacitance should include the processor's package capacitance (C_{IN}). The frequency f includes driving the load high and then back low. Address and data pins can drive high and low at a maximum rate of $1/t_{CK}$ while in SDRAM burst mode.

Example:

Estimate P_{EXT} with the following assumptions:

– a system with one bank of external memory (32-bit)
– two 1M × 16 SDRAM chips, each with a control signal load of 3 pF and a data signal load of 4 pF
– external data writes occur in burst mode, two every $1/t_{CK}$ cycles, a potential frequency of $1/t_{CK}$ cycles/s. Assume 50% pin switching
– the external SDRAM clock rate is 60 MHz ($2/t_{CK}$).

The P_{EXT} equation is calculated for each class of pins that can drive:

Table V. External Power Calculations

Pin Type	# of Pins	% Switching	× C	× f	× V_{DD}^2	= P_{EXT}
Address	11	50	× 10.7	× 30 MHz	× 10.9 V	= 0.019 W
$\overline{MS_0}$	1	0	× 10.7	—	× 10.9 V	= 0.000 W
$\overline{SDWE}$	1	0	× 10.7	—	× 10.9 V	= 0.000 W
Data	32	50	× 7.7	× 30 MHz	× 10.9 V	= 0.042 W
SDRAM CLK	1	–	× 10.7	× 30 MHz	× 10.9 V	= 0.007 W

P_{EXT} = 0.068 W

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation. (I_{DDIN} see calculation in Electrical Characteristics section):

$$P_{TOTAL} = P_{EXT} + (I_{DDIN} \times V_{DD})$$

Note that the conditions causing a worst-case P_{EXT} differ from those causing a worst-case P_{INT}. Maximum P_{INT} cannot occur while 100% of the output pins are switching from all ones (1s) to all zeros (0s). Note also that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

ENVIRONMENTAL CONDITIONS

Thermal Characteristics

The ADSP-21065L is offered in a 208-lead MQFP and a 196-ball Mini-BGA package.

The ADSP-21065L is specified for a case temperature (T_{CASE}). To ensure that T_{CASE} is not exceeded, an air flow source may be used.

$$T_{CASE} = T_{AMB} + (PD \times \theta_{CA})$$

T_{CASE} = Case temperature (measured on top surface of package)

PD = Power Dissipation in W (this value depends upon the specific application; a method for calculating PD is shown under Power Dissipation)

θ_{JC} = 7.1°C/W for 208-lead MQFP
θ_{JC} = 5.1°C/W for 196-ball Mini-BGA

Airflow

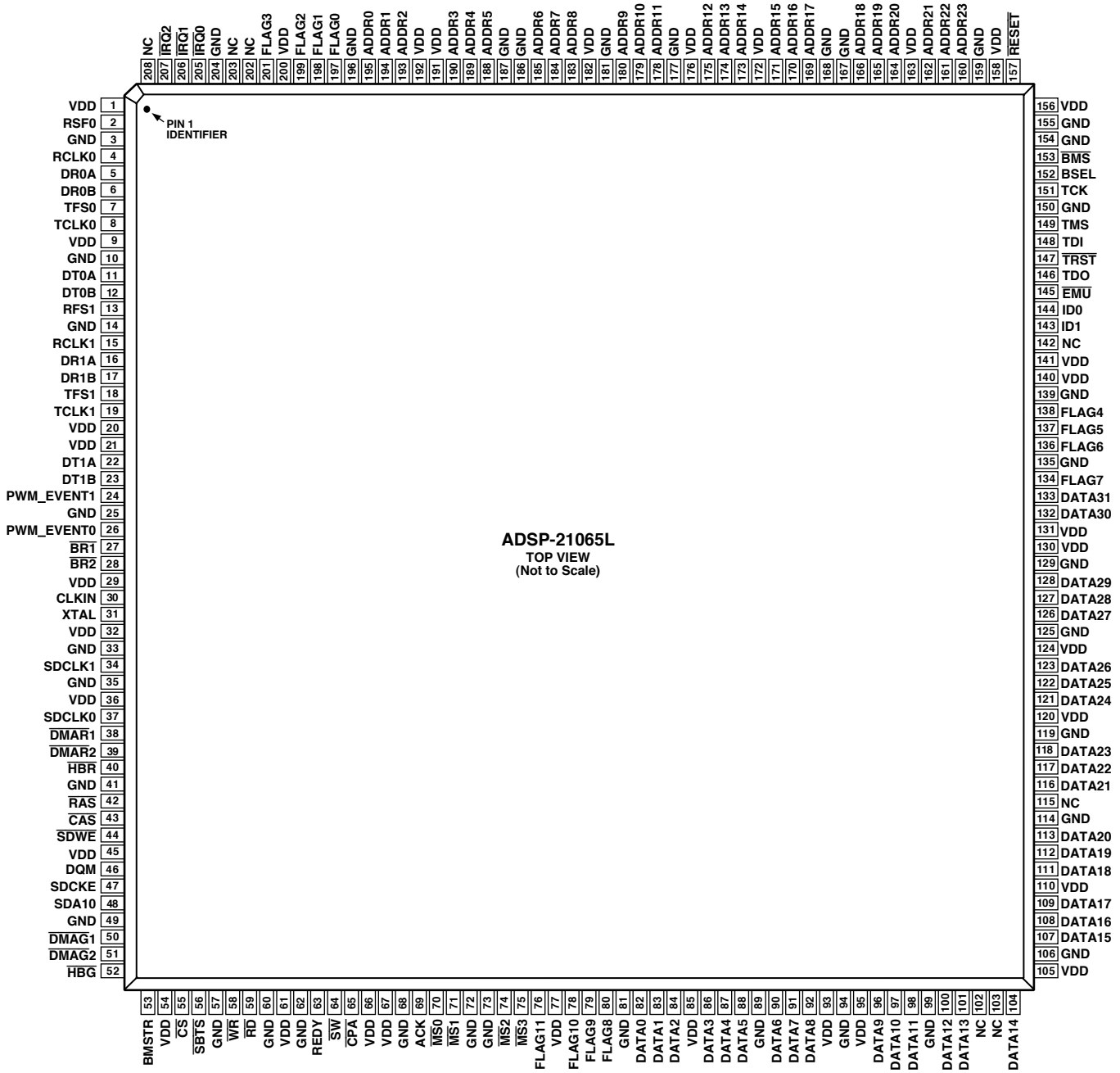
Table VI. Thermal Characteristics (208-Lead MQFP)

(Linear Ft./Min.)	0	100	200	400	600
θ_{CA} (°C/W)	24	20	19	17	13

Table VII. 196-Ball Mini-BGA

(Linear Ft./Min.)	0	200	400
θ_{CA} (°C/W)	38	29	23

208-LEAD MQFP PIN



NC = NO CONNECT

196-BALL MINI-BGA PIN CONFIGURATION

Ball #	Name	Ball #	Name	Ball #	Name	Ball #	Name	Ball #	Name
A1	NC1	B1	DR0A	C1	TCLK0	D1	RCLK1	E1	TFS1
A2	NC2	B2	RFS0	C2	RCLK0	D2	TFS0	E2	DT0B
A3	FLAG2	B3	IRQ0	C3	IRQ2	D3	DR0B	E3	DT0A
A4	ADDR0	B4	FLAG0	C4	FLAG3	D4	IRQ1	E4	RFS1
A5	ADDR3	B5	ADDR2	C5	ADDR1	D5	FLAG1	E5	VDD
A6	ADDR6	B6	ADDR5	C6	ADDR4	D6	VDD	E6	GND
A7	ADDR7	B7	ADDR9	C7	ADDR10	D7	VDD	E7	GND
A8	ADDR8	B8	ADDR12	C8	ADDR13	D8	VDD	E8	GND
A9	ADDR11	B9	ADDR15	C9	ADDR16	D9	VDD	E9	GND
A10	ADDR14	B10	ADDR19	C10	ADDR20	D10	VDD	E10	VDD
A11	ADDR17	B11	ADDR21	C11	ADDR22	D11	BMS	E11	ID0
A12	ADDR18	B12	ADDR23	C12	RESET	D12	TMS	E12	TDI
A13	NC8	B13	GND	C13	BSEL	D13	TRST	E13	ID1
A14	NC7	B14	TCK	C14	TDO	D14	EMU	E14	FLAG4
F1	TCLK1	G1	PWM_ EVENT1	H1	PWM_ EVENT0	J1	CLKIN	K1	DMAR1
F2	DR1B	G2	DT1B	H2	BR1	J2	XTAL	K2	SDCLK0
F3	DR1A	G3	DT1A	H3	BR2	J3	SDCLK1	K3	HBR
F4	VDD	G4	VDD	H4	VDD	J4	VDD	K4	SDWE
F5	GND	G5	GND	H5	GND	J5	GND	K5	VDD
F6	GND	G6	GND	H6	GND	J6	GND	K6	GND
F7	GND	G7	GND	H7	GND	J7	GND	K7	GND
F8	GND	G8	GND	H8	GND	J8	GND	K8	GND
F9	GND	G9	GND	H9	GND	J9	GND	K9	GND
F10	GND	G10	GND	H10	GND	J10	GND	K10	VDD
F11	VDD	G11	VDD	H11	VDD	J11	VDD	K11	DATA19
F12	FLAG6	G12	DATA31	H12	DATA28	J12	DATA24	K12	DATA21
F13	FLAG5	G13	DATA30	H13	DATA27	J13	DATA25	K13	DATA20
F14	FLAG7	G14	DATA29	H14	DATA26	J14	DATA23	K14	DATA22
L1	DMAR2	M1	RAS	N1	DQM	P1	NC3		
L2	CAS	M2	SDCKE	N2	HBG	P2	NC4		
L3	SDA10	M3	DMAG1	N3	BMSTR	P3	GND		
L4	DMAG2	M4	CS	N4	SBTS	P4	WR		
L5	VDD	M5	RD	N5	REDY	P5	SW		
L6	VDD	M6	CPA	N6	GND	P6	MS0		
L7	VDD	M7	ACK	N7	MS1	P7	MS2		
L8	VDD	M8	FLAG10	N8	FLAG11	P8	MS3		
L9	VDD	M9	DATA2	N9	DATA1	P9	FLAG9		
L10	DATA8	M10	DATA5	N10	DATA4	P10	FLAG8		
L11	DATA13	M11	DATA9	N11	DATA7	P11	DATA0		
L12	DATA16	M12	DATA12	N12	DATA10	P12	DATA3		
L13	DATA17	M13	DATA14	N13	DATA11	P13	DATA6		
L14	DATA18	M14	DATA15	N14	NC6	P14	NC5		