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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	49
Number of Gates	15000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a3p015-qng68i

ProASIC3 Device Family Overview

ProASIC3 DC and Switching Characteristics

Pin Descriptions

Package Pin Assignments

Datasheet Information

Table 2-11 • **Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1]**
Applicable to Advanced I/O Banks

	C_{LOAD} (pF)	VCCI (V)	Static Power PDC3 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	–	468.67
3.3 V LVCMOS Wide Range[4]	35	3.3	–	468.67
2.5 V LVCMOS	35	2.5	–	267.48
1.8 V LVCMOS	35	1.8	–	149.46
1.5 V LVCMOS (JESD8-11)	35	1.5	–	103.12
3.3 V PCI	10	3.3	–	201.02
3.3 V PCI-X	10	3.3	–	201.02
Differential				
LVDS	–	2.5	7.74	88.92
LVPECL	–	3.3	19.54	166.52

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *PDC3 is the static power (where applicable) measured on VCCI.*
3. *PAC10 is the total dynamic power measured on VCC and VCCI.*
4. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*

Table 2-12 • **Summary of I/O Output Buffer Power (Per Pin) – Default I/O Software Settings[1]**
Applicable to Standard Plus I/O Banks

	C_{LOAD} (pF)	VCCI (V)	Static Power PDC3 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	–	452.67
3.3 V LVCMOS Wide Range[4]	35	3.3	–	452.67
2.5 V LVCMOS	35	2.5	–	258.32
1.8 V LVCMOS	35	1.8	–	133.59
1.5 V LVCMOS (JESD8-11)	35	1.5	–	92.84
3.3 V PCI	10	3.3	–	184.92
3.3 V PCI-X	10	3.3	–	184.92

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *P_{DC3} is the static power (where applicable) measured on VMV.*
3. *P_{AC10} is the total dynamic power measured on VCC and VMV.*
4. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*

Table 2-45 • **3.3 V LVTTL / 3.3 V LVCMOS High Slew**
Commercial-Case Conditions: T$_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard I/O Banks

Drive Strength	Speed Grade	t$_{DOUT}$	t$_{DP}$	t$_{DIN}$	t$_{PY}$	t$_{EOUT}$	t$_{ZL}$	t$_{ZH}$	t$_{LZ}$	t$_{HZ}$	Units
	–2	0.49	3.29	0.03	0.75	0.32	3.36	2.80	1.79	2.01	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-46 • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew**
Commercial-Case Conditions: T$_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard I/O Banks

Drive Strength	Speed Grade	t$_{DOUT}$	t$_{DP}$	t$_{DIN}$	t$_{PY}$	t$_{EOUT}$	t$_{ZL}$	t$_{ZH}$	t$_{LZ}$	t$_{HZ}$	Units
2 mA	Std.	0.66	9.46	0.04	1.00	0.43	9.64	8.54	2.07	2.04	ns
	–1	0.56	8.05	0.04	0.85	0.36	8.20	7.27	1.76	1.73	ns
	–2	0.49	7.07	0.03	0.75	0.32	7.20	6.38	1.55	1.52	ns
4 mA	Std.	0.66	9.46	0.04	1.00	0.43	9.64	8.54	2.07	2.04	ns
	–1	0.56	8.05	0.04	0.85	0.36	8.20	7.27	1.76	1.73	ns
	–2	0.49	7.07	0.03	0.75	0.32	7.20	6.38	1.55	1.52	ns
6 mA	Std.	0.66	6.57	0.04	1.00	0.43	6.69	5.98	2.40	2.57	ns
	–1	0.56	5.59	0.04	0.85	0.36	5.69	5.09	2.04	2.19	ns
	–2	0.49	4.91	0.03	0.75	0.32	5.00	4.47	1.79	1.92	ns
8 mA	Std.	0.66	6.57	0.04	1.00	0.43	6.69	5.98	2.40	2.57	ns
	–1	0.56	5.59	0.04	0.85	0.36	5.69	5.09	2.04	2.19	ns
	–2	0.49	4.91	0.03	0.75	0.32	5.00	4.47	1.79	1.92	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-49 • **Minimum and Maximum DC Input and Output Levels**
Applicable to Standard I/O Banks

3.3 V LVCMOS Wide Range	Equiv. Software Default	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[2]	IIH[3]
Drive Strength	Drive Strength Option[1]	Min V	Max V	Min V	Max V	Max V	Min V	µA	µA	Max mA[4]	Max mA[4]	µA[5]	µA[5]
100 µA	2 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	25	27	10	10
100 µA	4 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	25	27	10	10
100 µA	6 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	51	54	10	10
100 µA	8 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	51	54	10	10

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*

2. *IIL is the input leakage current per I/O pin over recommended operation conditions where −0.3 V < VIN < VIL.*

3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*

4. *Currents are measured at 85°C junction temperature.*

5. *All LVMCOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*

6. *Software default selection highlighted in gray.*

Timing Characteristics

Table 2-88 • **3.3 V PCI/PCI-X**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.68	0.04	0.86	0.43	2.73	1.95	3.21	3.58	4.97	4.19	ns
–1	0.56	2.28	0.04	0.73	0.36	2.32	1.66	2.73	3.05	4.22	3.56	ns
–2	0.49	2.00	0.03	0.65	0.32	2.04	1.46	2.40	2.68	3.71	3.13	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-89 • **3.3 V PCI/PCI-X**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.31	0.04	0.85	0.43	2.35	1.70	2.79	3.22	4.59	3.94	ns
–1	0.56	1.96	0.04	0.72	0.36	2.00	1.45	2.37	2.74	3.90	3.35	ns
–2	0.49	1.72	0.03	0.64	0.32	1.76	1.27	2.08	2.41	3.42	2.94	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Differential I/O Characteristics

Physical Implementation

Configuration of the I/O modules as a differential pair is handled by Microsemi Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-12. The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, ProASIC3 also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).
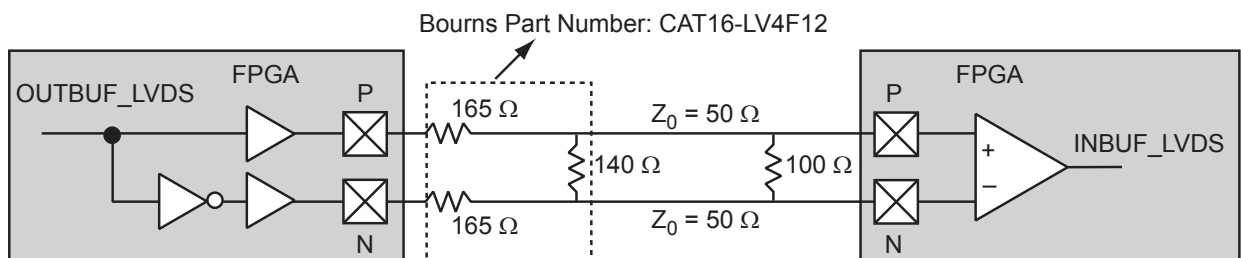
Figure 2-12 • **LVDS Circuit Diagram and Board-Level Implementation**

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset
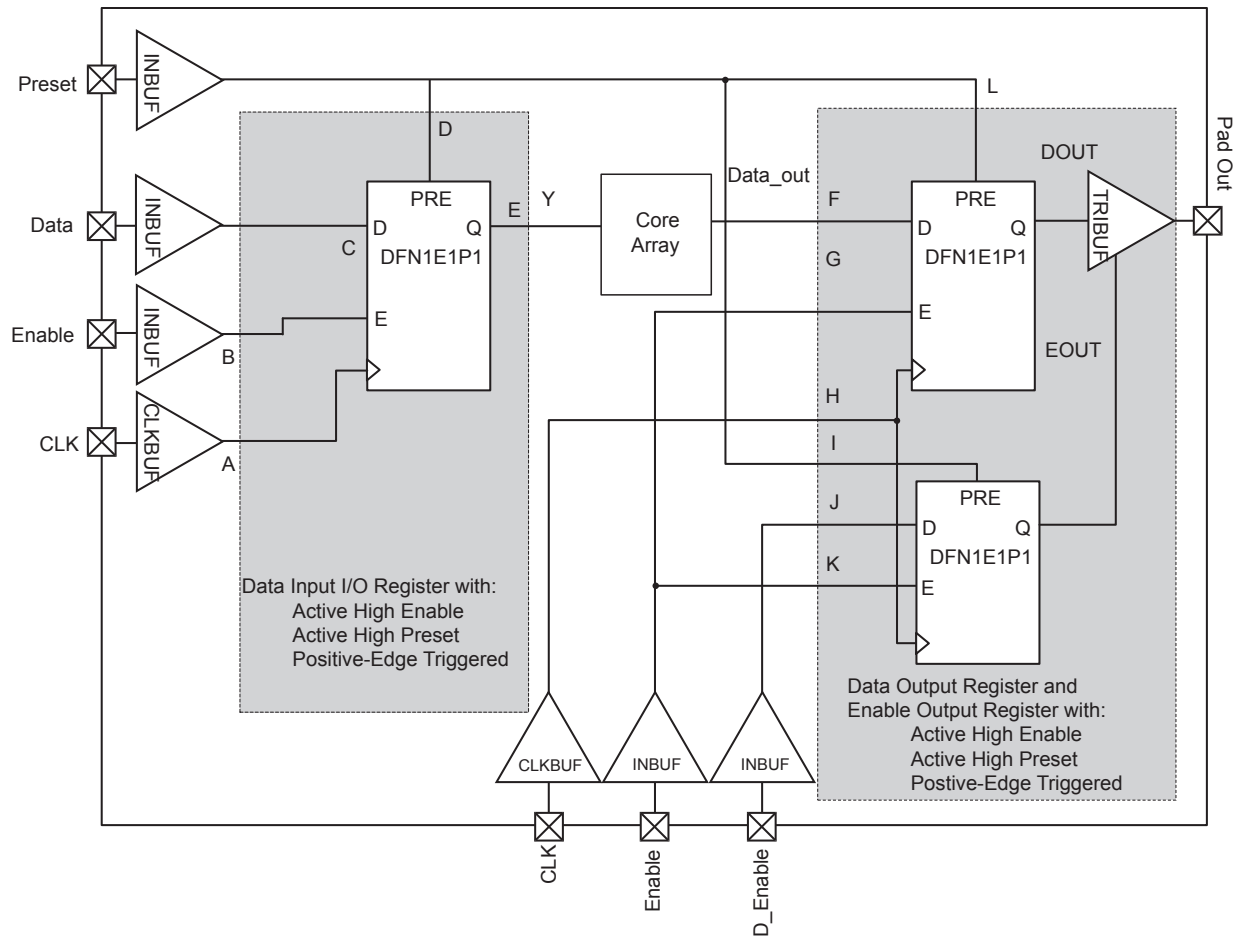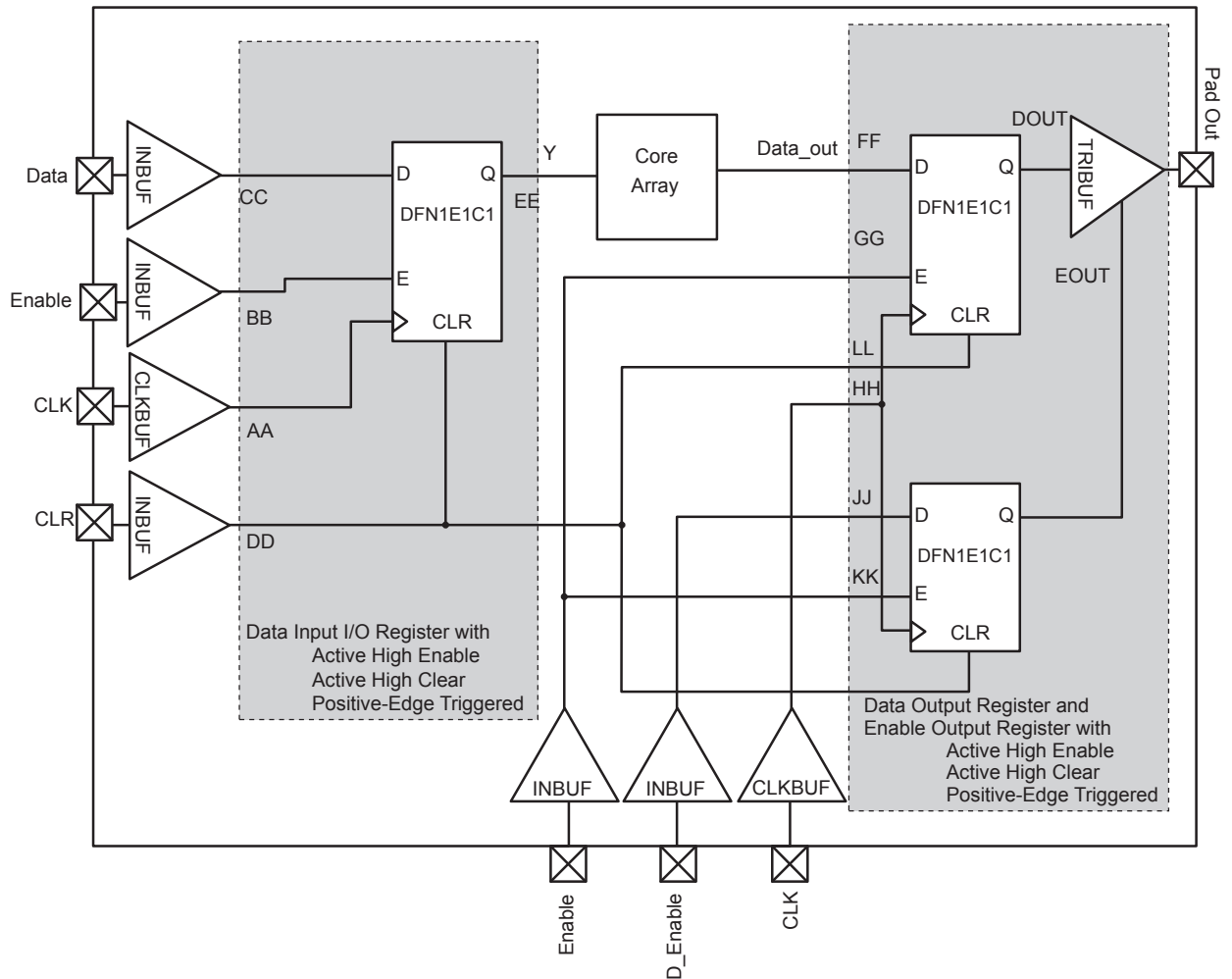

Figure 2-15 • **Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset**

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

Figure 2-16 • **Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

Table 2-113 • **A3P600 Global Resource**
Commercial-Case Conditions: T$_J$ = 70°C, VCC = 1.425 V

Parameter	Description	−2		−1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t$_{RCKL}$	Input Low Delay for Global Clock	0.87	1.09	0.99	1.24	1.17	1.46	ns
t$_{RCKH}$	Input High Delay for Global Clock	0.86	1.11	0.98	1.27	1.15	1.49	ns
t$_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
t$_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
t$_{RCKSW}$	Maximum Skew for Global Clock		0.26		0.29		0.34	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-114 • **A3P1000 Global Resource**
Commercial-Case Conditions: T$_J$ = 70°C, VCC = 1.425 V

| Parameter	Description	−2		−1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t$_{RCKL}$	Input Low Delay for Global Clock	0.94	1.16	1.07	1.32	1.26	1.55	ns
t$_{RCKH}$	Input High Delay for Global Clock	0.93	1.19	1.06	1.35	1.24	1.59	ns
t$_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
t$_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
t$_{RCKSW}$	Maximum Skew for Global Clock		0.26		0.29		0.35	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
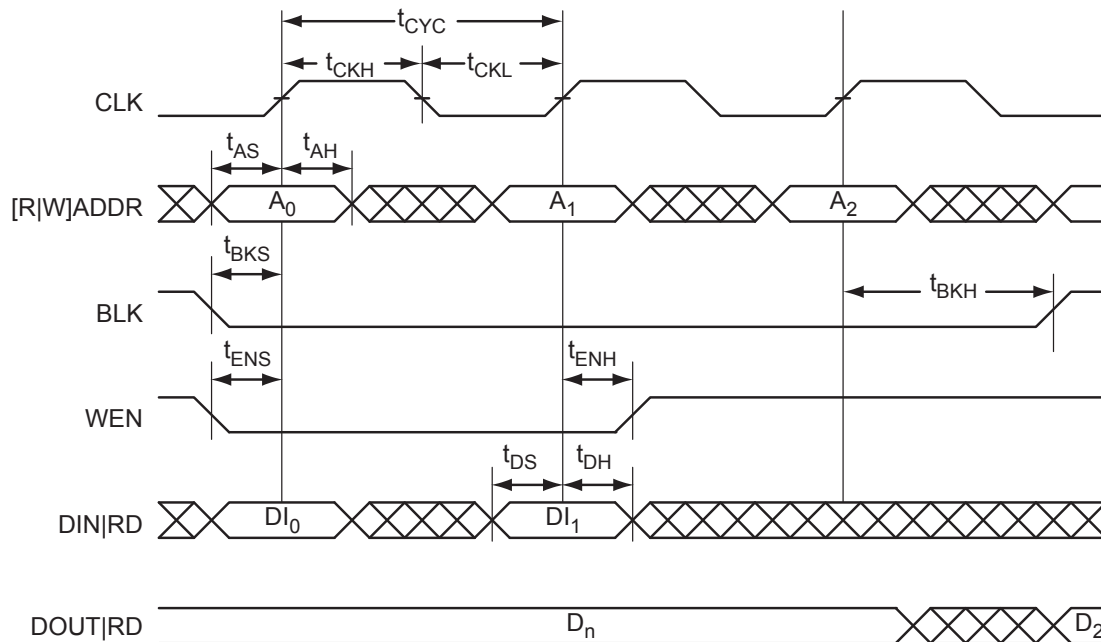
Figure 2-33 • **RAM Write, Output Retained. Applicable to Both RAM4K9 and RAM512x18.**
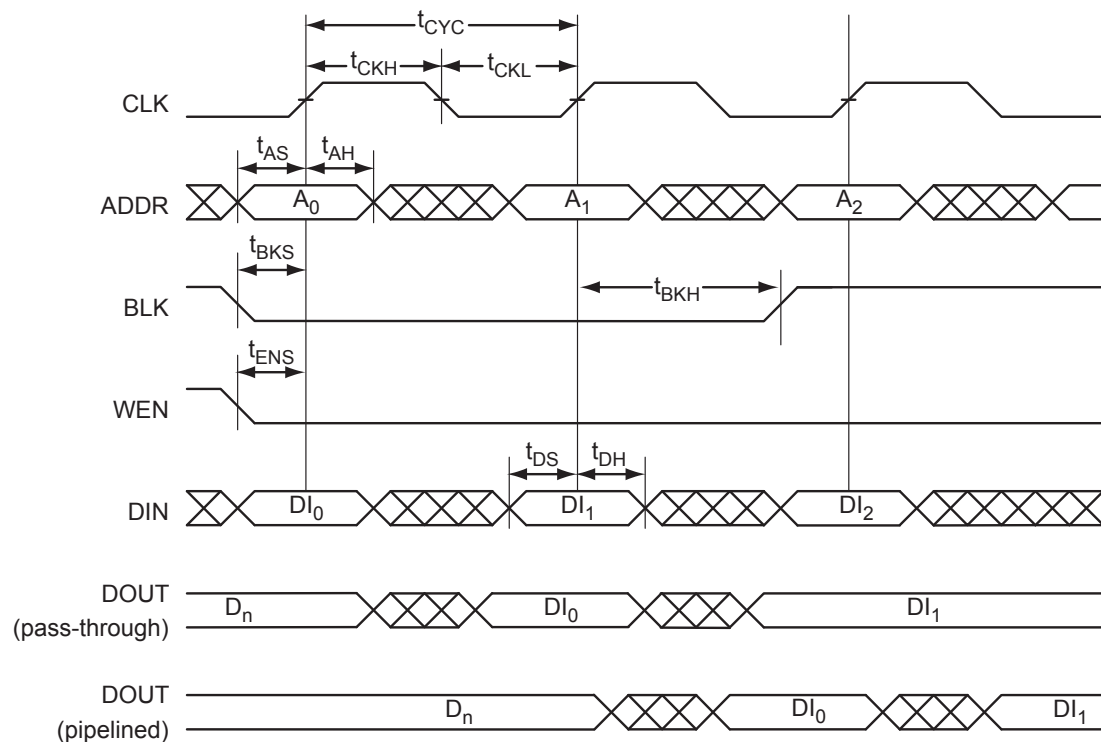
Figure 2-34 • **RAM Write, Output as Write Data (WMODE = 1). Applicable to RAM4K9 Only.**

Figure 2-41 • **FIFO FULL Flag and AFULL Flag Assertion**
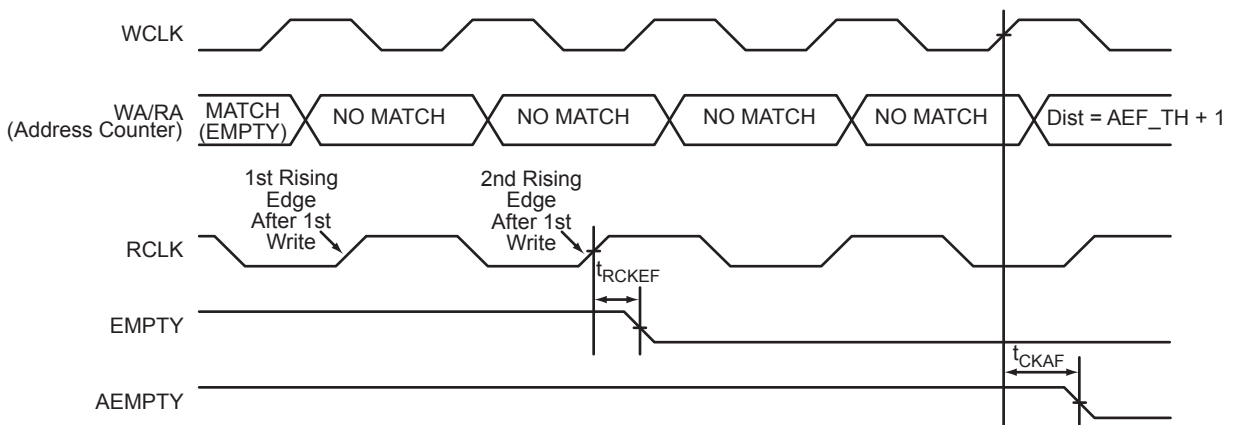
Figure 2-42 • **FIFO EMPTY Flag and AEMPTY Flag Deassertion**
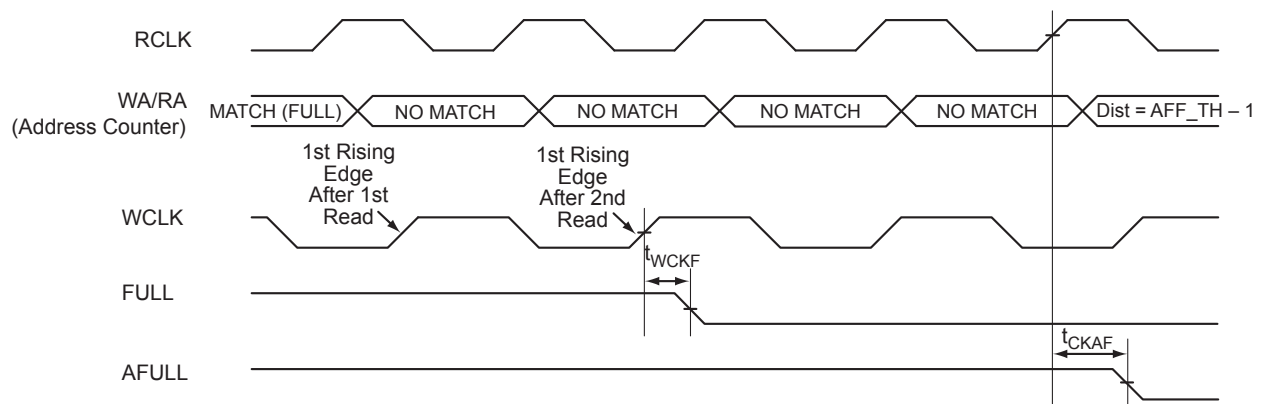
Figure 2-43 • **FIFO FULL Flag and AFULL Flag Deassertion**

Table 2-121 • **A3P250 FIFO 1k×4**
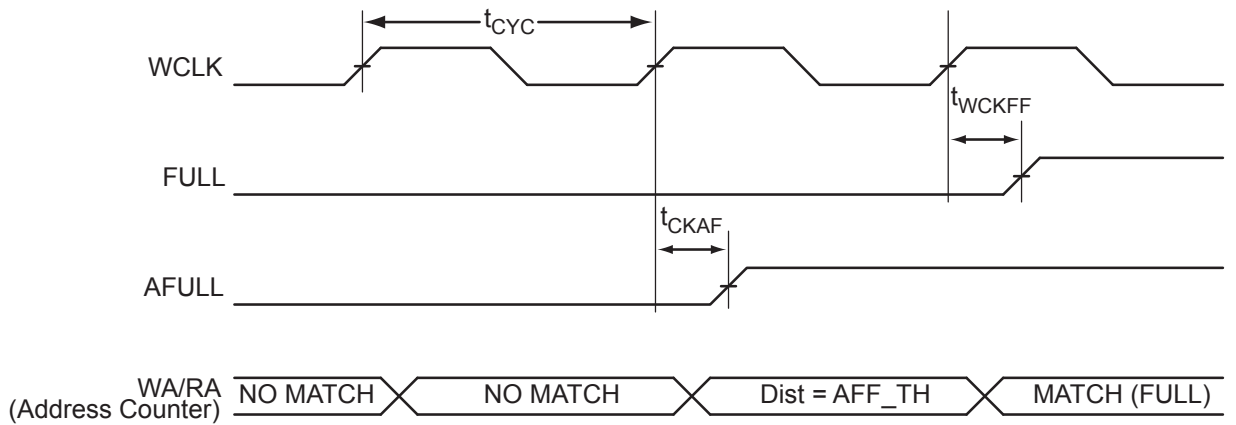**Worst Commercial-Case Conditions: T$_J$ = 70°C, VCC = 1.425 V**

Parameter	Description	–2	–1	Std.	Units
t$_{ENS}$	REN, WEN Setup Time	4.05	4.61	5.42	ns
t$_{ENH}$	REN, WEN Hold Time	0.00	0.00	0.00	ns
t$_{BKS}$	BLK Setup Time	0.19	0.22	0.26	ns
t$_{BKH}$	BLK Hold Time	0.00	0.00	0.00	ns
t$_{DS}$	Input Data (WD) Setup Time	0.18	0.21	0.25	ns
t$_{DH}$	Input Data (WD) Hold Time	0.00	0.00	0.00	ns
t$_{CKQ1}$	Clock High to New Data Valid on RD (flow-through)	2.36	2.68	3.15	ns
t$_{CKQ2}$	Clock High to New Data Valid on RD (pipelined)	0.89	1.02	1.20	ns
t$_{RCKEF}$	RCLK High to Empty Flag Valid	1.72	1.96	2.30	ns
t$_{WCKFF}$	WCLK High to Full Flag Valid	1.63	1.86	2.18	ns
t$_{CKAF}$	Clock High to Almost Empty/Full Flag Valid	6.19	7.05	8.29	ns
t$_{RSTFG}$	RESET Low to Empty/Full Flag Valid	1.69	1.93	2.27	ns
t$_{RSTAF}$	RESET Low to Almost Empty/Full Flag Valid	6.13	6.98	8.20	ns
t$_{RSTBQ}$	RESET Low to Data Out Low on RD (flow-through)	0.92	1.05	1.23	ns
	RESET Low to Data Out Low on RD (pipelined)	0.92	1.05	1.23	ns
t$_{REMRSTB}$	RESET Removal	0.29	0.33	0.38	ns
t$_{RECRSTB}$	RESET Recovery	1.50	1.71	2.01	ns
t$_{MPWRSTB}$	RESET Minimum Pulse Width	0.21	0.24	0.29	ns
t$_{CYC}$	Clock Cycle Time	3.23	3.68	4.32	ns
F$_{MAX}$	Maximum Frequency for FIFO	310	272	231	MHz

mode is not used in the design, the FF pin is available as a regular I/O. For IGLOOe, ProASIC3EL, and RT ProASIC3 only, the FF pin can be configured as a Schmitt trigger input.

When Flash*Freeze mode is used, the FF pin must not be left floating to avoid accidentally entering Flash*Freeze mode. While in Flash*Freeze mode, the Flash*Freeze pin should be constantly asserted.

The Flash*Freeze pin can be used with any single-ended I/O standard supported by the I/O bank in which the pin is located, and input signal levels compatible with the I/O standard selected. The FF pin should be treated as a sensitive asynchronous signal. When defining pin placement and board layout, simultaneously switching outputs (SSOs) and their effects on sensitive asynchronous pins must be considered.

Unused FF or I/O pins are tristated with weak pull-up. This default configuration applies to both Flash*Freeze mode and normal operation mode. No user intervention is required.

JTAG Pins

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

TCK   **Test Clock**

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements. Refer to Table 1 for more information.

Table 1 • **Recommended Tie-Off Values for the TCK and TRST Pins**

VJTAG	Tie-Off Resistance
3.3 V	200 Ω –1 kΩ
2.5 V	200 Ω –1 kΩ
1.8 V	500 Ω –1 kΩ
1.5 V	500 Ω –1 kΩ

Notes:

1. *Equivalent parallel resistance if more than one device is on the JTAG chain*
2. *The TCK pin can be pulled up/down.*
3. *The TRST pin is pulled down.*

TDI   **Test Data Input**

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO   **Test Data Output**

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

TMS   **Test Mode Select**

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

TRST   **Boundary Scan Reset Pin**

The TRST pin functions as an active low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from Table 1 and must satisfy the parallel resistance value requirement. The values in Table 1 correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

QN68		QN68	
Pin Number	A3P015 Function	Pin Number	A3P015 Function
1	IO82RSB1	37	TRST
2	IO80RSB1	38	VJTAG
3	IO78RSB1	39	IO40RSB0
4	IO76RSB1	40	IO37RSB0
5	GEC0/IO73RSB1	41	GDB0/IO34RSB0
6	GEA0/IO72RSB1	42	GDA0/IO33RSB0
7	GEB0/IO71RSB1	43	GDC0/IO32RSB0
8	VCC	44	VCCIB0
9	GND	45	GND
10	VCCIB1	46	VCC
11	IO68RSB1	47	IO31RSB0
12	IO67RSB1	48	IO29RSB0
13	IO66RSB1	49	IO28RSB0
14	IO65RSB1	50	IO27RSB0
15	IO64RSB1	51	IO25RSB0
16	IO63RSB1	52	IO24RSB0
17	IO62RSB1	53	IO22RSB0
18	IO60RSB1	54	IO21RSB0
19	IO58RSB1	55	IO19RSB0
20	IO56RSB1	56	IO17RSB0
21	IO54RSB1	57	IO15RSB0
22	IO52RSB1	58	IO14RSB0
23	IO51RSB1	59	VCCIB0
24	VCC	60	GND
25	GND	61	VCC
26	VCCIB1	62	IO12RSB0
27	IO50RSB1	63	IO10RSB0
28	IO48RSB1	64	IO08RSB0
29	IO46RSB1	65	IO06RSB0
30	IO44RSB1	66	IO04RSB0
31	IO42RSB1	67	IO02RSB0
32	TCK	68	IO00RSB0
33	TDI		
34	TMS		
35	VPUMP		
36	TDO		

QN132	
Pin Number	A3P250 Function
A1	GAB2/IO117UPB3
A2	IO117VPB3
A3	VCCIB3
A4	GFC1/IO110PDB3
A5	GFB0/IO109NPB3
A6	VCCPLF
A7	GFA1/IO108PPB3
A8	GFC2/IO105PPB3
A9	IO103NDB3
A10	VCC
A11	GEA1/IO98PPB3
A12	GEA0/IO98NPB3
A13	GEC2/IO95RSB2
A14	IO91RSB2
A15	VCC
A16	IO90RSB2
A17	IO87RSB2
A18	IO85RSB2
A19	IO82RSB2
A20	IO76RSB2
A21	IO70RSB2
A22	VCC
A23	GDB2/IO62RSB2
A24	TDI
A25	TRST
A26	GDC1/IO58UDB1
A27	VCC
A28	IO54NDB1
A29	IO52NDB1
A30	GCA2/IO51PPB1
A31	GCA0/IO50NPB1
A32	GCB1/IO49PDB1
A33	IO47NSB1
A34	VCC
A35	IO41NPB1
A36	GBA2/IO41PPB1

QN132	
Pin Number	A3P250 Function
A37	GBB1/IO38RSB0
A38	GBC0/IO35RSB0
A39	VCCIB0
A40	IO28RSB0
A41	IO22RSB0
A42	IO18RSB0
A43	IO14RSB0
A44	IO11RSB0
A45	IO07RSB0
A46	VCC
A47	GAC1/IO05RSB0
A48	GAB0/IO02RSB0
B1	IO118VDB3
B2	GAC2/IO116UDB3
B3	GND
B4	GFC0/IO110NDB3
B5	VCOMPLF
B6	GND
B7	GFB2/IO106PSB3
B8	IO103PDB3
B9	GND
B10	GEB0/IO99NDB3
B11	VMV3
B12	GEB2/IO96RSB2
B13	IO92RSB2
B14	GND
B15	IO89RSB2
B16	IO86RSB2
B17	GND
B18	IO78RSB2
B19	IO72RSB2
B20	GND
B21	GNDQ
B22	TMS
B23	TDO
B24	GDC0/IO58VDB1

QN132	
Pin Number	A3P250 Function
B25	GND
B26	IO54PDB1
B27	GCB2/IO52PDB1
B28	GND
B29	GCB0/IO49NDB1
B30	GCC1/IO48PDB1
B31	GND
B32	GBB2/IO42PDB1
B33	VMV1
B34	GBA0/IO39RSB0
B35	GBC1/IO36RSB0
B36	GND
B37	IO26RSB0
B38	IO21RSB0
B39	GND
B40	IO13RSB0
B41	IO08RSB0
B42	GND
B43	GAC0/IO04RSB0
B44	GNDQ
C1	GAA2/IO118UDB3
C2	IO116VDB3
C3	VCC
C4	GFB1/IO109PPB3
C5	GFA0/IO108NPB3
C6	GFA2/IO107PSB3
C7	IO105NPB3
C8	VCCIB3
C9	GEB1/IO99PDB3
C10	GNDQ
C11	GEA2/IO97RSB2
C12	IO94RSB2
C13	VCCIB2
C14	IO88RSB2
C15	IO84RSB2
C16	IO80RSB2

VQ100		VQ100		VQ100	
Pin Number	**A3P060 Function**	**Pin Number**	**A3P060 Function**	**Pin Number**	**A3P060 Function**
1	GND	37	VCC	73	GBA2/IO25RSB0
2	GAA2/IO51RSB1	38	GND	74	VMV0
3	IO52RSB1	39	VCCIB1	75	GNDQ
4	GAB2/IO53RSB1	40	IO60RSB1	76	GBA1/IO24RSB0
5	IO95RSB1	41	IO59RSB1	77	GBA0/IO23RSB0
6	GAC2/IO94RSB1	42	IO58RSB1	78	GBB1/IO22RSB0
7	IO93RSB1	43	IO57RSB1	79	GBB0/IO21RSB0
8	IO92RSB1	44	GDC2/IO56RSB1	80	GBC1/IO20RSB0
9	GND	45	GDB2/IO55RSB1	81	GBC0/IO19RSB0
10	GFB1/IO87RSB1	46	GDA2/IO54RSB1	82	IO18RSB0
11	GFB0/IO86RSB1	47	TCK	83	IO17RSB0
12	VCOMPLF	48	TDI	84	IO15RSB0
13	GFA0/IO85RSB1	49	TMS	85	IO13RSB0
14	VCCPLF	50	VMV1	86	IO11RSB0
15	GFA1/IO84RSB1	51	GND	87	VCCIB0
16	GFA2/IO83RSB1	52	VPUMP	88	GND
17	VCC	53	NC	89	VCC
18	VCCIB1	54	TDO	90	IO10RSB0
19	GEC1/IO77RSB1	55	TRST	91	IO09RSB0
20	GEB1/IO75RSB1	56	VJTAG	92	IO08RSB0
21	GEB0/IO74RSB1	57	GDA1/IO49RSB0	93	GAC1/IO07RSB0
22	GEA1/IO73RSB1	58	GDC0/IO46RSB0	94	GAC0/IO06RSB0
23	GEA0/IO72RSB1	59	GDC1/IO45RSB0	95	GAB1/IO05RSB0
24	VMV1	60	GCC2/IO43RSB0	96	GAB0/IO04RSB0
25	GNDQ	61	GCB2/IO42RSB0	97	GAA1/IO03RSB0
26	GEA2/IO71RSB1	62	GCA0/IO40RSB0	98	GAA0/IO02RSB0
27	GEB2/IO70RSB1	63	GCA1/IO39RSB0	99	IO01RSB0
28	GEC2/IO69RSB1	64	GCC0/IO36RSB0	100	IO00RSB0
29	IO68RSB1	65	GCC1/IO35RSB0		
30	IO67RSB1	66	VCCIB0		
31	IO66RSB1	67	GND		
32	IO65RSB1	68	VCC		
33	IO64RSB1	69	IO31RSB0		
34	IO63RSB1	70	GBC2/IO29RSB0		
35	IO62RSB1	71	GBB2/IO27RSB0		
36	IO61RSB1	72	IO26RSB0		

PQ208		PQ208		PQ208	
Pin Number	A3P600 Function	Pin Number	A3P600 Function	Pin Number	A3P600 Function
109	TRST	145	IO64PDB1	181	IO27RSB0
110	VJTAG	146	IO63NDB1	182	IO26RSB0
111	GDA0/IO88NDB1	147	IO63PDB1	183	IO25RSB0
112	GDA1/IO88PDB1	148	IO62NDB1	184	IO24RSB0
113	GDB0/IO87NDB1	149	GBC2/IO62PDB1	185	IO23RSB0
114	GDB1/IO87PDB1	150	IO61NDB1	186	VCCIB0
115	GDC0/IO86NDB1	151	GBB2/IO61PDB1	187	VCC
116	GDC1/IO86PDB1	152	IO60NDB1	188	IO20RSB0
117	IO84NDB1	153	GBA2/IO60PDB1	189	IO19RSB0
118	IO84PDB1	154	VMV1	190	IO18RSB0
119	IO82NDB1	155	GNDQ	191	IO17RSB0
120	IO82PDB1	156	GND	192	IO16RSB0
121	IO81PSB1	157	VMV0	193	IO14RSB0
122	GND	158	GBA1/IO59RSB0	194	IO12RSB0
123	VCCIB1	159	GBA0/IO58RSB0	195	GND
124	IO77NDB1	160	GBB1/IO57RSB0	196	IO10RSB0
125	IO77PDB1	161	GBB0/IO56RSB0	197	IO09RSB0
126	NC	162	GND	198	IO08RSB0
127	IO74NDB1	163	GBC1/IO55RSB0	199	IO07RSB0
128	GCC2/IO74PDB1	164	GBC0/IO54RSB0	200	VCCIB0
129	GCB2/IO73PSB1	165	IO52RSB0	201	GAC1/IO05RSB0
130	GND	166	IO50RSB0	202	GAC0/IO04RSB0
131	GCA2/IO72PSB1	167	IO48RSB0	203	GAB1/IO03RSB0
132	GCA1/IO71PDB1	168	IO46RSB0	204	GAB0/IO02RSB0
133	GCA0/IO71NDB1	169	IO44RSB0	205	GAA1/IO01RSB0
134	GCB0/IO70NDB1	170	VCCIB0	206	GAA0/IO00RSB0
135	GCB1/IO70PDB1	171	VCC	207	GNDQ
136	GCC0/IO69NDB1	172	IO36RSB0	208	VMV0
137	GCC1/IO69PDB1	173	IO35RSB0		
138	IO67NDB1	174	IO34RSB0		
139	IO67PDB1	175	IO33RSB0		
140	VCCIB1	176	IO32RSB0		
141	GND	177	IO31RSB0		
142	VCC	178	GND		
143	IO65PSB1	179	IO29RSB0		
144	IO64NDB1	180	IO28RSB0		

FG144	
Pin Number	**A3P400 Function**
K1	GEB0/IO136NDB3
K2	GEA1/IO135PDB3
K3	GEA0/IO135NDB3
K4	GEA2/IO134RSB2
K5	IO127RSB2
K6	IO121RSB2
K7	GND
K8	IO104RSB2
K9	GDC2/IO82RSB2
K10	GND
K11	GDA0/IO79VDB1
K12	GDB0/IO78VDB1
L1	GND
L2	VMV3
L3	GEB2/IO133RSB2
L4	IO128RSB2
L5	VCCIB2
L6	IO119RSB2
L7	IO114RSB2
L8	IO110RSB2
L9	TMS
L10	VJTAG
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO132RSB2
M3	IO129RSB2
M4	IO126RSB2
M5	IO124RSB2
M6	IO122RSB2
M7	IO117RSB2
M8	IO115RSB2
M9	TDI
M10	VCCIB2
M11	VPUMP
M12	GNDQ

FG484		FG484	
Pin Number	**A3P400 Function**	**Pin Number**	**A3P400 Function**
Y15	VCC	AB7	IO119RSB2
Y16	NC	AB8	IO114RSB2
Y17	NC	AB9	IO109RSB2
Y18	GND	AB10	NC
Y19	NC	AB11	NC
Y20	NC	AB12	IO104RSB2
Y21	NC	AB13	IO103RSB2
Y22	VCCIB1	AB14	NC
AA1	GND	AB15	NC
AA2	VCCIB3	AB16	IO91RSB2
AA3	NC	AB17	IO90RSB2
AA4	NC	AB18	NC
AA5	NC	AB19	NC
AA6	NC	AB20	VCCIB2
AA7	NC	AB21	GND
AA8	NC	AB22	GND
AA9	NC		
AA10	NC		
AA11	NC		
AA12	NC		
AA13	NC		
AA14	NC		
AA15	NC		
AA16	NC		
AA17	NC		
AA18	NC		
AA19	NC		
AA20	NC		
AA21	VCCIB1		
AA22	GND		
AB1	GND		
AB2	GND		
AB3	VCCIB2		
AB4	NC		
AB5	NC		
AB6	IO121RSB2		

Revision	Changes	Page
Revision 9 (Oct 2009) Product Brief v1.3	The CS121 package was added to table under "Features and Benefits" section, the "I/Os Per Package 1" table, Table 1 • ProASIC3 FPGAs Package Sizes Dimensions, "ProASIC3 Ordering Information", and the "Temperature Grade Offerings" table.	I – IV
	"ProASIC3 Ordering Information" was revised to include the fact that some RoHS compliant packages are halogen-free.	IV
Packaging v1.5	The "CS121 – Bottom View" figure and pin table for A3P060 are new.	4-15
Revision 8 (Aug 2009) Product Brief v1.2	All references to M7 devices (CoreMP7) and speed grade –F were removed from this document.	N/A
	Table 1-1 I/O Standards supported is new.	1-7
	The I/Os with Advanced I/O Standards section was revised to add definitions of hot-swap and cold-sparing.	1-7
DC and Switching Characteristics v1.4	3.3 V LVCMOS and 1.2 V LVCMOS Wide Range support was added to the datasheet. This affects all tables that contained 3.3 V LVCMOS and 1.2 V LVCMOS data.	N/A
	I_{IL} and I_{IH} input leakage current information was added to all "Minimum and Maximum DC Input and Output Levels" tables.	N/A
	–F was removed from the datasheet. The speed grade is no longer supported.	N/A
	The notes in Table 2-2 • Recommended Operating Conditions 1 were updated.	2-2
	Table 2-4 • Overshoot and Undershoot Limits 1 was updated.	2-3
	Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays was updated.	2-6
	In Table 2-116 • RAM4K9, the following specifications were removed: t_{WRO} t_{CCKH}	2-96
	In Table 2-117 • RAM512X18, the following specifications were removed: t_{WRO} t_{CCKH}	2-97
	In the title of Table 2-74 • 1.8 V LVCMOS High Slew, VCCI had a typo. It was changed from 3.0 V to 1.7 V.	2-58
Revision 7 (Feb 2009) Product Brief v1.1	The "Advanced I/O" section was revised to add a bullet regarding wide range power supply voltage support.	I
	The table under "Features and Benefits" section, was updated to include a value for typical equivalent macrocells for A3P250.	I
	The QN48 package was added to the following tables: the table under "Features and Benefits" section, "I/Os Per Package 1" "ProASIC3 FPGAs Package Sizes Dimensions", and "Temperature Grade Offerings". The number of singled-ended I/Os for QN68 was added to the "I/Os Per Package 1" table.	N/A
	The Wide Range I/O Support section is new.	1-7
Revision 6 (Dec 2008) Packaging v1.4	The "QN48 – Bottom View" section is new.	4-1
	The "QN68" pin table for A3P030 is new.	4-5

Revision	Changes	Page
Advance v0.6 (continued)	The "RESET" section was updated.	2-25
	The "WCLK and RCLK" section was updated.	2-25
	The "RESET" section was updated.	2-25
	The "RESET" section was updated.	2-27
	The "Introduction" of the "Advanced I/Os" section was updated.	2-28
	The "I/O Banks" section is new. This section explains the following types of I/Os: Advanced Standard+ Standard Table 2-12 • Automotive ProASIC3 Bank Types Definition and Differences is new. This table describes the standards listed above.	2-29
	PCI-X 3.3 V was added to the Compatible Standards for 3.3 V in Table 2-11 • VCCI Voltages and Compatible Standards	2-29
	Table 2-13 • ProASIC3 I/O Features was updated.	2-30
	The "Double Data Rate (DDR) Support" section was updated to include information concerning implementation of the feature.	2-32
	The "Electrostatic Discharge (ESD) Protection" section was updated to include testing information.	2-35
	Level 3 and 4 descriptions were updated in Table 2-43 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3 Devices.	2-64
	The notes in Table 2-43 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3 Devices were updated.	2-64
	The "Simultaneous Switching Outputs (SSOs) and Printed Circuit Board Layout" section is new.	2-41
	A footnote was added to Table 2-14 • Maximum I/O Frequency for Single-Ended and Differential I/Os in All Banks in Automotive ProASIC3 Devices (maximum drive strength and high slew selected).	2-30
	Table 2-18 • Automotive ProASIC3 I/O Attributes vs. I/O Standard Applications	2-45
	Table 2-50 • ProASIC3 Output Drive (OUT_DRIVE) for Standard I/O Bank Type (A3P030 device)	2-83
	Table 2-51 • ProASIC3 Output Drive for Standard+ I/O Bank Type was updated.	2-84
	Table 2-54 • ProASIC3 Output Drive for Advanced I/O Bank Type was updated.	2-84
	The "x" was updated in the "User I/O Naming Convention" section.	2-48
	The "VCC Core Supply Voltage" pin description was updated.	2-50
	The "VMVx I/O Supply Voltage (quiet)" pin description was updated to include information concerning leaving the pin unconnected.	2-50
	The "VJTAG JTAG Supply Voltage" pin description was updated.	2-50
	The "VPUMP Programming Supply Voltage" pin description was updated to include information on what happens when the pin is tied to ground.	2-50
	The "I/O User Input/Output" pin description was updated to include information on what happens when the pin is unused.	2-50
	The "JTAG Pins" section was updated to include information on what happens when the pin is unused.	2-51