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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

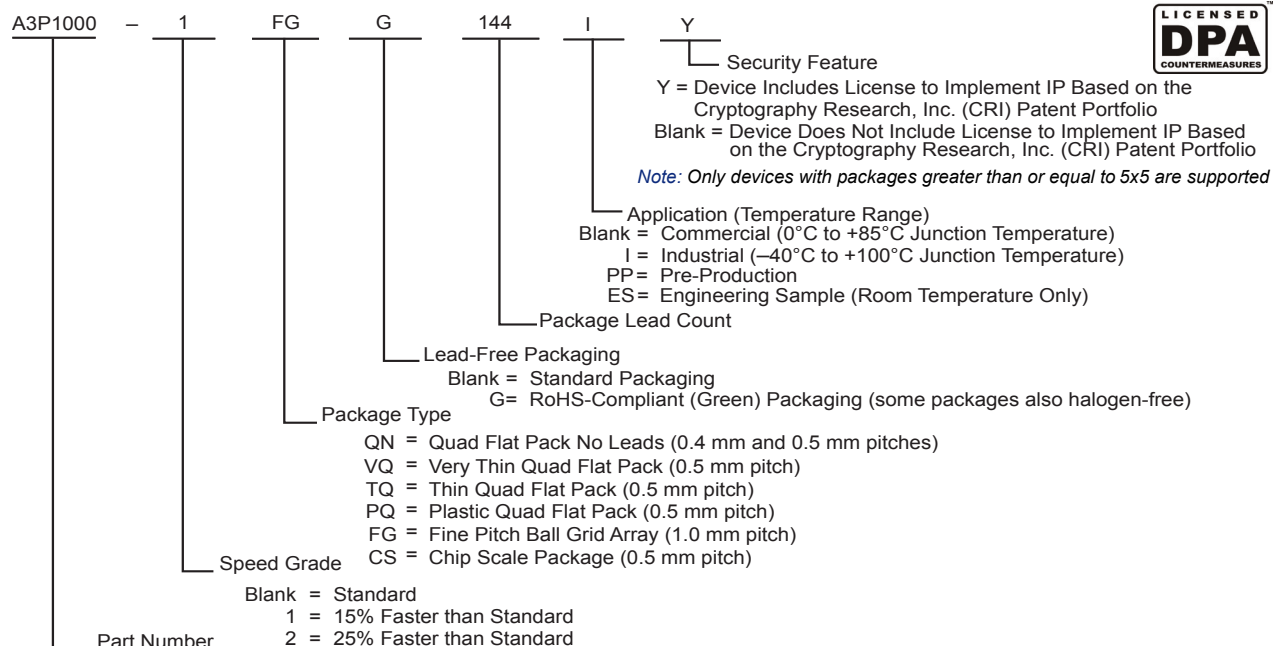
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	18432
Number of I/O	80
Number of Gates	60000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	132-WFQFN
Supplier Device Package	132-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a3p060-1qng132i

ProASIC3 Ordering Information



ProASIC3 Devices

A3P015 = 15,000 System Gates (A3P015 is not recommended for new designs.)
 A3P030 = 30,000 System Gates
 A3P060 = 60,000 System Gates
 A3P125 = 125,000 System Gates
 A3P250 = 250,000 System Gates
 A3P400 = 400,000 System Gates
 A3P600 = 600,000 System Gates
 A3P1000 = 1,000,000 System Gates

ProASIC3 Devices with Cortex-M1

M1A3P250 = 250,000 System Gates
 M1A3P400 = 400,000 System Gates
 M1A3P600 = 600,000 System Gates
 M1A3P1000 = 1,000,000 System Gates

ProASIC3 Device Status

ProASIC3 Devices	Status	Cortex-M1 Devices	Status
A3P015	Not recommended for new designs.		
A3P030	Production		
A3P060	Production		
A3P125	Production		
A3P250	Production	M1A3P250	Production
A3P400	Production	M1A3P400	Production
A3P600	Production	M1A3P600	Production
A3P1000	Production	M1A3P1000	Production

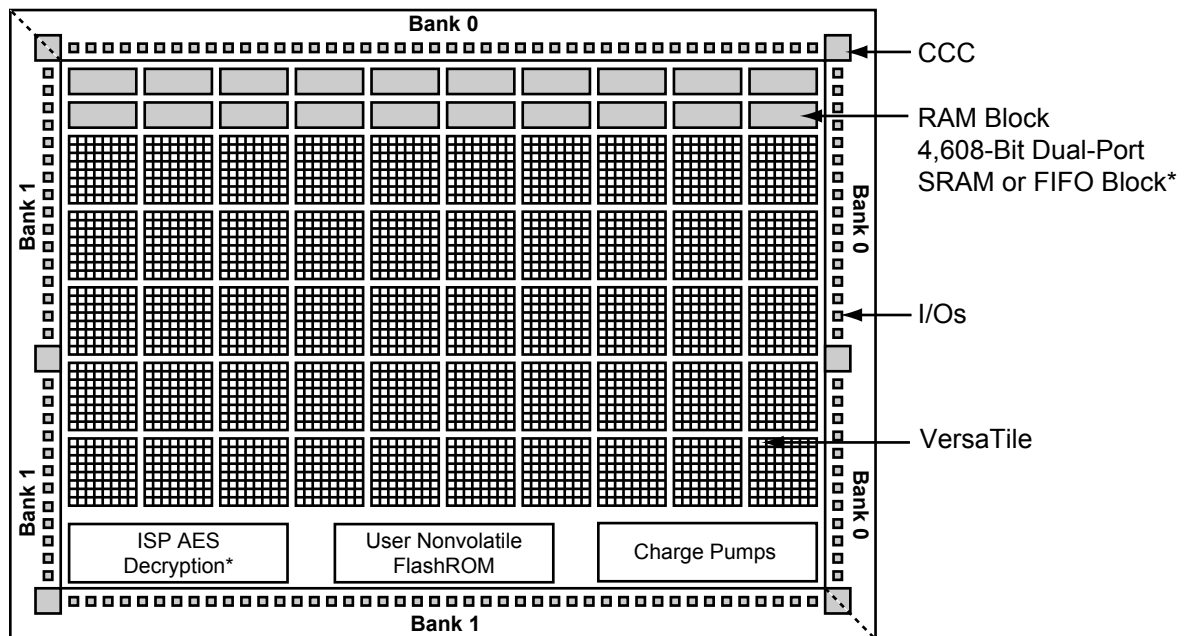
Advanced Flash Technology

The ProASIC3 family offers many benefits, including nonvolatility and reprogrammability through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

Advanced Architecture

The proprietary ProASIC3 architecture provides granularity comparable to standard-cell ASICs. The ProASIC3 device consists of five distinct and programmable architectural features (Figure 1-1 and Figure 1-2 on page 1-4):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory†
- Extensive CCCs and PLLs†
- Advanced I/O structure



Note: *Not supported by A3P015 and A3P030 devices

Figure 1-1 • ProASIC3 Device Architecture Overview with Two I/O Banks (A3P015, A3P030, A3P060, and A3P125)

† The A3P015 and A3P030 do not support PLL or SRAM.

User I/O Characteristics

Timing Model

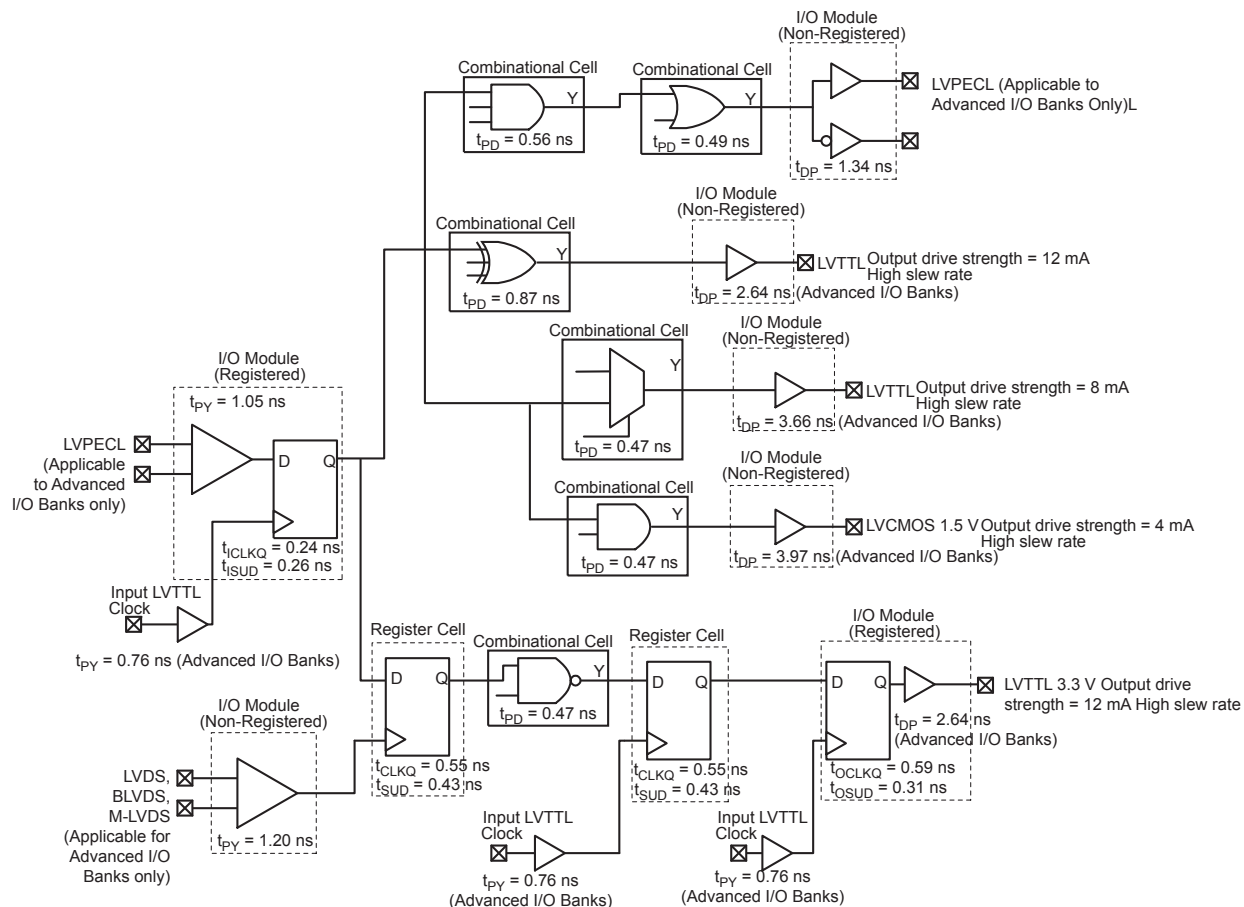


Figure 2-3 • Timing Model

Operating Conditions: –2 Speed, Commercial Temperature Range ($T_J = 70^\circ\text{C}$), Worst Case $V_{CC} = 1.425$ V

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-18 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings
 Applicable to Advanced I/O Banks

I/O Standard	Drive Strength	Equiv. Software Default Drive Strength Option ²	Slew Rate	VIL		VIH		VOL	VOH	IOL ¹ mA	IOH ¹ mA
				Min V	Max V	Min V	Max V	Max V	Min V		
3.3 V LVTTTL / 3.3 V LVC MOS	12 mA	12 mA	High	−0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVC MOS Wide Range ³	100 μ A	12 mA	High	−0.3	0.8	2	3.6	0.2	VCCI − 0.2	0.1	0.1
2.5 V LVC MOS	12 mA	12 mA	High	−0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8 V LVC MOS	12 mA	12 mA	High	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	12	12
1.5 V LVC MOS	12 mA	12 mA	High	−0.3	0.35 * VCCI	0.65 * VCCI	1.6	0.25 * VCCI	0.75 * VCCI	12	12
3.3 V PCI	Per PCI specifications										
3.3 V PCI-X	Per PCI-X specifications										

Notes:

1. Currents are measured at 85°C junction temperature.
2. 3.3 V LVC MOS wide range is applicable to 100 μ A drive strength only. The configuration will NOT operate at the equivalent software default drive strength. These values are for Normal Ranges ONLY.
3. All LVC MOS 3.3 V software macros support LVC MOS 3.3 V wide range as specified in the JESD-8B specification.

Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings
 –2 Speed Grade, Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$,
 Worst-Case V_{CCI} (per standard)
 Standard Plus I/O Banks

I/O Standard	Drive Strength	Equiv. Software Default Drive Strength Option ¹	Slew Rate	Capacitive Load (pF)	External Resistor	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	12 mA	High	35	–	0.45	2.36	0.03	0.75	0.32	2.40	1.93	2.08	2.41	4.07	3.60	ns
3.3 V LVCMOS Wide Range ²	100 μA	12 mA	High	35	–	0.45	3.65	0.03	1.14	0.32	3.65	2.93	3.22	3.72	6.18	5.46	ns
2.5 V LVCMOS	12 mA	12 mA	High	35	–	0.45	2.39	0.03	0.97	0.32	2.44	2.35	2.11	2.32	4.11	4.02	ns
1.8 V LVCMOS	8 mA	8 mA	High	35	–	0.45	3.03	0.03	0.90	0.32	2.87	3.03	2.19	2.32	4.54	4.70	ns
1.5 V LVCMOS	4 mA	4 mA	High	35	–	0.45	3.61	0.03	1.06	0.32	3.35	3.61	2.26	2.34	5.02	5.28	ns
3.3 V PCI	Per PCI spec	–	High	10	25 ⁴	0.45	1.72	0.03	0.64	0.32	1.76	1.27	2.08	2.41	3.42	2.94	ns
3.3 V PCI-X	Per PCI-X spec	–	High	10	25 ⁴	0.45	1.72	0.03	0.62	0.32	1.76	1.27	2.08	2.41	3.42	2.94	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.
4. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-11 on page 2-64](#) for connectivity. This resistor is not required during normal operation.

Table 2-34 • I/O Short Currents IOSH/IOSL
 Applicable to Standard I/O Banks

	Drive Strength	IOSL (mA) ¹	IOSH (mA) ¹
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
3.3 V LVCMOS Wide Range ²	100 μ A	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	18	16
	4 mA	18	16
	6 mA	37	32
	8 mA	37	32
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
1.5 V LVCMOS	2 mA	16	13

Notes:

1. $T_J = 100^\circ\text{C}$
2. Applicable to 3.3 V LVCMOS Wide Range. I_{OSL}/I_{OSH} dependent on the I/O buffer drive strength selected for wide range applications. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3 V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C , the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-35 • Duration of Short Circuit Event Before Failure

Temperature	Time before Failure
-40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	0.5 years

Table 2-36 • I/O Input Rise Time, Fall Time, and Related I/O Reliability

Input Buffer	Input Rise/Fall Time (min)	Input Rise/Fall Time (max)	Reliability
LVTTTL/LVCMOS	No requirement	10 ns *	20 years (110°C)
LVDS/B-LVDS/ M-LVDS/LVPECL	No requirement	10 ns *	10 years (100°C)

Note: *The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.

Table 2-64 • 2.5 V LVCMOS High Slew

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
Applicable to Standard I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.66	8.20	0.04	1.29	0.43	7.24	8.20	2.03	1.91	ns
	–1	0.56	6.98	0.04	1.10	0.36	6.16	6.98	1.73	1.62	ns
	–2	0.49	6.13	0.03	0.96	0.32	5.41	6.13	1.52	1.43	ns
4 mA	Std.	0.66	8.20	0.04	1.29	0.43	7.24	8.20	2.03	1.91	ns
	–1	0.56	6.98	0.04	1.10	0.36	6.16	6.98	1.73	1.62	ns
	–2	0.49	6.13	0.03	0.96	0.32	5.41	6.13	1.52	1.43	ns
6 mA	Std.	0.66	4.77	0.04	1.29	0.43	4.55	4.77	2.38	2.55	ns
	–1	0.56	4.05	0.04	1.10	0.36	3.87	4.05	2.03	2.17	ns
	–2	0.49	3.56	0.03	0.96	0.32	3.40	3.56	1.78	1.91	ns
8 mA	Std.	0.66	4.77	0.04	1.29	0.43	4.55	4.77	2.38	2.55	ns
	–1	0.56	4.05	0.04	1.10	0.36	3.87	4.05	2.03	2.17	ns
	–2	0.49	3.56	0.03	0.96	0.32	3.40	3.56	1.78	1.91	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-65 • 2.5 V LVCMOS Low Slew

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
Applicable to Standard I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.66	11.00	0.04	1.29	0.43	10.37	11.00	2.03	1.83	ns
	–1	0.56	9.35	0.04	1.10	0.36	8.83	9.35	1.73	1.56	ns
	–2	0.49	8.21	0.03	0.96	0.32	7.75	8.21	1.52	1.37	ns
4 mA	Std.	0.66	11.00	0.04	1.29	0.43	10.37	11.00	2.03	1.83	ns
	–1	0.56	9.35	0.04	1.10	0.36	8.83	9.35	1.73	1.56	ns
	–2	0.49	8.21	0.03	0.96	0.32	7.75	8.21	1.52	1.37	ns
6 mA	Std.	0.66	7.50	0.04	1.29	0.43	7.36	7.50	2.39	2.46	ns
	–1	0.56	6.38	0.04	1.10	0.36	6.26	6.38	2.03	2.10	ns
	–2	0.49	5.60	0.03	0.96	0.32	5.49	5.60	1.78	1.84	ns
8 mA	Std.	0.66	7.50	0.04	1.29	0.43	7.36	7.50	2.39	2.46	ns
	–1	0.56	6.38	0.04	1.10	0.36	6.26	6.38	2.03	2.10	ns
	–2	0.49	5.60	0.03	0.96	0.32	5.49	5.60	1.78	1.84	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-71 • 1.8 V LVCMOS Low Slew

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 1.7\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	15.53	0.04	1.22	0.43	14.11	15.53	2.78	1.60	16.35	17.77	ns
	–1	0.56	13.21	0.04	1.04	0.36	12.01	13.21	2.36	1.36	13.91	15.11	ns
	–2	0.49	11.60	0.03	0.91	0.32	10.54	11.60	2.07	1.19	12.21	13.27	ns
4 mA	Std.	0.66	10.48	0.04	1.22	0.43	10.41	10.48	3.23	2.73	12.65	12.71	ns
	–1	0.56	8.91	0.04	1.04	0.36	8.86	8.91	2.75	2.33	10.76	10.81	ns
	–2	0.49	7.82	0.03	0.91	0.32	7.77	7.82	2.41	2.04	9.44	9.49	ns
6 mA	Std.	0.66	8.05	0.04	1.22	0.43	8.20	7.84	3.54	3.27	10.43	10.08	ns
	–1	0.56	6.85	0.04	1.04	0.36	6.97	6.67	3.01	2.78	8.88	8.57	ns
	–2	0.49	6.01	0.03	0.91	0.32	6.12	5.86	2.64	2.44	7.79	7.53	ns
8 mA	Std.	0.66	7.50	0.04	1.22	0.43	7.64	7.30	3.61	3.41	9.88	9.53	ns
	–1	0.56	6.38	0.04	1.04	0.36	6.50	6.21	3.07	2.90	8.40	8.11	ns
	–2	0.49	5.60	0.03	0.91	0.32	5.71	5.45	2.69	2.55	7.38	7.12	ns
12 mA	Std.	0.66	7.29	0.04	1.22	0.43	7.23	7.29	3.71	3.95	9.47	9.53	ns
	–1	0.56	6.20	0.04	1.04	0.36	6.15	6.20	3.15	3.36	8.06	8.11	ns
	–2	0.49	5.45	0.03	0.91	0.32	5.40	5.45	2.77	2.95	7.07	7.12	ns
16 mA	Std.	0.66	7.29	0.04	1.22	0.43	7.23	7.29	3.71	3.95	9.47	9.53	ns
	–1	0.56	6.20	0.04	1.04	0.36	6.15	6.20	3.15	3.36	8.06	8.11	ns
	–2	0.49	5.45	0.03	0.91	0.32	5.40	5.45	2.77	2.95	7.07	7.12	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-72 • 1.8 V LVC MOS High Slew**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 1.7\text{ V}$** **Applicable to Standard Plus I/O Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	11.33	0.04	1.20	0.43	8.72	11.33	2.24	1.52	10.96	13.57	ns
	–1	0.56	9.64	0.04	1.02	0.36	7.42	9.64	1.91	1.29	9.32	11.54	ns
	–2	0.49	8.46	0.03	0.90	0.32	6.51	8.46	1.68	1.14	8.18	10.13	ns
4 mA	Std.	0.66	6.48	0.04	1.20	0.43	5.48	6.48	2.65	2.60	7.72	8.72	ns
	–1	0.56	5.51	0.04	1.02	0.36	4.66	5.51	2.25	2.21	6.56	7.42	ns
	–2	0.49	4.84	0.03	0.90	0.32	4.09	4.84	1.98	1.94	5.76	6.51	ns
6 mA	Std.	0.66	4.06	0.04	1.20	0.43	3.84	4.06	2.93	3.10	6.07	6.30	ns
	–1	0.56	3.45	0.04	1.02	0.36	3.27	3.45	2.49	2.64	5.17	5.36	ns
	–2	0.49	3.03	0.03	0.90	0.32	2.87	3.03	2.19	2.32	4.54	4.70	ns
8 mA	Std.	0.66	4.06	0.04	1.20	0.43	3.84	4.06	2.93	3.10	6.07	6.30	ns
	–1	0.56	3.45	0.04	1.02	0.36	3.27	3.45	2.49	2.64	5.17	5.36	ns
	–2	0.49	3.03	0.03	0.90	0.32	2.87	3.03	2.19	2.32	4.54	4.70	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Input Register

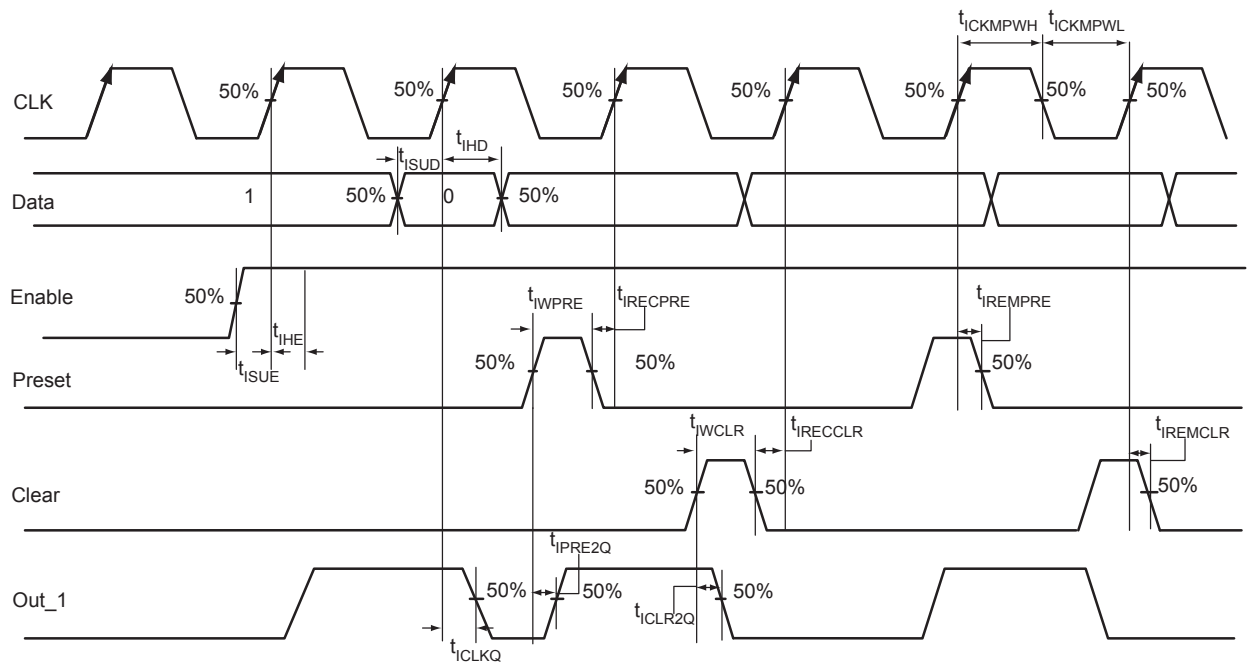


Figure 2-17 • Input Register Timing Diagram

Timing Characteristics

Table 2-98 • Input Data Register Propagation Delays

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2	-1	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.24	0.27	0.32	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.26	0.30	0.35	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.37	0.42	0.50	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.45	0.52	0.61	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.45	0.52	0.61	ns
t_{IEMCLR}	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	0.00	ns
t_{IRECCLR}	Asynchronous Clear Recovery Time for the Input Data Register	0.22	0.25	0.30	ns
t_{IEMPRE}	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	0.00	ns
t_{IRECPRE}	Asynchronous Preset Recovery Time for the Input Data Register	0.22	0.25	0.30	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.22	0.25	0.30	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.22	0.25	0.30	ns
t_{ICKMPWH}	Clock Minimum Pulse Width High for the Input Data Register	0.36	0.41	0.48	ns
t_{ICKMPWL}	Clock Minimum Pulse Width Low for the Input Data Register	0.32	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

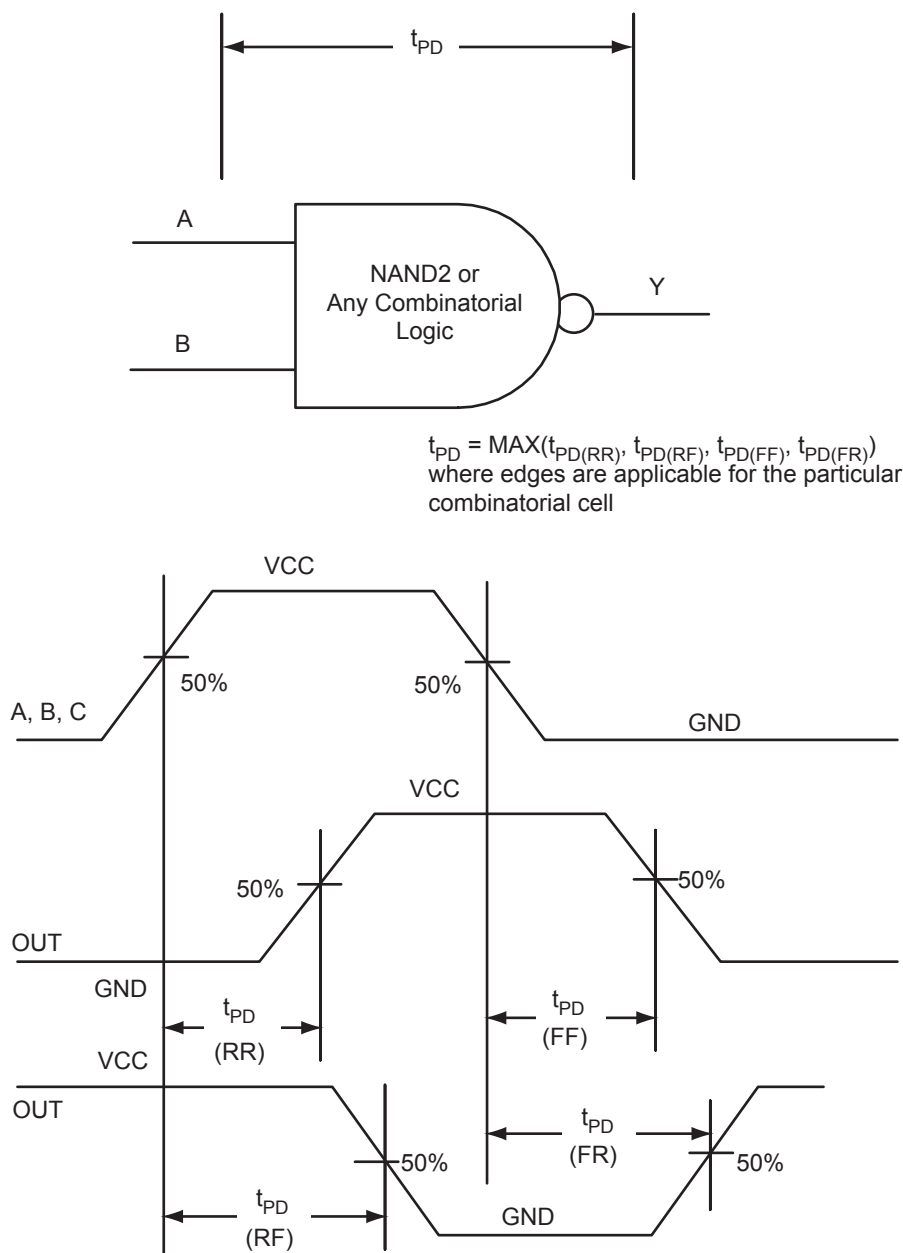


Figure 2-25 • Timing Model and Waveforms

FIFO

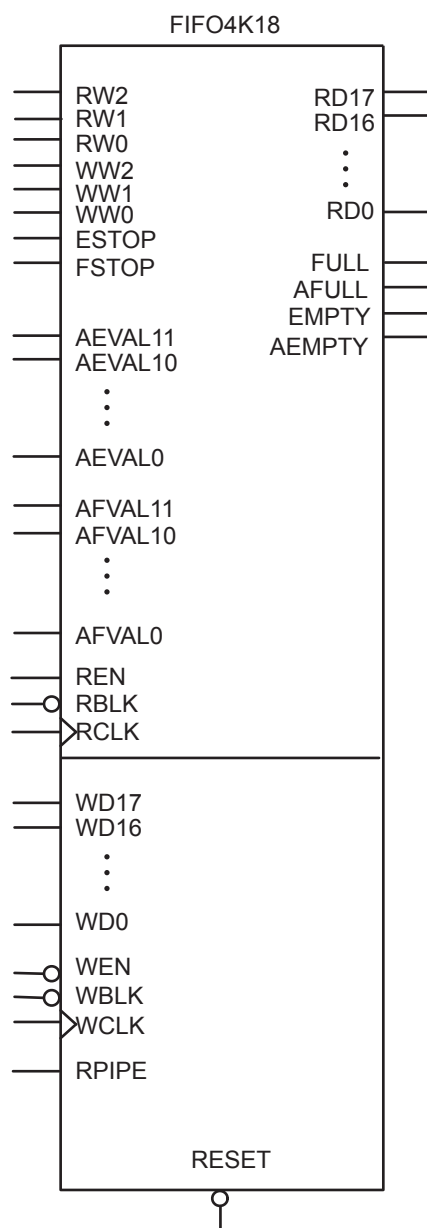


Figure 2-36 • FIFO Model

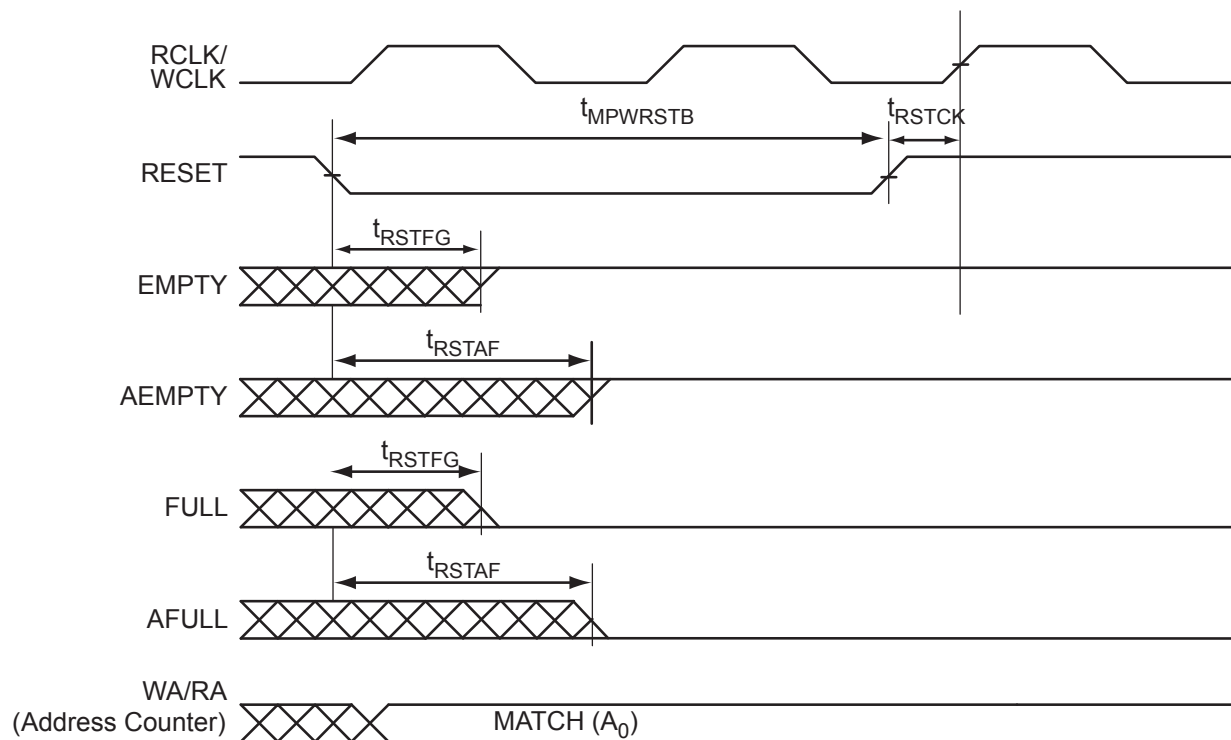


Figure 2-39 • FIFO Reset

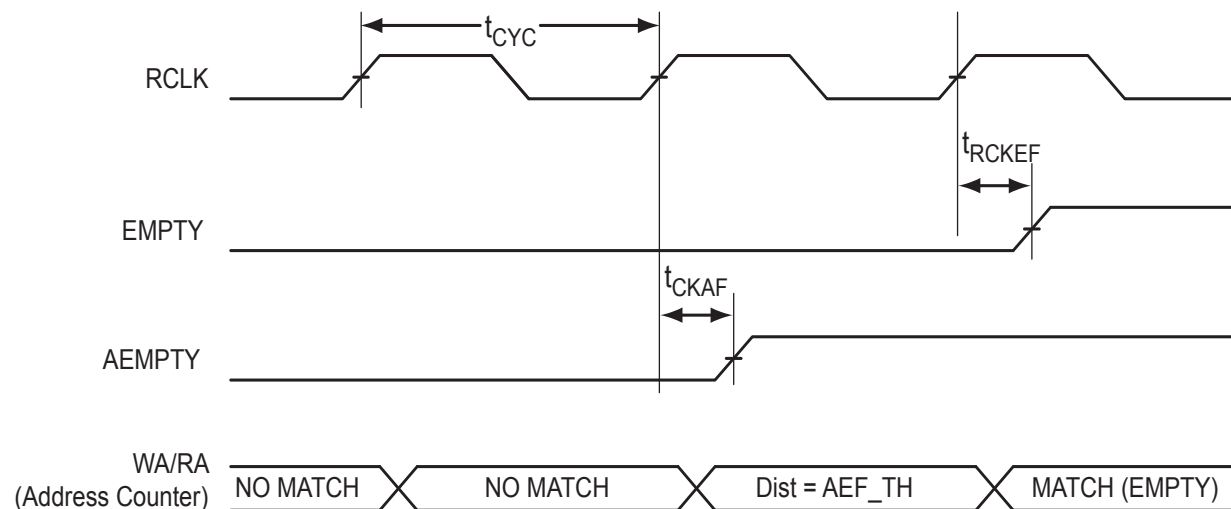
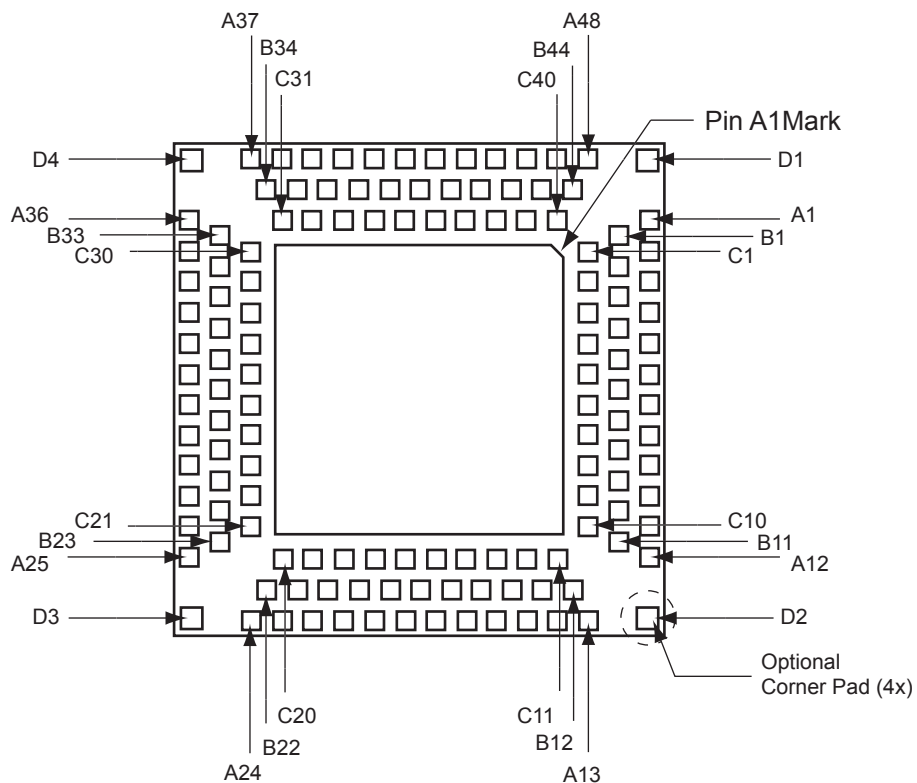


Figure 2-40 • FIFO EMPTY Flag and AEMPTY Flag Assertion

QN132 – Bottom View



Notes:

1. The die attach paddle center of the package is tied to ground (GND).
2. Option corner pads come with this device and package combination. It is optional to tie them to ground or leave them floating.
3. The QN132 package is discontinued and is not available for ProASIC3 devices.
4. For more information on package drawings, see [PD3068: Package Mechanical Drawings](#).

QN132	
Pin Number	A3P250 Function
A1	GAB2/IO117UPB3
A2	IO117VPB3
A3	VCCIB3
A4	GFC1/IO110PDB3
A5	GFB0/IO109NPB3
A6	VCCPLF
A7	GFA1/IO108PPB3
A8	GFC2/IO105PPB3
A9	IO103NDB3
A10	VCC
A11	GEA1/IO98PPB3
A12	GEA0/IO98NPB3
A13	GEC2/IO95RSB2
A14	IO91RSB2
A15	VCC
A16	IO90RSB2
A17	IO87RSB2
A18	IO85RSB2
A19	IO82RSB2
A20	IO76RSB2
A21	IO70RSB2
A22	VCC
A23	GDB2/IO62RSB2
A24	TDI
A25	TRST
A26	GDC1/IO58UDB1
A27	VCC
A28	IO54NDB1
A29	IO52NDB1
A30	GCA2/IO51PPB1
A31	GCA0/IO50NPB1
A32	GCB1/IO49PDB1
A33	IO47NSB1
A34	VCC
A35	IO41NPB1
A36	GBA2/IO41PPB1

QN132	
Pin Number	A3P250 Function
A37	GBB1/IO38RSB0
A38	GBC0/IO35RSB0
A39	VCCIB0
A40	IO28RSB0
A41	IO22RSB0
A42	IO18RSB0
A43	IO14RSB0
A44	IO11RSB0
A45	IO07RSB0
A46	VCC
A47	GAC1/IO05RSB0
A48	GAB0/IO02RSB0
B1	IO118VDB3
B2	GAC2/IO116UDB3
B3	GND
B4	GFC0/IO110NDB3
B5	VCOMPLF
B6	GND
B7	GFB2/IO106PSB3
B8	IO103PDB3
B9	GND
B10	GEB0/IO99NDB3
B11	VMV3
B12	GEB2/IO96RSB2
B13	IO92RSB2
B14	GND
B15	IO89RSB2
B16	IO86RSB2
B17	GND
B18	IO78RSB2
B19	IO72RSB2
B20	GND
B21	GNDQ
B22	TMS
B23	TDO
B24	GDC0/IO58VDB1

QN132	
Pin Number	A3P250 Function
B25	GND
B26	IO54PDB1
B27	GCB2/IO52PDB1
B28	GND
B29	GCB0/IO49NDB1
B30	GCC1/IO48PDB1
B31	GND
B32	GBB2/IO42PDB1
B33	VMV1
B34	GBA0/IO39RSB0
B35	GBC1/IO36RSB0
B36	GND
B37	IO26RSB0
B38	IO21RSB0
B39	GND
B40	IO13RSB0
B41	IO08RSB0
B42	GND
B43	GAC0/IO04RSB0
B44	GNDQ
C1	GAA2/IO118UDB3
C2	IO116VDB3
C3	VCC
C4	GFB1/IO109PPB3
C5	GFA0/IO108NPB3
C6	GFA2/IO107PSB3
C7	IO105NPB3
C8	VCCIB3
C9	GEB1/IO99PDB3
C10	GNDQ
C11	GEA2/IO97RSB2
C12	IO94RSB2
C13	VCCIB2
C14	IO88RSB2
C15	IO84RSB2
C16	IO80RSB2

QN132	
Pin Number	A3P250 Function
C17	IO74RSB2
C18	VCCIB2
C19	TCK
C20	VMV2
C21	VPUMP
C22	VJTAG
C23	VCCIB1
C24	IO53NSB1
C25	IO51NPB1
C26	GCA1/IO50PPB1
C27	GCC0/IO48NDB1
C28	VCCIB1
C29	IO42NDB1
C30	GNDQ
C31	GBA1/IO40RSB0
C32	GBB0/IO37RSB0
C33	VCC
C34	IO24RSB0
C35	IO19RSB0
C36	IO16RSB0
C37	IO10RSB0
C38	VCCIB0
C39	GAB1/IO03RSB0
C40	VMV0
D1	GND
D2	GND
D3	GND
D4	GND

FG144	
Pin Number	A3P060 Function
K1	GEB0/IO74RSB1
K2	GEA1/IO73RSB1
K3	GEA0/IO72RSB1
K4	GEA2/IO71RSB1
K5	IO65RSB1
K6	IO64RSB1
K7	GND
K8	IO57RSB1
K9	GDC2/IO56RSB1
K10	GND
K11	GDA0/IO50RSB0
K12	GDB0/IO48RSB0
L1	GND
L2	VMV1
L3	GEB2/IO70RSB1
L4	IO67RSB1
L5	VCCIB1
L6	IO62RSB1
L7	IO59RSB1
L8	IO58RSB1
L9	TMS
L10	VJTAG
L11	VMV1
L12	TRST
M1	GNDQ
M2	GEC2/IO69RSB1
M3	IO68RSB1
M4	IO66RSB1
M5	IO63RSB1
M6	IO61RSB1
M7	IO60RSB1
M8	NC
M9	TDI
M10	VCCIB1
M11	VPUMP
M12	GNDQ

FG256	
Pin Number	A3P600 Function
P9	IO107RSB2
P10	IO104RSB2
P11	IO97RSB2
P12	VMV1
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO88NDB1
R1	GEA1/IO144PDB3
R2	GEA0/IO144NDB3
R3	IO139RSB2
R4	GEC2/IO141RSB2
R5	IO132RSB2
R6	IO127RSB2
R7	IO121RSB2
R8	IO114RSB2
R9	IO109RSB2
R10	IO105RSB2
R11	IO98RSB2
R12	IO96RSB2
R13	GDB2/IO90RSB2
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO137RSB2
T3	GEB2/IO142RSB2
T4	IO134RSB2
T5	IO125RSB2
T6	IO123RSB2
T7	IO118RSB2
T8	IO115RSB2
T9	IO111RSB2
T10	IO106RSB2
T11	IO102RSB2
T12	GDC2/IO91RSB2

FG256	
Pin Number	A3P600 Function
T13	IO93RSB2
T14	GDA2/IO89RSB2
T15	TMS
T16	GND

FG484	
Pin Number	A3P1000 Function
R17	GDB1/IO112PPB1
R18	GDC1/IO111PDB1
R19	IO107NDB1
R20	VCC
R21	IO104NDB1
R22	IO105PDB1
T1	IO198PDB3
T2	IO198NDB3
T3	NC
T4	IO194PPB3
T5	IO192PPB3
T6	GEC1/IO190PPB3
T7	IO192NPB3
T8	GNDQ
T9	GEA2/IO187RSB2
T10	IO161RSB2
T11	IO155RSB2
T12	IO141RSB2
T13	IO129RSB2
T14	IO124RSB2
T15	GNDQ
T16	IO110PDB1
T17	VJTAG
T18	GDC0/IO111NDB1
T19	GDA1/IO113PDB1
T20	NC
T21	IO108PDB1
T22	IO105NDB1
U1	IO195PDB3
U2	IO195NDB3
U3	IO194NPB3
U4	GEB1/IO189PDB3
U5	GEB0/IO189NDB3
U6	VMV2
U7	IO179RSB2
U8	IO171RSB2

FG484	
Pin Number	A3P1000 Function
U9	IO165RSB2
U10	IO159RSB2
U11	IO151RSB2
U12	IO137RSB2
U13	IO134RSB2
U14	IO128RSB2
U15	VMV1
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO113NDB1
U20	NC
U21	IO108NDB1
U22	IO109PDB1
V1	NC
V2	NC
V3	GND
V4	GEA1/IO188PDB3
V5	GEA0/IO188NDB3
V6	IO184RSB2
V7	GEC2/IO185RSB2
V8	IO168RSB2
V9	IO163RSB2
V10	IO157RSB2
V11	IO149RSB2
V12	IO143RSB2
V13	IO138RSB2
V14	IO131RSB2
V15	IO125RSB2
V16	GDB2/IO115RSB2
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	IO109NDB1

FG484	
Pin Number	A3P1000 Function
W1	NC
W2	IO191PDB3
W3	NC
W4	GND
W5	IO183RSB2
W6	GEB2/IO186RSB2
W7	IO172RSB2
W8	IO170RSB2
W9	IO164RSB2
W10	IO158RSB2
W11	IO153RSB2
W12	IO142RSB2
W13	IO135RSB2
W14	IO130RSB2
W15	GDC2/IO116RSB2
W16	IO120RSB2
W17	GDA2/IO114RSB2
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	VCCIB3
Y2	IO191NDB3
Y3	NC
Y4	IO182RSB2
Y5	GND
Y6	IO177RSB2
Y7	IO174RSB2
Y8	VCC
Y9	VCC
Y10	IO154RSB2
Y11	IO148RSB2
Y12	IO140RSB2
Y13	NC
Y14	VCC

Revision	Changes	Page
Advance v0.3	The "PLL Macro" section was updated. EXTFB information was removed from this section.	2-15
	The CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT} was updated in Table 2-11 • ProASIC3 CCC/PLL Specification	2-29
	EXTFB was removed from Figure 2-27 • CCC/PLL Macro.	2-28
	Table 2-13 • ProASIC3 I/O Features was updated.	2-30
	The "Hot-Swap Support" section was updated.	2-33
	The "Cold-Sparing Support" section was updated.	2-34
	"Electrostatic Discharge (ESD) Protection" section was updated.	2-35
	The LVPECL specification in Table 2-43 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3 Devices was updated.	2-64
	In the Bank 1 area of Figure 2-72, VMV2 was changed to VMV1 and VCCIB2 was changed to VCC _I B1.	2-97
	The VJTAG and I/O pin descriptions were updated in the "Pin Descriptions" section.	2-50
	The "JTAG Pins" section was updated.	2-51
	"128-Bit AES Decryption" section was updated to include M7 device information.	2-53
	Table 3-6 was updated.	3-6
	Table 3-7 was updated.	3-6
	In Table 3-11, PAC4 was updated.	3-93-8
	Table 3-20 was updated.	3-20
	The note in Table 3-32 was updated.	3-27
	All Timing Characteristics tables were updated from LVTTTL to Register Delays	3-31 to 3-73
	The Timing Characteristics for RAM4K9, RAM512X18, and FIFO were updated.	3-85 to 3-90
	F_{TCKMAX} was updated in Table 3-110.	3-97
Advance v0.2	Figure 2-11 was updated.	2-9
	The "Clock Resources (VersaNets)" section was updated.	2-9
	The "VersaNet Global Networks and Spine Access" section was updated.	2-9
	The "PLL Macro" section was updated.	2-15
	Figure 2-27 was updated.	2-28
	Figure 2-20 was updated.	2-19
	Table 2-5 was updated.	2-25
	Table 2-6 was updated.	2-25
	The "FIFO Flag Usage Considerations" section was updated.	2-27
	Table 2-13 was updated.	2-30
	Figure 2-24 was updated.	2-31
	The "Cold-Sparing Support" section is new.	2-34