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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 36864 |
| Number of I/O | 87 |
| Number of Gates | 250000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 132-WFQFN |
| Supplier Device Package | 132-QFN (8x8) |
| Purchase URL | https://www.e-xfl.com/product-detail/microsemi/a3p250-qng132i |

0 – I/O is set to drive out logic Low

Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming

Z -Tristate: I/O is tristated

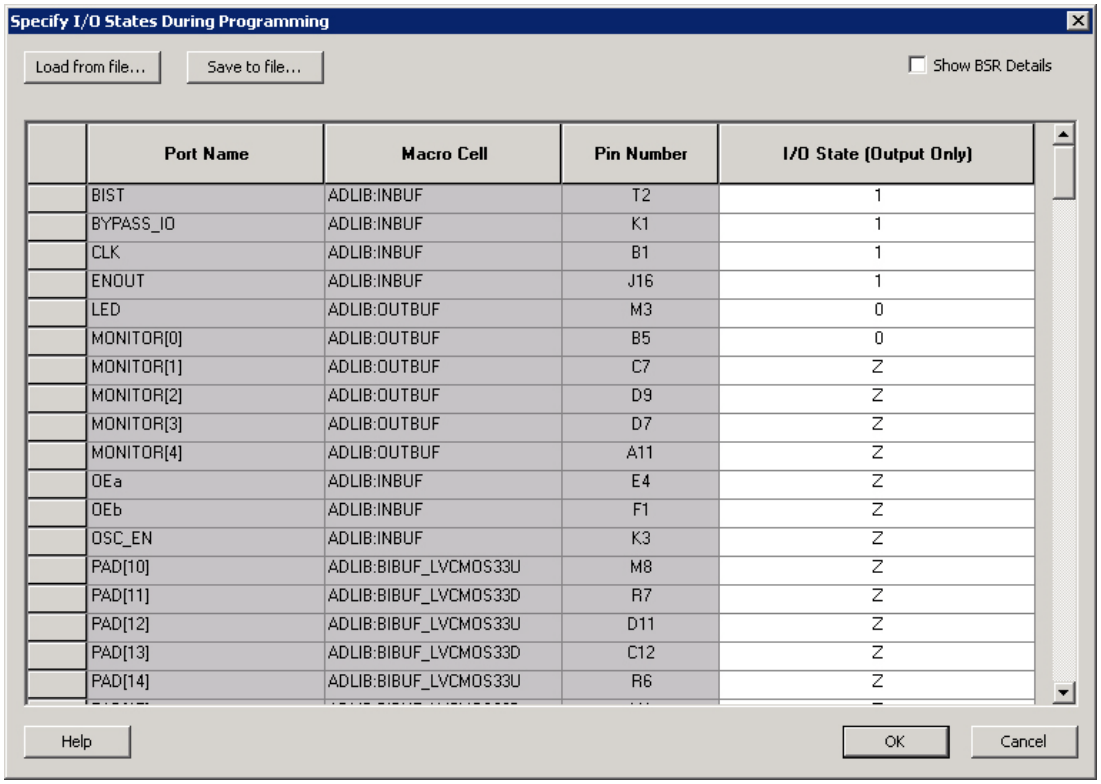



***Figure 1-4 •*** **I/O States During Programming Window**

6. Click OK to return to the FlashPoint – Programming File Generator window.

Note: I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

# 2 – ProASIC3 DC and Switching Characteristics

## General Specifications

### Operating Conditions

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 on page 2-2 is not implied.

***Table 2-1 •*** **Absolute Maximum Ratings**

| Symbol | Parameter | Limits | Units |
|---|---|---|---|
| VCC | DC core supply voltage | –0.3 to 1.65 | V |
| VJTAG | JTAG DC voltage | –0.3 to 3.75 | V |
| VPUMP | Programming voltage | –0.3 to 3.75 | V |
| VCCPLL | Analog power supply (PLL) | –0.3 to 1.65 | V |
| VCCI | DC I/O output buffer supply voltage | –0.3 to 3.75 | V |
| VMV | DC I/O input buffer supply voltage | –0.3 to 3.75 | V |
| VI | I/O input voltage | –0.3 V to 3.6 V<br>(when I/O hot insertion mode is enabled)<br>–0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower<br>(when I/O hot-insertion mode is disabled) | V |
| $T_{STG}$ [2] | Storage temperature | –65 to +150 | °C |
| $T_J$ [2] | Junction temperature | +125 | °C |

*Notes:*

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-4 on page 2-3.*
2. *VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information.*
3. *For flash programming and retention maximum limits, refer to Table 2-3 on page 2-3, and for recommended operating limits, refer to Table 2-2 on page 2-2.*

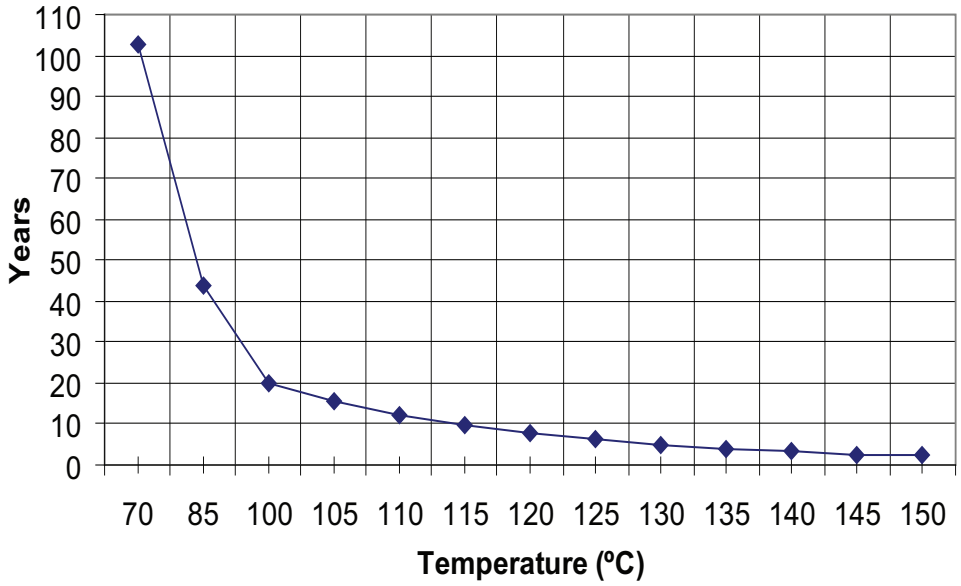
**Table 2-2 • Recommended Operating Conditions [1]**

| Symbol | Parameters [1] | | Commercial | Industrial | Units |
|---|---|---|---|---|---|
| $T_J$ | Junction temperature | | 0 to 85[2] | -40 to 100[2] | °C |
| VCC[3] | 1.5 V DC core supply voltage | | 1.425 to 1.575 | 1.425 to 1.575 | V |
| VJTAG | JTAG DC voltage | | 1.4 to 3.6 | 1.4 to 3.6 | V |
| VPUMP | Programming voltage | Programming Mode | 3.15 to 3.45 | 3.15 to 3.45 | V |
| | | Operation [4] | 0 to 3.6 | 0 to 3.6 | V |
| VCCPLL | Analog power supply (PLL) | | 1.425 to 1.575 | 1.425 to 1.575 | V |
| VCCI and VMV [5] | 1.5 V DC supply voltage | | 1.425 to 1.575 | 1.425 to 1.575 | V |
| | 1.8 V DC supply voltage | | 1.7 to 1.9 | 1.7 to 1.9 | V |
| | 2.5 V DC supply voltage | | 2.3 to 2.7 | 2.3 to 2.7 | V |
| | 3.3 V DC supply voltage | | 3.0 to 3.6 | 3.0 to 3.6 | V |
| | 3.3 V wide range DC supply voltage [6] | | 2.7 to 3.6 | 2.7 to 3.6 | V |
| | LVDS/B-LVDS/M-LVDS differential I/O | | 2.375 to 2.625 | 2.375 to 2.625 | V |
| | LVPECL differential I/O | | 3.0 to 3.6 | 3.0 to 3.6 | V |

*Notes:*

1. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
2. *Software Default Junction Temperature Range in the Libero® System-on-Chip (SoC) software is set to 0°C to +70°C for commercial, and -40°C to +85°C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microsemi recommends using custom settings for temperature range before running timing and power analysis tools. For more information regarding custom settings, refer to the New Project Dialog Box in the Libero SoC Online Help.*
3. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-18 on page 2-19.*
4. *VPUMP can be left floating during operation (not programming mode).*
5. *VMV and VCCI should be at the same voltage within a given I/O bank. VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information.*
6. *3.3 V wide range is compliant to the JESD8-B specification and supports 3.0 V VCCI operation.*

| Tj (°C) | HTR Lifetime (yrs) |
|---|---|
| 70 | 102.7 |
| 85 | 43.8 |
| 100 | 20.0 |
| 105 | 15.6 |
| 110 | 12.3 |
| 115 | 9.7 |
| 120 | 7.7 |
| 125 | 6.2 |
| 130 | 5.0 |
| 135 | 4.0 |
| 140 | 3.3 |
| 145 | 2.7 |
| 150 | 2.2 |




*Note: HTR time is the period during which you would not expect a verify failure due to flash cell leakage.*

***Figure 2-1 •*** **High-Temperature Data Retention (HTR)**

***Table 2-3 •*** **Flash Programming Limits – Retention, Storage and Operating Temperature[1]**

| Product Grade | Programming Cycles | Program Retention (biased/unbiased) | Maximum Storage Temperature $T_{STG}$ (°C) | Maximum Operating Junction Temperature $T_J$ (°C)[2] |
|---|---|---|---|---|
| Commercial | 500 | 20 years | 110 | 100 |
| Industrial | 500 | 20 years | 110 | 100 |

1. *This is a stress rating only; functional operation at any condition other than those indicated is not implied.*
2. *These limits apply for program/data retention only. Refer to Table 2-1 on page 2-1 and Table 2-2 for device operating conditions and absolute limits.*

***Table 2-4 •*** **Overshoot and Undershoot Limits [1]**

| VCCI and VMV | Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2] | Maximum Overshoot/ Undershoot[2] |
|---|---|---|
| 2.7 V or less | 10% | 1.4 V |
| | 5% | 1.49 V |
| 3 V | 10% | 1.1 V |
| | 5% | 1.19 V |
| 3.3 V | 10% | 0.79 V |
| | 5% | 0.88 V |
| 3.6 V | 10% | 0.45 V |
| | 5% | 0.54 V |

*Notes:*

1. *Based on reliability requirements at 85°C.*
2. *The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*
3. *This table does not provide PCI overshoot/undershoot limits.*

**Table 2-13 • Summary of I/O Output Buffer Power (Per Pin) – Default I/O Software Settings [1] Applicable to Standard I/O Banks**

| | $C_{LOAD}$ (pF) | VCCI (V) | Static Power PDC3 (mW) [2] | Dynamic Power PAC10 (µW/MHz) [3] |
|---|---|---|---|---|
| **Single-Ended** | | | | |
| 3.3 V LVTTL / 3.3 V LVCMOS | 35 | 3.3 | – | 431.08 |
| 3.3 V LVCMOS Wide Range[4] | 35 | 3.3 | – | 431.08 |
| 2.5 V LVCMOS | 35 | 2.5 | – | 247.36 |
| 1.8 V LVCMOS | 35 | 1.8 | – | 128.46 |
| 1.5 V LVCMOS (JESD8-11) | 35 | 1.5 | – | 89.46 |

*Notes:*

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *$P_{DC3}$ is the static power (where applicable) measured on VCCI.*
3. *$P_{AC10}$ is the total dynamic power measured on VCC and VCCI.*
4. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*

## Timing Characteristics

**Table 2-41 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**
**Applicable to Advanced I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.66 | 7.66 | 0.04 | 1.02 | 0.43 | 7.80 | 6.59 | 2.65 | 2.61 | 10.03 | 8.82 | ns |
| | –1 | 0.56 | 6.51 | 0.04 | 0.86 | 0.36 | 6.63 | 5.60 | 2.25 | 2.22 | 8.54 | 7.51 | ns |
| | –2 | 0.49 | 5.72 | 0.03 | 0.76 | 0.32 | 5.82 | 4.92 | 1.98 | 1.95 | 7.49 | 6.59 | ns |
| 4 mA | Std. | 0.66 | 7.66 | 0.04 | 1.02 | 0.43 | 7.80 | 6.59 | 2.65 | 2.61 | 10.03 | 8.82 | ns |
| | –1 | 0.56 | 6.51 | 0.04 | 0.86 | 0.36 | 6.63 | 5.60 | 2.25 | 2.22 | 8.54 | 7.51 | ns |
| | –2 | 0.49 | 5.72 | 0.03 | 0.76 | 0.32 | 5.82 | 4.92 | 1.98 | 1.95 | 7.49 | 6.59 | ns |
| 6 mA | Std. | 0.66 | 4.91 | 0.04 | 1.02 | 0.43 | 5.00 | 4.07 | 2.99 | 3.20 | 7.23 | 6.31 | ns |
| | –1 | 0.56 | 4.17 | 0.04 | 0.86 | 0.36 | 4.25 | 3.46 | 2.54 | 2.73 | 6.15 | 5.36 | ns |
| | –2 | 0.49 | 3.66 | 0.03 | 0.76 | 0.32 | 3.73 | 3.04 | 2.23 | 2.39 | 5.40 | 4.71 | ns |
| 8 mA | Std. | 0.66 | 4.91 | 0.04 | 1.02 | 0.43 | 5.00 | 4.07 | 2.99 | 3.20 | 7.23 | 6.31 | ns |
| | –1 | 0.56 | 4.17 | 0.04 | 0.86 | 0.36 | 4.25 | 3.46 | 2.54 | 2.73 | 6.15 | 5.36 | ns |
| | –2 | 0.49 | 3.66 | 0.03 | 0.76 | 0.32 | 3.73 | 3.04 | 2.23 | 2.39 | 5.40 | 4.71 | ns |
| 12 mA | Std. | 0.66 | 3.53 | 0.04 | 1.02 | 0.43 | 3.60 | 2.82 | 3.21 | 3.58 | 5.83 | 5.06 | ns |
| | –1 | 0.56 | 3.00 | 0.04 | 0.86 | 0.36 | 3.06 | 2.40 | 2.73 | 3.05 | 4.96 | 4.30 | ns |
| | –2 | 0.49 | 2.64 | 0.03 | 0.76 | 0.32 | 2.69 | 2.11 | 2.40 | 2.68 | 4.36 | 3.78 | ns |
| 16 mA | Std. | 0.66 | 3.33 | 0.04 | 1.02 | 0.43 | 3.39 | 2.56 | 3.26 | 3.68 | 5.63 | 4.80 | ns |
| | –1 | 0.56 | 2.83 | 0.04 | 0.86 | 0.36 | 2.89 | 2.18 | 2.77 | 3.13 | 4.79 | 4.08 | ns |
| | –2 | 0.49 | 2.49 | 0.03 | 0.76 | 0.32 | 2.53 | 1.91 | 2.44 | 2.75 | 4.20 | 3.58 | ns |
| 24 mA | Std. | 0.66 | 3.08 | 0.04 | 1.02 | 0.43 | 3.13 | 2.12 | 3.32 | 4.06 | 5.37 | 4.35 | ns |
| | –1 | 0.56 | 2.62 | 0.04 | 0.86 | 0.36 | 2.66 | 1.80 | 2.83 | 3.45 | 4.57 | 3.70 | ns |
| | –2 | 0.49 | 2.30 | 0.03 | 0.76 | 0.32 | 2.34 | 1.58 | 2.48 | 3.03 | 4.01 | 3.25 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

**Table 2-42 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**
**Applicable to Advanced I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.66 | 10.26 | 0.04 | 1.02 | 0.43 | 10.45 | 8.90 | 2.64 | 2.46 | 12.68 | 11.13 | ns |
| | –1 | 0.56 | 8.72 | 0.04 | 0.86 | 0.36 | 8.89 | 7.57 | 2.25 | 2.09 | 10.79 | 9.47 | ns |
| | –2 | 0.49 | 7.66 | 0.03 | 0.76 | 0.32 | 7.80 | 6.64 | 1.98 | 1.83 | 9.47 | 8.31 | ns |
| 4 mA | Std. | 0.66 | 10.26 | 0.04 | 1.02 | 0.43 | 10.45 | 8.90 | 2.64 | 2.46 | 12.68 | 11.13 | ns |
| | –1 | 0.56 | 8.72 | 0.04 | 0.86 | 0.36 | 8.89 | 7.57 | 2.25 | 2.09 | 10.79 | 9.47 | ns |
| | –2 | 0.49 | 7.66 | 0.03 | 0.76 | 0.32 | 7.80 | 6.64 | 1.98 | 1.83 | 9.47 | 8.31 | ns |
| 6 mA | Std. | 0.66 | 7.27 | 0.04 | 1.02 | 0.43 | 7.41 | 6.28 | 2.98 | 3.04 | 9.65 | 8.52 | ns |
| | –1 | 0.56 | 6.19 | 0.04 | 0.86 | 0.36 | 6.30 | 5.35 | 2.54 | 2.59 | 8.20 | 7.25 | ns |
| | –2 | 0.49 | 5.43 | 0.03 | 0.76 | 0.32 | 5.53 | 4.69 | 2.23 | 2.27 | 7.20 | 6.36 | ns |
| 8 mA | Std. | 0.66 | 7.27 | 0.04 | 1.02 | 0.43 | 7.41 | 6.28 | 2.98 | 3.04 | 9.65 | 8.52 | ns |
| | –1 | 0.56 | 6.19 | 0.04 | 0.86 | 0.36 | 6.30 | 5.35 | 2.54 | 2.59 | 8.20 | 7.25 | ns |
| | –2 | 0.49 | 5.43 | 0.03 | 0.76 | 0.32 | 5.53 | 4.69 | 2.23 | 2.27 | 7.20 | 6.36 | ns |
| 12 mA | Std. | 0.66 | 5.58 | 0.04 | 1.02 | 0.43 | 5.68 | 4.87 | 3.21 | 3.42 | 7.92 | 7.11 | ns |
| | –1 | 0.56 | 4.75 | 0.04 | 0.86 | 0.36 | 4.84 | 4.14 | 2.73 | 2.91 | 6.74 | 6.05 | ns |
| | –2 | 0.49 | 4.17 | 0.03 | 0.76 | 0.32 | 4.24 | 3.64 | 2.39 | 2.55 | 5.91 | 5.31 | ns |
| 16 mA | Std. | 0.66 | 5.21 | 0.04 | 1.02 | 0.43 | 5.30 | 4.56 | 3.26 | 3.51 | 7.54 | 6.80 | ns |
| | –1 | 0.56 | 4.43 | 0.04 | 0.86 | 0.36 | 4.51 | 3.88 | 2.77 | 2.99 | 6.41 | 5.79 | ns |
| | –2 | 0.49 | 3.89 | 0.03 | 0.76 | 0.32 | 3.96 | 3.41 | 2.43 | 2.62 | 5.63 | 5.08 | ns |
| 24 mA | Std. | 0.66 | 4.85 | 0.04 | 1.02 | 0.43 | 4.94 | 4.54 | 3.32 | 3.88 | 7.18 | 6.78 | ns |
| | –1 | 0.56 | 4.13 | 0.04 | 0.86 | 0.36 | 4.20 | 3.87 | 2.82 | 3.30 | 6.10 | 5.77 | ns |
| | –2 | 0.49 | 3.62 | 0.03 | 0.76 | 0.32 | 3.69 | 3.39 | 2.48 | 2.90 | 5.36 | 5.06 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

**Table 2-75 • 1.8 V LVCMOS Low Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**
**Applicable to Standard I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.66 | 15.01 | 0.04 | 1.20 | 0.43 | 13.15 | 15.01 | 1.99 | 1.99 | ns |
| | –1 | 0.56 | 12.77 | 0.04 | 1.02 | 0.36 | 11.19 | 12.77 | 1.70 | 1.70 | ns |
| | –2 | 0.49 | 11.21 | 0.03 | 0.90 | 0.32 | 9.82 | 11.21 | 1.49 | 1.49 | ns |
| 4 mA | Std. | 0.66 | 10.10 | 0.04 | 1.20 | 0.43 | 9.55 | 10.10 | 2.41 | 2.37 | ns |
| | –1 | 0.56 | 8.59 | 0.04 | 1.02 | 0.36 | 8.13 | 8.59 | 2.05 | 2.02 | ns |
| | –2 | 0.49 | 7.54 | 0.03 | 0.90 | 0.32 | 7.13 | 7.54 | 1.80 | 1.77 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

## 1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

**Table 2-76 • Minimum and Maximum DC Input and Output Levels**
**Applicable to Advanced I/O Banks**

| 1.5 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max., V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| 2 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.575 | 0.25 * VCCI | 0.75 * VCCI | 2 | 2 | 16 | 13 | 10 | 10 |
| 4 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.575 | 0.25 * VCCI | 0.75 * VCCI | 4 | 4 | 33 | 25 | 10 | 10 |
| 6 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.575 | 0.25 * VCCI | 0.75 * VCCI | 6 | 6 | 39 | 32 | 10 | 10 |
| 8 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.575 | 0.25 * VCCI | 0.75 * VCCI | 8 | 8 | 55 | 66 | 10 | 10 |
| 12 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.575 | 0.25 * VCCI | 0.75 * VCCI | 12 | 12 | 55 | 66 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

## Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

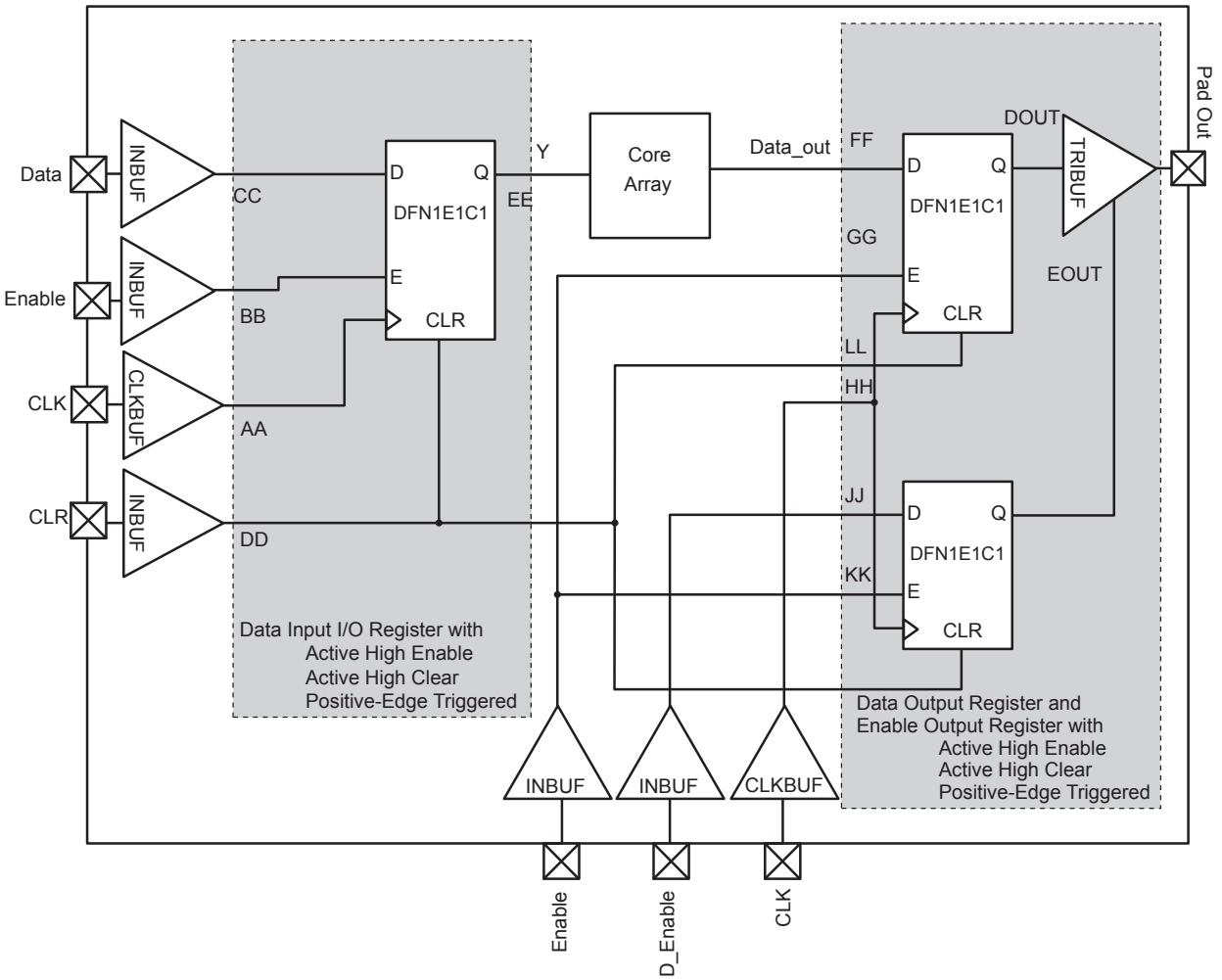



***Figure 2-16 •*** **Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

## Timing Characteristics

***Table 2-100* • Output Enable Register Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{OECLKQ}$ | Clock-to-Q of the Output Enable Register | 0.59 | 0.67 | 0.79 | ns |
| $t_{OESUD}$ | Data Setup Time for the Output Enable Register | 0.31 | 0.36 | 0.42 | ns |
| $t_{OEHD}$ | Data Hold Time for the Output Enable Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{OESUE}$ | Enable Setup Time for the Output Enable Register | 0.44 | 0.50 | 0.58 | ns |
| $t_{OEHE}$ | Enable Hold Time for the Output Enable Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{OECLR2Q}$ | Asynchronous Clear-to-Q of the Output Enable Register | 0.67 | 0.76 | 0.89 | ns |
| $t_{OEPRE2Q}$ | Asynchronous Preset-to-Q of the Output Enable Register | 0.67 | 0.76 | 0.89 | ns |
| $t_{OEREMCLR}$ | Asynchronous Clear Removal Time for the Output Enable Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Enable Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{OEREMPRE}$ | Asynchronous Preset Removal Time for the Output Enable Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{ORECPRE}$ | Asynchronous Preset Recovery Time for the Output Enable Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{OEWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Output Enable Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{OEWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Output Enable Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{OECKMPWH}$ | Clock Minimum Pulse Width High for the Output Enable Register | 0.36 | 0.41 | 0.48 | ns |
| $t_{OECKMPWL}$ | Clock Minimum Pulse Width Low for the Output Enable Register | 0.32 | 0.37 | 0.43 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-120* • A3P250 FIFO 512×8**
**Worst Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{ENS}$ | REN, WEN Setup Time | 3.75 | 4.27 | 5.02 | ns |
| $t_{ENH}$ | REN, WEN Hold Time | 0.00 | 0.00 | 0.00 | ns |
| $t_{BKS}$ | BLK Setup Time | 0.19 | 0.22 | 0.26 | ns |
| $t_{BKH}$ | BLK Hold Time | 0.00 | 0.00 | 0.00 | ns |
| $t_{DS}$ | Input Data (WD) Setup Time | 0.18 | 0.21 | 0.25 | ns |
| $t_{DH}$ | Input Data (WD) Hold Time | 0.00 | 0.00 | 0.00 | ns |
| $t_{CKQ1}$ | Clock High to New Data Valid on RD (flow-through) | 2.17 | 2.47 | 2.90 | ns |
| $t_{CKQ2}$ | Clock High to New Data Valid on RD (pipelined) | 0.94 | 1.07 | 1.26 | ns |
| $t_{RCKEF}$ | RCLK High to Empty Flag Valid | 1.72 | 1.96 | 2.30 | ns |
| $t_{WCKFF}$ | WCLK High to Full Flag Valid | 1.63 | 1.86 | 2.18 | ns |
| $t_{CKAF}$ | Clock High to Almost Empty/Full Flag Valid | 6.19 | 7.05 | 8.29 | ns |
| $t_{RSTFG}$ | RESET Low to Empty/Full Flag Valid | 1.69 | 1.93 | 2.27 | ns |
| $t_{RSTAF}$ | RESET Low to Almost Empty/Full Flag Valid | 6.13 | 6.98 | 8.20 | ns |
| $t_{RSTBQ}$ | RESET Low to Data Out Low on RD (flow-through) | 0.92 | 1.05 | 1.23 | ns |
| | RESET Low to Data Out Low on RD (pipelined) | 0.92 | 1.05 | 1.23 | ns |
| $t_{REMRSTB}$ | RESET Removal | 0.29 | 0.33 | 0.38 | ns |
| $t_{RECRSTB}$ | RESET Recovery | 1.50 | 1.71 | 2.01 | ns |
| $t_{MPWRSTB}$ | RESET Minimum Pulse Width | 0.21 | 0.24 | 0.29 | ns |
| $t_{CYC}$ | Clock Cycle Time | 3.23 | 3.68 | 4.32 | ns |
| $F_{MAX}$ | Maximum Frequency for FIFO | 310 | 272 | 231 | MHz |

### VJTAG JTAG Supply Voltage

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design.

If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a device is in a JTAG chain of interconnected boards, the board containing the device can be powered down, provided both VJTAG and VCC to the part remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

### VPUMP Programming Supply Voltage

ProASIC3 devices support single-voltage ISP of the configuration flash and FlashROM. For programming, VPUMP should be 3.3 V nominal. During normal device operation, VPUMP can be left floating or can be tied (pulled up) to any voltage between 0 V and the VPUMP maximum. Programming power supply voltage (VPUMP) range is listed in Table 2-2 on page 2-2.

When the VPUMP pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 µF and 0.33 µF capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

## User Pins

### I/O User Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to $V_{CCI}$. With $V_{CCI}$, VMV, and $V_{CC}$ supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

### GL Globals

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits in IGLOO and ProASIC3 Devices" chapter of the *ProASIC3 FPGA Fabric User's Guide*. All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

Refer to the I/O Structure section of the handbook for the device you are using for an explanation of the naming of global pins.

### FF Flash*Freeze Mode Activation Pin

Flash*Freeze is available on IGLOO, ProASIC3L, and RT ProASIC3 devices. It is not supported on ProASIC3/E devices. The FF pin is a dedicated input pin used to enter and exit Flash*Freeze mode. The FF pin is active-low, has the same characteristics as a single-ended I/O, and must meet the maximum rise and fall times. When Flash*Freeze

| QN132 | |
|---|---|
| Pin Number | A3P030 Function |
| A1 | IO01RSB1 |
| A2 | IO81RSB1 |
| A3 | NC |
| A4 | IO80RSB1 |
| A5 | GEC0/IO77RSB1 |
| A6 | NC |
| A7 | GEB0/IO75RSB1 |
| A8 | IO73RSB1 |
| A9 | NC |
| A10 | VCC |
| A11 | IO71RSB1 |
| A12 | IO68RSB1 |
| A13 | IO63RSB1 |
| A14 | IO60RSB1 |
| A15 | NC |
| A16 | IO59RSB1 |
| A17 | IO57RSB1 |
| A18 | VCC |
| A19 | IO54RSB1 |
| A20 | IO52RSB1 |
| A21 | IO49RSB1 |
| A22 | IO48RSB1 |
| A23 | IO47RSB1 |
| A24 | TDI |
| A25 | TRST |
| A26 | IO44RSB0 |
| A27 | NC |
| A28 | IO43RSB0 |
| A29 | IO42RSB0 |
| A30 | IO40RSB0 |
| A31 | IO39RSB0 |
| A32 | GDC0/IO36RSB0 |
| A33 | NC |
| A34 | VCC |
| A35 | IO34RSB0 |
| A36 | IO31RSB0 |

| QN132 | |
|---|---|
| Pin Number | A3P030 Function |
| A37 | IO26RSB0 |
| A38 | IO23RSB0 |
| A39 | NC |
| A40 | IO22RSB0 |
| A41 | IO20RSB0 |
| A42 | IO18RSB0 |
| A43 | VCC |
| A44 | IO15RSB0 |
| A45 | IO12RSB0 |
| A46 | IO10RSB0 |
| A47 | IO09RSB0 |
| A48 | IO06RSB0 |
| B1 | IO02RSB1 |
| B2 | IO82RSB1 |
| B3 | GND |
| B4 | IO79RSB1 |
| B5 | NC |
| B6 | GND |
| B7 | IO74RSB1 |
| B8 | NC |
| B9 | GND |
| B10 | IO70RSB1 |
| B11 | IO67RSB1 |
| B12 | IO64RSB1 |
| B13 | IO61RSB1 |
| B14 | GND |
| B15 | IO58RSB1 |
| B16 | IO56RSB1 |
| B17 | GND |
| B18 | IO53RSB1 |
| B19 | IO50RSB1 |
| B20 | GND |
| B21 | IO46RSB1 |
| B22 | TMS |
| B23 | TDO |
| B24 | IO45RSB0 |

| QN132 | |
|---|---|
| Pin Number | A3P030 Function |
| B25 | GND |
| B26 | NC |
| B27 | IO41RSB0 |
| B28 | GND |
| B29 | GDA0/IO37RSB0 |
| B30 | NC |
| B31 | GND |
| B32 | IO33RSB0 |
| B33 | IO30RSB0 |
| B34 | IO27RSB0 |
| B35 | IO24RSB0 |
| B36 | GND |
| B37 | IO21RSB0 |
| B38 | IO19RSB0 |
| B39 | GND |
| B40 | IO16RSB0 |
| B41 | IO13RSB0 |
| B42 | GND |
| B43 | IO08RSB0 |
| B44 | IO05RSB0 |
| C1 | IO03RSB1 |
| C2 | IO00RSB1 |
| C3 | NC |
| C4 | IO78RSB1 |
| C5 | GEA0/IO76RSB1 |
| C6 | NC |
| C7 | NC |
| C8 | VCCIB1 |
| C9 | IO69RSB1 |
| C10 | IO66RSB1 |
| C11 | IO65RSB1 |
| C12 | IO62RSB1 |
| C13 | NC |
| C14 | NC |
| C15 | IO55RSB1 |
| C16 | VCCIB1 |

| QN132 | |
|---|---|
| **Pin Number** | **A3P060 Function** |
| C17 | IO57RSB1 |
| C18 | NC |
| C19 | TCK |
| C20 | VMV1 |
| C21 | VPUMP |
| C22 | VJTAG |
| C23 | VCCIB0 |
| C24 | NC |
| C25 | NC |
| C26 | GCA1/IO42RSB0 |
| C27 | GCC0/IO39RSB0 |
| C28 | VCCIB0 |
| C29 | IO29RSB0 |
| C30 | GNDQ |
| C31 | GBA1/IO27RSB0 |
| C32 | GBB0/IO24RSB0 |
| C33 | VCC |
| C34 | IO19RSB0 |
| C35 | IO16RSB0 |
| C36 | IO13RSB0 |
| C37 | GAC1/IO10RSB0 |
| C38 | NC |
| C39 | GAA0/IO05RSB0 |
| C40 | VMV0 |
| D1 | GND |
| D2 | GND |
| D3 | GND |
| D4 | GND |

| QN132 | |
|---|---|
| **Pin Number** | **A3P250 Function** |
| C17 | IO74RSB2 |
| C18 | VCCIB2 |
| C19 | TCK |
| C20 | VMV2 |
| C21 | VPUMP |
| C22 | VJTAG |
| C23 | VCCIB1 |
| C24 | IO53NSB1 |
| C25 | IO51NPB1 |
| C26 | GCA1/IO50PPB1 |
| C27 | GCC0/IO48NDB1 |
| C28 | VCCIB1 |
| C29 | IO42NDB1 |
| C30 | GNDQ |
| C31 | GBA1/IO40RSB0 |
| C32 | GBB0/IO37RSB0 |
| C33 | VCC |
| C34 | IO24RSB0 |
| C35 | IO19RSB0 |
| C36 | IO16RSB0 |
| C37 | IO10RSB0 |
| C38 | VCCIB0 |
| C39 | GAB1/IO03RSB0 |
| C40 | VMV0 |
| D1 | GND |
| D2 | GND |
| D3 | GND |
| D4 | GND |

| PQ208 | |
|---|---|
| Pin Number | A3P250 Function |
| 109 | TRST |
| 110 | VJTAG |
| 111 | GDA0/IO60VDB1 |
| 112 | GDA1/IO60UDB1 |
| 113 | GDB0/IO59VDB1 |
| 114 | GDB1/IO59UDB1 |
| 115 | GDC0/IO58VDB1 |
| 116 | GDC1/IO58UDB1 |
| 117 | IO57VDB1 |
| 118 | IO57UDB1 |
| 119 | IO56NDB1 |
| 120 | IO56PDB1 |
| 121 | IO55RSB1 |
| 122 | GND |
| 123 | VCCIB1 |
| 124 | NC |
| 125 | NC |
| 126 | VCC |
| 127 | IO53NDB1 |
| 128 | GCC2/IO53PDB1 |
| 129 | GCB2/IO52PSB1 |
| 130 | GND |
| 131 | GCA2/IO51PSB1 |
| 132 | GCA1/IO50PDB1 |
| 133 | GCA0/IO50NDB1 |
| 134 | GCB0/IO49NDB1 |
| 135 | GCB1/IO49PDB1 |
| 136 | GCC0/IO48NDB1 |
| 137 | GCC1/IO48PDB1 |
| 138 | IO47NDB1 |
| 139 | IO47PDB1 |
| 140 | VCCIB1 |
| 141 | GND |
| 142 | VCC |
| 143 | IO46RSB1 |
| 144 | IO45NDB1 |

| PQ208 | |
|---|---|
| Pin Number | A3P250 Function |
| 145 | IO45PDB1 |
| 146 | IO44NDB1 |
| 147 | IO44PDB1 |
| 148 | IO43NDB1 |
| 149 | GBC2/IO43PDB1 |
| 150 | IO42NDB1 |
| 151 | GBB2/IO42PDB1 |
| 152 | IO41NDB1 |
| 153 | GBA2/IO41PDB1 |
| 154 | VMV1 |
| 155 | GNDQ |
| 156 | GND |
| 157 | NC |
| 158 | GBA1/IO40RSB0 |
| 159 | GBA0/IO39RSB0 |
| 160 | GBB1/IO38RSB0 |
| 161 | GBB0/IO37RSB0 |
| 162 | GND |
| 163 | GBC1/IO36RSB0 |
| 164 | GBC0/IO35RSB0 |
| 165 | IO34RSB0 |
| 166 | IO33RSB0 |
| 167 | IO32RSB0 |
| 168 | IO31RSB0 |
| 169 | IO30RSB0 |
| 170 | VCCIB0 |
| 171 | VCC |
| 172 | IO29RSB0 |
| 173 | IO28RSB0 |
| 174 | IO27RSB0 |
| 175 | IO26RSB0 |
| 176 | IO25RSB0 |
| 177 | IO24RSB0 |
| 178 | GND |
| 179 | IO23RSB0 |
| 180 | IO22RSB0 |

| PQ208 | |
|---|---|
| Pin Number | A3P250 Function |
| 181 | IO21RSB0 |
| 182 | IO20RSB0 |
| 183 | IO19RSB0 |
| 184 | IO18RSB0 |
| 185 | IO17RSB0 |
| 186 | VCCIB0 |
| 187 | VCC |
| 188 | IO16RSB0 |
| 189 | IO15RSB0 |
| 190 | IO14RSB0 |
| 191 | IO13RSB0 |
| 192 | IO12RSB0 |
| 193 | IO11RSB0 |
| 194 | IO10RSB0 |
| 195 | GND |
| 196 | IO09RSB0 |
| 197 | IO08RSB0 |
| 198 | IO07RSB0 |
| 199 | IO06RSB0 |
| 200 | VCCIB0 |
| 201 | GAC1/IO05RSB0 |
| 202 | GAC0/IO04RSB0 |
| 203 | GAB1/IO03RSB0 |
| 204 | GAB0/IO02RSB0 |
| 205 | GAA1/IO01RSB0 |
| 206 | GAA0/IO00RSB0 |
| 207 | GNDQ |
| 208 | VMV0 |

| PQ208 | |
|---|---|
| Pin Number | A3P400 Function |
| 109 | TRST |
| 110 | VJTAG |
| 111 | GDA0/IO79VDB1 |
| 112 | GDA1/IO79UDB1 |
| 113 | GDB0/IO78VDB1 |
| 114 | GDB1/IO78UDB1 |
| 115 | GDC0/IO77VDB1 |
| 116 | GDC1/IO77UDB1 |
| 117 | IO76VDB1 |
| 118 | IO76UDB1 |
| 119 | IO75NDB1 |
| 120 | IO75PDB1 |
| 121 | IO74RSB1 |
| 122 | GND |
| 123 | VCCIB1 |
| 124 | NC |
| 125 | NC |
| 126 | VCC |
| 127 | IO72NDB1 |
| 128 | GCC2/IO72PDB1 |
| 129 | GCB2/IO71PSB1 |
| 130 | GND |
| 131 | GCA2/IO70PSB1 |
| 132 | GCA1/IO69PDB1 |
| 133 | GCA0/IO69NDB1 |
| 134 | GCB0/IO68NDB1 |
| 135 | GCB1/IO68PDB1 |
| 136 | GCC0/IO67NDB1 |
| 137 | GCC1/IO67PDB1 |
| 138 | IO66NDB1 |
| 139 | IO66PDB1 |
| 140 | VCCIB1 |
| 141 | GND |
| 142 | VCC |
| 143 | IO65RSB1 |
| 144 | IO64NDB1 |

| PQ208 | |
|---|---|
| Pin Number | A3P400 Function |
| 145 | IO64PDB1 |
| 146 | IO63NDB1 |
| 147 | IO63PDB1 |
| 148 | IO62NDB1 |
| 149 | GBC2/IO62PDB1 |
| 150 | IO61NDB1 |
| 151 | GBB2/IO61PDB1 |
| 152 | IO60NDB1 |
| 153 | GBA2/IO60PDB1 |
| 154 | VMV1 |
| 155 | GNDQ |
| 156 | GND |
| 157 | VMV0 |
| 158 | GBA1/IO59RSB0 |
| 159 | GBA0/IO58RSB0 |
| 160 | GBB1/IO57RSB0 |
| 161 | GBB0/IO56RSB0 |
| 162 | GND |
| 163 | GBC1/IO55RSB0 |
| 164 | GBC0/IO54RSB0 |
| 165 | IO52RSB0 |
| 166 | IO49RSB0 |
| 167 | IO46RSB0 |
| 168 | IO43RSB0 |
| 169 | IO40RSB0 |
| 170 | VCCIB0 |
| 171 | VCC |
| 172 | IO36RSB0 |
| 173 | IO35RSB0 |
| 174 | IO34RSB0 |
| 175 | IO33RSB0 |
| 176 | IO32RSB0 |
| 177 | IO31RSB0 |
| 178 | GND |
| 179 | IO29RSB0 |
| 180 | IO28RSB0 |

| PQ208 | |
|---|---|
| Pin Number | A3P400 Function |
| 181 | IO27RSB0 |
| 182 | IO26RSB0 |
| 183 | IO25RSB0 |
| 184 | IO24RSB0 |
| 185 | IO23RSB0 |
| 186 | VCCIB0 |
| 187 | VCC |
| 188 | IO21RSB0 |
| 189 | IO20RSB0 |
| 190 | IO19RSB0 |
| 191 | IO18RSB0 |
| 192 | IO17RSB0 |
| 193 | IO16RSB0 |
| 194 | IO15RSB0 |
| 195 | GND |
| 196 | IO13RSB0 |
| 197 | IO11RSB0 |
| 198 | IO09RSB0 |
| 199 | IO07RSB0 |
| 200 | VCCIB0 |
| 201 | GAC1/IO05RSB0 |
| 202 | GAC0/IO04RSB0 |
| 203 | GAB1/IO03RSB0 |
| 204 | GAB0/IO02RSB0 |
| 205 | GAA1/IO01RSB0 |
| 206 | GAA0/IO00RSB0 |
| 207 | GNDQ |
| 208 | VMV0 |

| FG144 | |
|---|---|
| **Pin Number** | **A3P1000 Function** |
| A1 | GNDQ |
| A2 | VMV0 |
| A3 | GAB0/IO02RSB0 |
| A4 | GAB1/IO03RSB0 |
| A5 | IO10RSB0 |
| A6 | GND |
| A7 | IO44RSB0 |
| A8 | VCC |
| A9 | IO69RSB0 |
| A10 | GBA0/IO76RSB0 |
| A11 | GBA1/IO77RSB0 |
| A12 | GNDQ |
| B1 | GAB2/IO224PDB3 |
| B2 | GND |
| B3 | GAA0/IO00RSB0 |
| B4 | GAA1/IO01RSB0 |
| B5 | IO13RSB0 |
| B6 | IO26RSB0 |
| B7 | IO35RSB0 |
| B8 | IO60RSB0 |
| B9 | GBB0/IO74RSB0 |
| B10 | GBB1/IO75RSB0 |
| B11 | GND |
| B12 | VMV1 |
| C1 | IO224NDB3 |
| C2 | GFA2/IO206PPB3 |
| C3 | GAC2/IO223PDB3 |
| C4 | VCC |
| C5 | IO16RSB0 |
| C6 | IO29RSB0 |
| C7 | IO32RSB0 |
| C8 | IO63RSB0 |
| C9 | IO66RSB0 |
| C10 | GBA2/IO78PDB1 |
| C11 | IO78NDB1 |
| C12 | GBC2/IO80PPB1 |

| FG144 | |
|---|---|
| **Pin Number** | **A3P1000 Function** |
| D1 | IO213PDB3 |
| D2 | IO213NDB3 |
| D3 | IO223NDB3 |
| D4 | GAA2/IO225PPB3 |
| D5 | GAC0/IO04RSB0 |
| D6 | GAC1/IO05RSB0 |
| D7 | GBC0/IO72RSB0 |
| D8 | GBC1/IO73RSB0 |
| D9 | GBB2/IO79PDB1 |
| D10 | IO79NDB1 |
| D11 | IO80NPB1 |
| D12 | GCB1/IO92PPB1 |
| E1 | VCC |
| E2 | GFC0/IO209NDB3 |
| E3 | GFC1/IO209PDB3 |
| E4 | VCCIB3 |
| E5 | IO225NPB3 |
| E6 | VCCIB0 |
| E7 | VCCIB0 |
| E8 | GCC1/IO91PDB1 |
| E9 | VCCIB1 |
| E10 | VCC |
| E11 | GCA0/IO93NDB1 |
| E12 | IO94NDB1 |
| F1 | GFB0/IO208NPB3 |
| F2 | VCOMPLF |
| F3 | GFB1/IO208PPB3 |
| F4 | IO206NPB3 |
| F5 | GND |
| F6 | GND |
| F7 | GND |
| F8 | GCC0/IO91NDB1 |
| F9 | GCB0/IO92NPB1 |
| F10 | GND |
| F11 | GCA1/IO93PDB1 |
| F12 | GCA2/IO94PDB1 |

| FG144 | |
|---|---|
| **Pin Number** | **A3P1000 Function** |
| G1 | GFA1/IO207PPB3 |
| G2 | GND |
| G3 | VCCPLF |
| G4 | GFA0/IO207NPB3 |
| G5 | GND |
| G6 | GND |
| G7 | GND |
| G8 | GDC1/IO111PPB1 |
| G9 | IO96NDB1 |
| G10 | GCC2/IO96PDB1 |
| G11 | IO95NDB1 |
| G12 | GCB2/IO95PDB1 |
| H1 | VCC |
| H2 | GFB2/IO205PDB3 |
| H3 | GFC2/IO204PSB3 |
| H4 | GEC1/IO190PDB3 |
| H5 | VCC |
| H6 | IO105PDB1 |
| H7 | IO105NDB1 |
| H8 | GDB2/IO115RSB2 |
| H9 | GDC0/IO111NPB1 |
| H10 | VCCIB1 |
| H11 | IO101PSB1 |
| H12 | VCC |
| J1 | GEB1/IO189PDB3 |
| J2 | IO205NDB3 |
| J3 | VCCIB3 |
| J4 | GEC0/IO190NDB3 |
| J5 | IO160RSB2 |
| J6 | IO157RSB2 |
| J7 | VCC |
| J8 | TCK |
| J9 | GDA2/IO114RSB2 |
| J10 | TDO |
| J11 | GDA1/IO113PDB1 |
| J12 | GDB1/IO112PDB1 |

| Revision | Changes | Page |
|---|---|---|
| **Revision 2 (cont'd)** | The "ProASIC3 FPGAs Package Sizes Dimensions" table is new. | III |
| | In the "ProASIC3 Ordering Information", the QN package measurements were updated to include both 0.4 mm and 0.5 mm. | IV |
| | In the General Description section the number of I/Os was updated from 288 to 300. | 1-1 |
| Packaging v1.2 | The "QN68 – Bottom View" section is new. | 4-3 |
| **Revision 1 (Feb 2008)**<br>DC and Switching Characteristics v1.1 | In Table 2-2 • Recommended Operating Conditions 1, $T_J$ was listed in the symbol column and was incorrect. It was corrected and changed to $T_A$. | 2-2 |
| | In Table 2-3 • Flash Programming Limits – Retention, Storage and Operating Temperature, Maximum Operating Junction Temperature was changed from 110°C to 100°C for both commercial and industrial grades. | 2-3 |
| | The "PLL Behavior at Brownout Condition" section is new. | 2-4 |
| | In the "PLL Contribution—PPLL" section, the following was deleted:<br>FCLKIN is the input clock frequency. | 2-14 |
| | In Table 2-21 • Summary of Maximum and Minimum DC Input Levels, the note was incorrect. It previously said $T_J$ and it was corrected and changed to $T_A$. | 2-21 |
| | In Table 2-115 • ProASIC3 CCC/PLL Specification, the SCLK parameter and note 1 are new. | 2-90 |
| | Table 2-125 • JTAG 1532 was populated with the parameter data, which was not in the previous version of the document. | 2-108 |
| Packaging v1.1 | In the "VQ100" A3P030 pin table, the function of pin 63 was incorrect and changed from IO39RSB0 to GDB0/IO38RSB0. | 4-19 |
| **Revision 0 (Jan 2008)** | This document was previously in datasheet v2.2. As a result of moving to the handbook format, Actel has restarted the version numbers. | N/A |
| v2.2<br>(July 2007) | The M7 and M1 device part numbers have been updated in Table 1 • ProASIC3 Product Family, "I/Os Per Package", "Automotive ProASIC3 Ordering Information", "Temperature Grade Offerings", and "Speed Grade and Temperature Grade Matrix". | i, ii, iii, iii, iv |
| | The words "ambient temperature" were added to the temperature range in the "Automotive ProASIC3 Ordering Information", "Temperature Grade Offerings", and "Speed Grade and Temperature Grade Matrix" sections. | iii, iv |
| | The $T_J$ parameter in Table 3-2 • Recommended Operating Conditions was changed to $T_A$, ambient temperature, and table notes 4–6 were added. | 3-2 |
| v2.1<br>(May 2007) | In the "Clock Conditioning Circuit (CCC) and PLL" section, the Wide Input Frequency Range (1.5 MHz to 200 MHz) was changed to (1.5 MHz to 350 MHz). | i |
| | The "Clock Conditioning Circuit (CCC) and PLL" section was updated. | i |
| | In the "I/Os Per Package" section, the A3P030, A3P060, A3P125, ACP250, and A3P600 device I/Os were updated. | ii |
| | Table 3-5 • Package Thermal Resistivities was updated with A3P1000 information. The note below the table is also new. | 3-5 |

| Revision | Changes | Page |
|---|---|---|
| Advance v0.3 | The "PLL Macro" section was updated. EXTFB information was removed from this section. | 2-15 |
| | The CCC Output Peak-to-Peak Period Jitter $F_{CCC\_OUT}$ was updated in Table 2-11 • ProASIC3 CCC/PLL Specification | 2-29 |
| | EXTFB was removed from Figure 2-27 • CCC/PLL Macro. | 2-28 |
| | Table 2-13 • ProASIC3 I/O Features was updated. | 2-30 |
| | The "Hot-Swap Support" section was updated. | 2-33 |
| | The "Cold-Sparing Support" section was updated. | 2-34 |
| | "Electrostatic Discharge (ESD) Protection" section was updated. | 2-35 |
| | The LVPECL specification in Table 2-43 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3 Devices was updated. | 2-64 |
| | In the Bank 1 area of Figure 2-72, VMV2 was changed to VMV1 and VCCIB2 was changed to $VCC_I B1$. | 2-97 |
| | The VJTAG and I/O pin descriptions were updated in the "Pin Descriptions" section. | 2-50 |
| | The "JTAG Pins" section was updated. | 2-51 |
| | "128-Bit AES Decryption" section was updated to include M7 device information. | 2-53 |
| | Table 3-6 was updated. | 3-6 |
| | Table 3-7 was updated. | 3-6 |
| | In Table 3-11, PAC4 was updated. | 3-93-8 |
| | Table 3-20 was updated. | 3-20 |
| | The note in Table 3-32 was updated. | 3-27 |
| | All Timing Characteristics tables were updated from LVTTL to Register Delays | 3-31 to 3-73 |
| | The Timing Characteristics for RAM4K9, RAM512X18, and FIFO were updated. | 3-85 to 3-90 |
| | $F_{TCKMAX}$ was updated in Table 3-110. | 3-97 |
| Advance v0.2 | Figure 2-11 was updated. | 2-9 |
| | The "Clock Resources (VersaNets)" section was updated. | 2-9 |
| | The "VersaNet Global Networks and Spine Access" section was updated. | 2-9 |
| | The "PLL Macro" section was updated. | 2-15 |
| | Figure 2-27 was updated. | 2-28 |
| | Figure 2-20 was updated. | 2-19 |
| | Table 2-5 was updated. | 2-25 |
| | Table 2-6 was updated. | 2-25 |
| | The "FIFO Flag Usage Considerations" section was updated. | 2-27 |
| | Table 2-13 was updated. | 2-30 |
| | Figure 2-24 was updated. | 2-31 |
| | The "Cold-Sparing Support" section is new. | 2-34 |