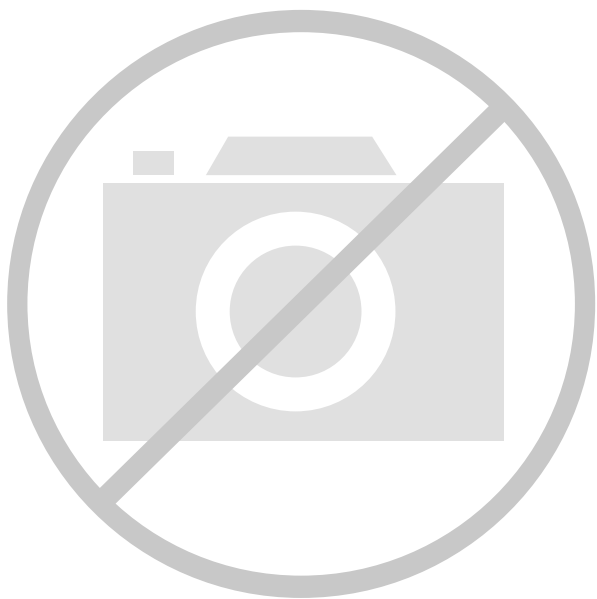




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	55296
Number of I/O	194
Number of Gates	400000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a3p400-2fgg484i

I/Os Per Package ¹

ProASIC3 Devices	A3P015 ²	A3P030	A3P060	A3P125	A3P250 ³		A3P400 ³		A3P600		A3P1000	
Cortex-M1 Devices					M1A3P250 ^{3,5}		M1A3P400 ³		M1A3P600		M1A3P1000	
Package	I/O Type											
	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O ⁴	Differential I/O Pairs	Single-Ended I/O ⁴	Differential I/O Pairs	Single-Ended I/O ⁴	Differential I/O Pairs	Single-Ended I/O ⁴	Differential I/O Pairs
QN48	–	34	–	–	–	–		–	–	–	–	–
QN68	49	49	–	–	–	–	–	–		–	–	–
QN132 ⁷	–	81	80	84	87	19	–	–		–	–	–
CS121	–	–	96	–	–	–	–	–	–	–	–	–
VQ100	–	77	71	71	68	13	–	–		–	–	–
TQ144	–	–	91	100	–	–	–	–	–	–	–	–
PQ208	–	–	–	133	151	34	151	34	154	35	154	35
FG144	–	–	96	97	97	24	97	25	97	25	97	25
FG256 ^{5,6}	–	–	–	–	157	38	178	38	177	43	177	44
FG484 ⁶	–	–	–	–	–	–	194	38	235	60	300	74

Notes:

1. When considering migrating your design to a lower- or higher-density device, refer to the [ProASIC3 FPGA Fabric User Guide](#) to ensure complying with design and board migration requirements.
2. A3P015 is not recommended for new designs.
3. For A3P250 and A3P400 devices, the maximum number of LVPECL pairs in east and west banks cannot exceed 15. Refer to the [ProASIC3 FPGA Fabric Users Guide](#) for position assignments of the 15 LVPECL pairs.
4. Each used differential I/O pair reduces the number of single-ended I/Os available by two.
5. The M1A3P250 device does not support FG256 package.
6. FG256 and FG484 are footprint-compatible packages.
7. Package not available.

Table 1 • ProASIC3 FPGAs Package Sizes Dimensions

Package	CS121	QN48	QN68	QN132 *	VQ100	TQ144	PQ208	FG144	FG256	FG484
Length × Width (mm × mm)	6 × 6	6 × 6	8 × 8	8 × 8	14 × 14	20 × 20	28 × 28	13 × 13	17 × 17	23 × 23
Nominal Area (mm ²)	36	36	64	64	196	400	784	169	289	529
Pitch (mm)	0.5	0.4	0.4	0.5	0.5	0.5	0.5	1.0	1.0	1.0
Height (mm)	0.99	0.90	0.90	0.75	1.00	1.40	3.40	1.45	1.60	2.23

Note: * Package not available

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-18 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings
 Applicable to Advanced I/O Banks

I/O Standard	Drive Strength	Equiv. Software Default Drive Strength Option ²	Slew Rate	VIL		VIH		VOL	VOH	IOL ¹ mA	IOH ¹ mA
				Min V	Max V	Min V	Max V	Max V	Min V		
3.3 V LVTTTL / 3.3 V LVC MOS	12 mA	12 mA	High	−0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVC MOS Wide Range ³	100 μ A	12 mA	High	−0.3	0.8	2	3.6	0.2	VCCI − 0.2	0.1	0.1
2.5 V LVC MOS	12 mA	12 mA	High	−0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8 V LVC MOS	12 mA	12 mA	High	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	12	12
1.5 V LVC MOS	12 mA	12 mA	High	−0.3	0.35 * VCCI	0.65 * VCCI	1.6	0.25 * VCCI	0.75 * VCCI	12	12
3.3 V PCI	Per PCI specifications										
3.3 V PCI-X	Per PCI-X specifications										

Notes:

1. Currents are measured at 85°C junction temperature.
2. 3.3 V LVC MOS wide range is applicable to 100 μ A drive strength only. The configuration will NOT operate at the equivalent software default drive strength. These values are for Normal Ranges ONLY.
3. All LVC MOS 3.3 V software macros support LVC MOS 3.3 V wide range as specified in the JESD-8B specification.

Table 2-30 • I/O Output Buffer Maximum Resistances¹
Applicable to Standard I/O Banks

Standard	Drive Strength	$R_{PULL-DOWN}$ (Ω) ²	$R_{PULL-UP}$ (Ω) ³
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
3.3 V LVCMOS Wide Range ⁴	100 μ A	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
1.5 V LVCMOS	2 mA	200	224

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. $R_{(PULL-DOWN-MAX)} = (VOL_{spec}) / IOL_{spec}$
3. $R_{(PULL-UP-MAX)} = (VCCI_{max} - VOH_{spec}) / IOH_{spec}$
4. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.

Table 2-31 • I/O Weak Pull-Up/Pull-Down Resistances
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

VCCI	$R_{(WEAK PULL-UP)}$ ¹ (Ω)		$R_{(WEAK PULL-DOWN)}$ ² (Ω)	
	Min	Max	Min	Max
3.3 V	10 k	45 k	10 k	45 k
3.3 V (wide range I/Os)	10 k	45 k	10 k	45 k
2.5 V	11 k	55 k	12 k	74 k
1.8 V	18 k	70 k	17 k	110 k
1.5 V	19 k	90 k	19 k	140 k

Notes:

1. $R_{(WEAK PULL-UP-MAX)} = (VCCI_{MAX} - VOH_{spec}) / I_{(WEAK PULL-UP-MIN)}$
2. $R_{(WEAK PULL-DOWN-MAX)} = (VOL_{spec}) / I_{(WEAK PULL-DOWN-MIN)}$

Table 2-54 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
Applicable to Standard I/O Banks

Drive Strength	Equiv. Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 μA	2 mA	Std.	0.60	10.93	0.04	1.52	0.43	10.93	9.46	3.20	3.32	ns
		–1	0.51	9.29	0.04	1.29	0.36	9.29	8.04	2.72	2.82	ns
		–2	0.45	8.16	0.03	1.13	0.32	8.16	7.06	2.39	2.48	ns
100 μA	4 mA	Std.	0.60	10.93	0.04	1.52	0.43	10.93	9.46	3.20	3.32	ns
		–1	0.51	9.29	0.04	1.29	0.36	9.29	8.04	2.72	2.82	ns
		–2	0.45	8.16	0.03	1.13	0.32	8.16	7.06	2.39	2.48	ns
100 μA	6 mA	Std.	0.60	6.82	0.04	1.52	0.43	6.82	5.70	3.70	4.16	ns
		–1	0.51	5.80	0.04	1.29	0.36	5.80	4.85	3.15	3.54	ns
		–2	0.45	5.09	0.03	1.13	0.32	5.09	4.25	2.77	3.11	ns
100 μA	8 mA	Std.	0.60	6.82	0.04	1.52	0.43	6.82	5.70	3.70	4.16	ns
		–1	0.51	5.80	0.04	1.29	0.36	5.80	4.85	3.15	3.54	ns
		–2	0.45	5.09	0.03	1.13	0.32	5.09	4.25	2.77	3.11	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. Software default selection highlighted in gray.
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-64 • 2.5 V LVCMOS High Slew

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
 Applicable to Standard I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.66	8.20	0.04	1.29	0.43	7.24	8.20	2.03	1.91	ns
	–1	0.56	6.98	0.04	1.10	0.36	6.16	6.98	1.73	1.62	ns
	–2	0.49	6.13	0.03	0.96	0.32	5.41	6.13	1.52	1.43	ns
4 mA	Std.	0.66	8.20	0.04	1.29	0.43	7.24	8.20	2.03	1.91	ns
	–1	0.56	6.98	0.04	1.10	0.36	6.16	6.98	1.73	1.62	ns
	–2	0.49	6.13	0.03	0.96	0.32	5.41	6.13	1.52	1.43	ns
6 mA	Std.	0.66	4.77	0.04	1.29	0.43	4.55	4.77	2.38	2.55	ns
	–1	0.56	4.05	0.04	1.10	0.36	3.87	4.05	2.03	2.17	ns
	–2	0.49	3.56	0.03	0.96	0.32	3.40	3.56	1.78	1.91	ns
8 mA	Std.	0.66	4.77	0.04	1.29	0.43	4.55	4.77	2.38	2.55	ns
	–1	0.56	4.05	0.04	1.10	0.36	3.87	4.05	2.03	2.17	ns
	–2	0.49	3.56	0.03	0.96	0.32	3.40	3.56	1.78	1.91	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-65 • 2.5 V LVCMOS Low Slew

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
 Applicable to Standard I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.66	11.00	0.04	1.29	0.43	10.37	11.00	2.03	1.83	ns
	–1	0.56	9.35	0.04	1.10	0.36	8.83	9.35	1.73	1.56	ns
	–2	0.49	8.21	0.03	0.96	0.32	7.75	8.21	1.52	1.37	ns
4 mA	Std.	0.66	11.00	0.04	1.29	0.43	10.37	11.00	2.03	1.83	ns
	–1	0.56	9.35	0.04	1.10	0.36	8.83	9.35	1.73	1.56	ns
	–2	0.49	8.21	0.03	0.96	0.32	7.75	8.21	1.52	1.37	ns
6 mA	Std.	0.66	7.50	0.04	1.29	0.43	7.36	7.50	2.39	2.46	ns
	–1	0.56	6.38	0.04	1.10	0.36	6.26	6.38	2.03	2.10	ns
	–2	0.49	5.60	0.03	0.96	0.32	5.49	5.60	1.78	1.84	ns
8 mA	Std.	0.66	7.50	0.04	1.29	0.43	7.36	7.50	2.39	2.46	ns
	–1	0.56	6.38	0.04	1.10	0.36	6.26	6.38	2.03	2.10	ns
	–2	0.49	5.60	0.03	0.96	0.32	5.49	5.60	1.78	1.84	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Timing Characteristics

Table 2-70 • 1.8 V LVCMOS High Slew

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 1.7\text{ V}$
 Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	11.86	0.04	1.22	0.43	9.14	11.86	2.77	1.66	11.37	14.10	ns
	–1	0.56	10.09	0.04	1.04	0.36	7.77	10.09	2.36	1.41	9.67	11.99	ns
	–2	0.49	8.86	0.03	0.91	0.32	6.82	8.86	2.07	1.24	8.49	10.53	ns
4 mA	Std.	0.66	6.91	0.04	1.22	0.43	5.86	6.91	3.22	2.84	8.10	9.15	ns
	–1	0.56	5.88	0.04	1.04	0.36	4.99	5.88	2.74	2.41	6.89	7.78	ns
	–2	0.49	5.16	0.03	0.91	0.32	4.38	5.16	2.41	2.12	6.05	6.83	ns
6 mA	Std.	0.66	4.45	0.04	1.22	0.43	4.18	4.45	3.53	3.38	6.42	6.68	ns
	–1	0.56	3.78	0.04	1.04	0.36	3.56	3.78	3.00	2.88	5.46	5.69	ns
	–2	0.49	3.32	0.03	0.91	0.32	3.12	3.32	2.64	2.53	4.79	4.99	ns
8 mA	Std.	0.66	3.92	0.04	1.22	0.43	3.93	3.92	3.60	3.52	6.16	6.16	ns
	–1	0.56	3.34	0.04	1.04	0.36	3.34	3.34	3.06	3.00	5.24	5.24	ns
	–2	0.49	2.93	0.03	0.91	0.32	2.93	2.93	2.69	2.63	4.60	4.60	ns
12 mA	Std.	0.66	3.53	0.04	1.22	0.43	3.60	3.04	3.70	4.08	5.84	5.28	ns
	–1	0.56	3.01	0.04	1.04	0.36	3.06	2.59	3.15	3.47	4.96	4.49	ns
	–2	0.49	2.64	0.03	0.91	0.32	2.69	2.27	2.76	3.05	4.36	3.94	ns
16 mA	Std.	0.66	3.53	0.04	1.22	0.43	3.60	3.04	3.70	4.08	5.84	5.28	ns
	–1	0.56	3.01	0.04	1.04	0.36	3.06	2.59	3.15	3.47	4.96	4.49	ns
	–2	0.49	2.64	0.03	0.91	0.32	2.69	2.27	2.76	3.05	4.36	3.94	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-97 • Parameter Definition and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	FF, HH
t_{OHD}	Data Hold Time for the Output Data Register	FF, HH
t_{OSUE}	Enable Setup Time for the Output Data Register	GG, HH
t_{OHE}	Enable Hold Time for the Output Data Register	GG, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	JJ, HH
t_{OEHD}	Data Hold Time for the Output Enable Register	JJ, HH
t_{OESUE}	Enable Setup Time for the Output Enable Register	KK, HH
t_{OEHE}	Enable Hold Time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t_{IHD}	Data Hold Time for the Input Data Register	CC, AA
t_{ISUE}	Enable Setup Time for the Input Data Register	BB, AA
t_{IHE}	Enable Hold Time for the Input Data Register	BB, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

Note: *See Figure 2-16 on page 2-71 for more information.

DDR Module Specifications

Input DDR Module

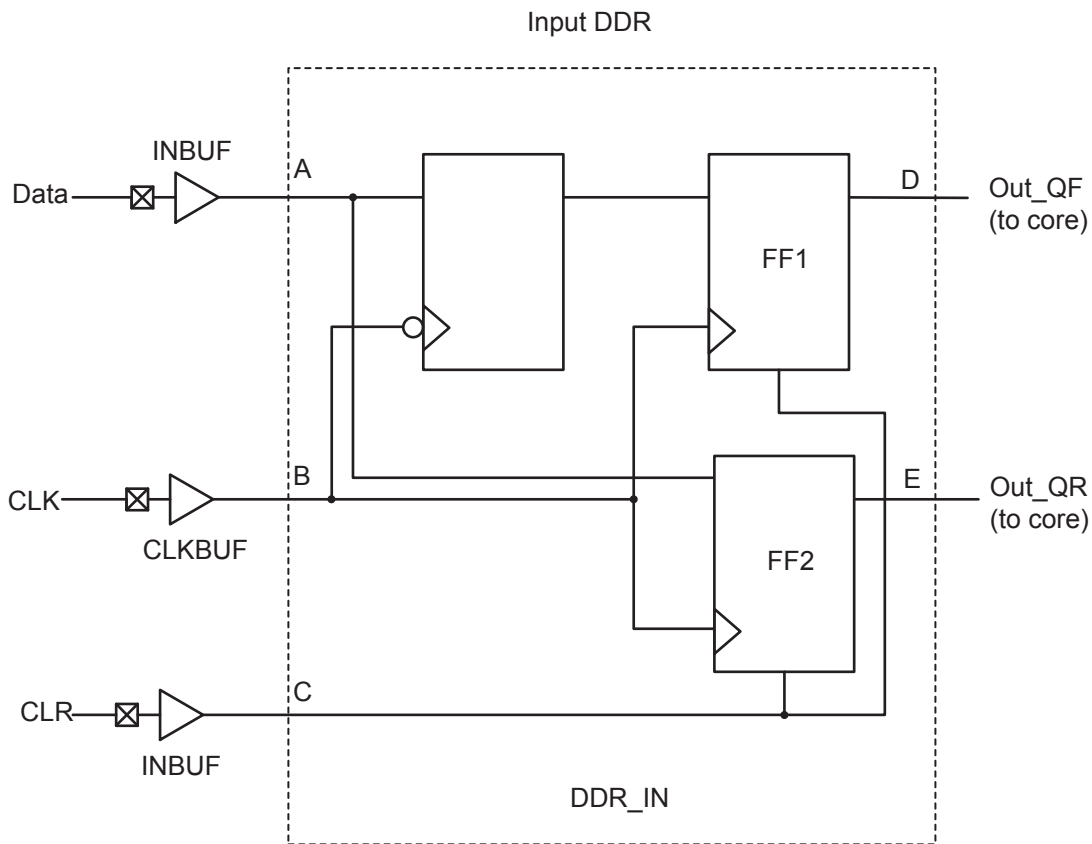


Figure 2-20 • Input DDR Timing Model

Table 2-101 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRCLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRCLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
$t_{DDR IHD}$	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

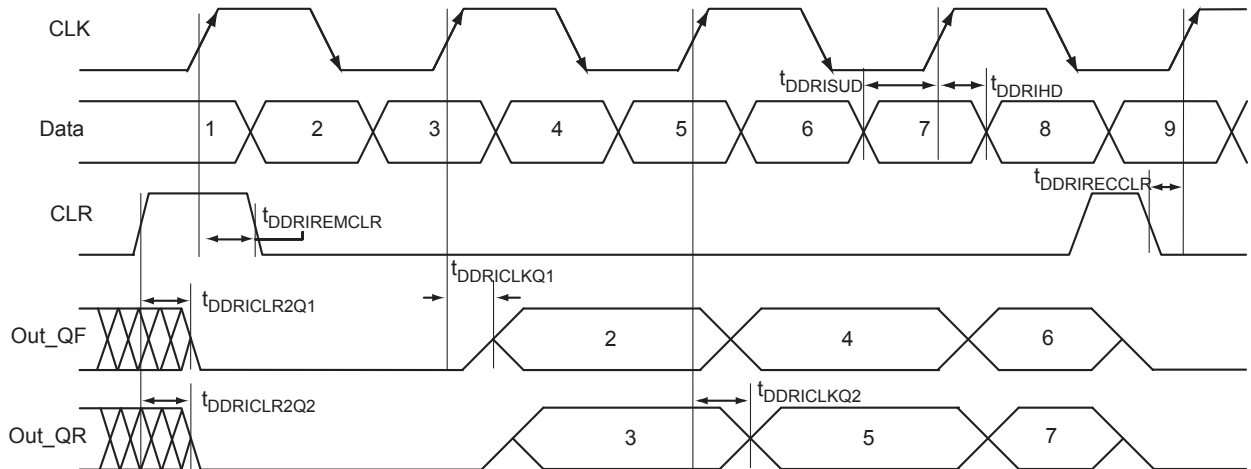


Figure 2-21 • Input DDR Timing Diagram

Timing Characteristics

Table 2-102 • Input DDR Propagation Delays

Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2	-1	Std.	Units
t_{DDRICKQ1}	Clock-to-Out Out_QR for Input DDR	0.27	0.31	0.37	ns
t_{DDRICKQ2}	Clock-to-Out Out_QF for Input DDR	0.39	0.44	0.52	ns
t_{DDRISUD}	Data Setup for Input DDR (Fall)	0.25	0.28	0.33	ns
	Data Setup for Input DDR (Rise)	0.25	0.28	0.33	ns
t_{DDRHD}	Data Hold for Input DDR (Fall)	0.00	0.00	0.00	ns
	Data Hold for Input DDR (Rise)	0.00	0.00	0.00	ns
$t_{\text{DDRCLR2Q1}}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.46	0.53	0.62	ns
$t_{\text{DDRCLR2Q2}}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.57	0.65	0.76	ns
$t_{\text{DDRREMCLR}}$	Asynchronous Clear Removal time for Input DDR	0.00	0.00	0.00	ns
$t_{\text{DDRRECCLR}}$	Asynchronous Clear Recovery time for Input DDR	0.22	0.25	0.30	ns
t_{DDRWCLR}	Asynchronous Clear Minimum Pulse Width for Input DDR	0.22	0.25	0.30	ns
$t_{\text{DDRICKMPWH}}$	Clock Minimum Pulse Width High for Input DDR	0.36	0.41	0.48	ns
$t_{\text{DDRICKMPWL}}$	Clock Minimum Pulse Width Low for Input DDR	0.32	0.37	0.43	ns
F_{DDRIMAX}	Maximum Frequency for Input DDR	350	309	263	MHz

Note: For specific junction temperature and voltage-supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The ProASIC3 library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the [Fusion](#), [IGLOO®/e](#), and [ProASIC3/E Macro Library Guide](#).

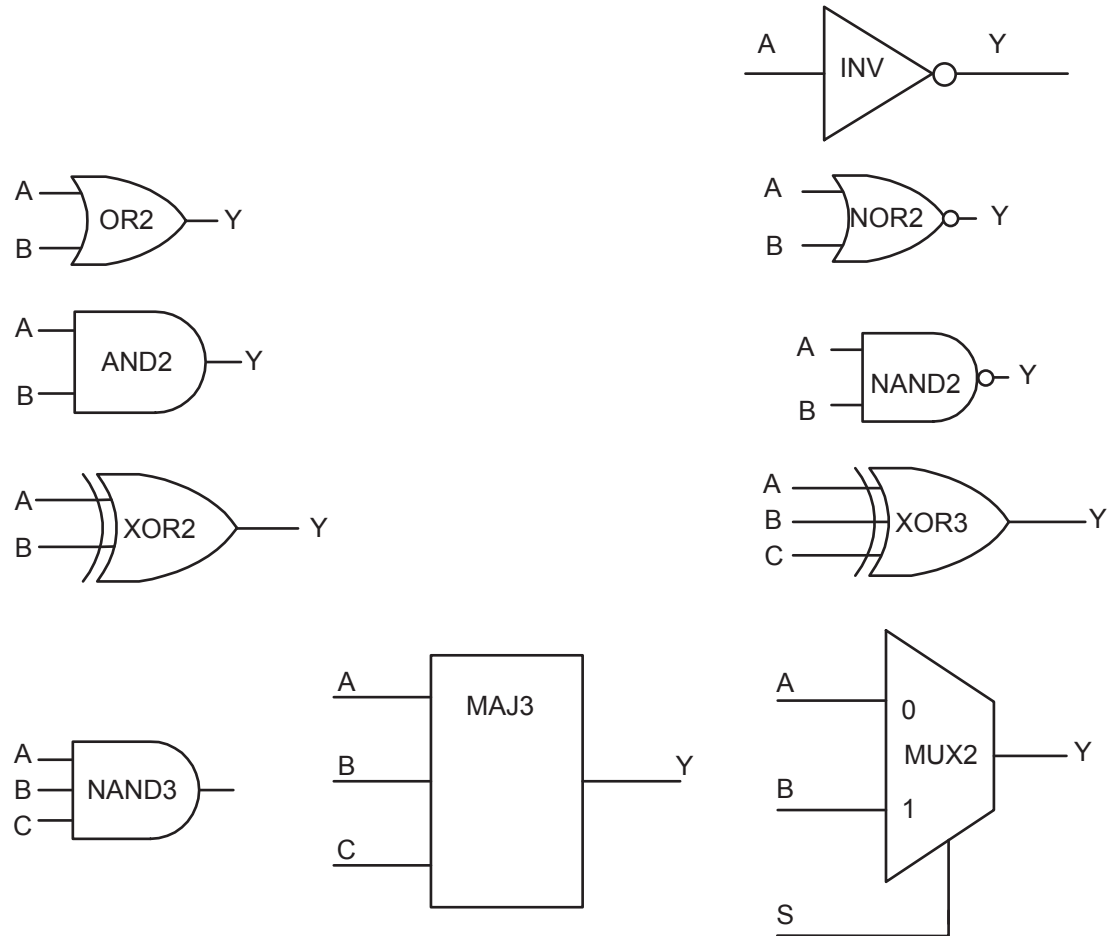


Figure 2-24 • Sample of Combinatorial Cells

Global Resource Characteristics

A3P250 Clock Tree Topology

Clock delays are device-specific. [Figure 2-28](#) is an example of a global tree used for clock routing. The global tree presented in [Figure 2-28](#) is driven by a CCC located on the west side of the A3P250 device. It is used to drive all D-flip-flops in the device.

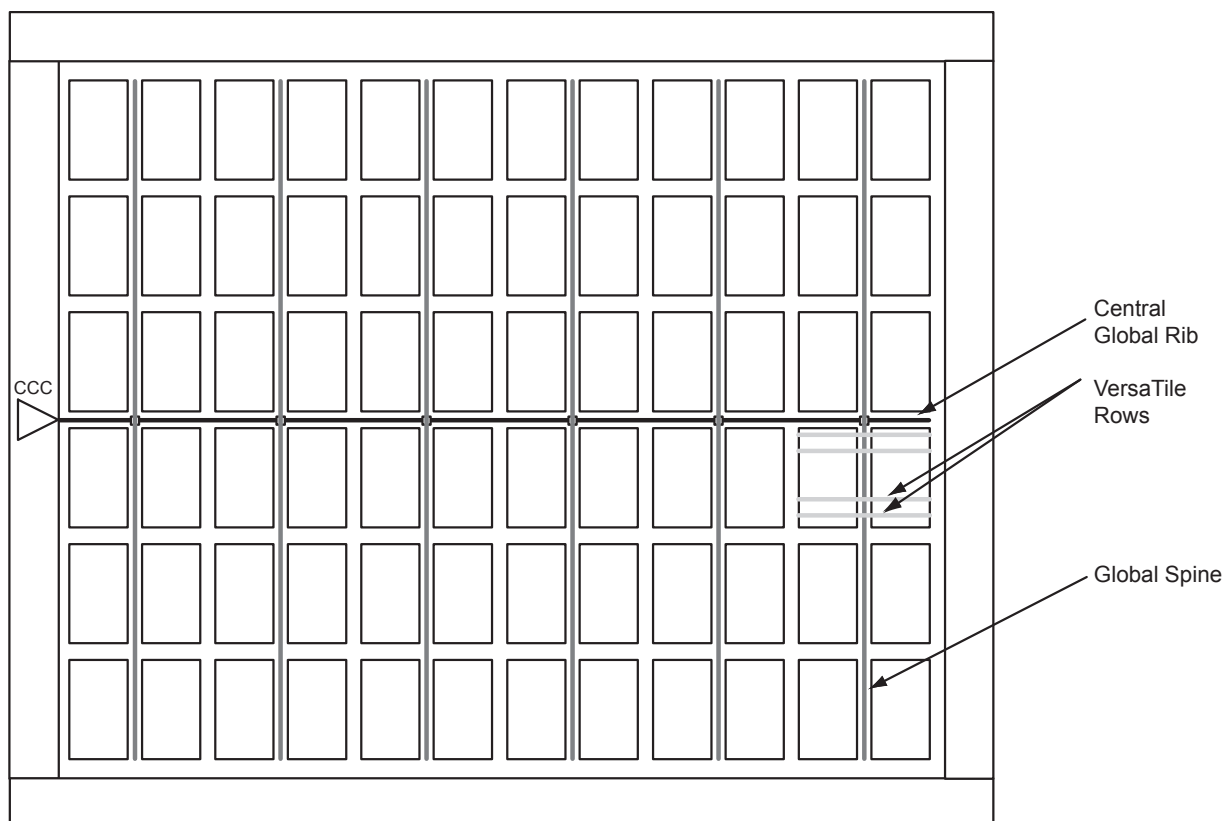


Figure 2-28 • Example of Global Tree Use in an A3P250 Device for Clock Routing

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard-dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the ["Clock Conditioning Circuits" section on page 2-90](#). [Table 2-108](#) to [Table 2-114 on page 2-89](#) present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500 Ω to 1 k Ω will satisfy the requirements.

Special Function Pins

NC **No Connect**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

DC **Do Not Connect**

This pin should not be connected to any signals on the PCB. These pins should be left unconnected.

Related Documents

User's Guides

ProASIC FPGA Fabric User's Guide

http://www.microsemi.com/soc/documents/PA3_UG.pdf

Packaging

The following documents provide packaging information and device selection for low power flash devices.

Product Catalog

http://www.microsemi.com/soc/documents/ProdCat_PIB.pdf

Lists devices currently recommended for new designs and the packages available for each member of the family. Use this document or the datasheet tables to determine the best package for your design, and which package drawing to use.

Package Mechanical Drawings

<http://www.microsemi.com/soc/documents/PckgMechDrwns.pdf>

This document contains the package mechanical drawings for all packages currently or previously supplied by Actel. Use the bookmarks to navigate to the package mechanical drawings.

Additional packaging materials are at <http://www.microsemi.com/products/solutions/package/docs.aspx>.

TQ144	
Pin Number	A3P125 Function
109	GBA1/IO40RSB0
110	GBA0/IO39RSB0
111	GBB1/IO38RSB0
112	GBB0/IO37RSB0
113	GBC1/IO36RSB0
114	GBC0/IO35RSB0
115	IO34RSB0
116	IO33RSB0
117	VCCIB0
118	GND
119	VCC
120	IO29RSB0
121	IO28RSB0
122	IO27RSB0
123	IO25RSB0
124	IO23RSB0
125	IO21RSB0
126	IO19RSB0
127	IO17RSB0
128	IO16RSB0
129	IO14RSB0
130	IO12RSB0
131	IO10RSB0
132	IO08RSB0
133	IO06RSB0
134	VCCIB0
135	GND
136	VCC
137	GAC1/IO05RSB0
138	GAC0/IO04RSB0
139	GAB1/IO03RSB0
140	GAB0/IO02RSB0
141	GAA1/IO01RSB0
142	GAA0/IO00RSB0
143	GNDQ
144	VMV0

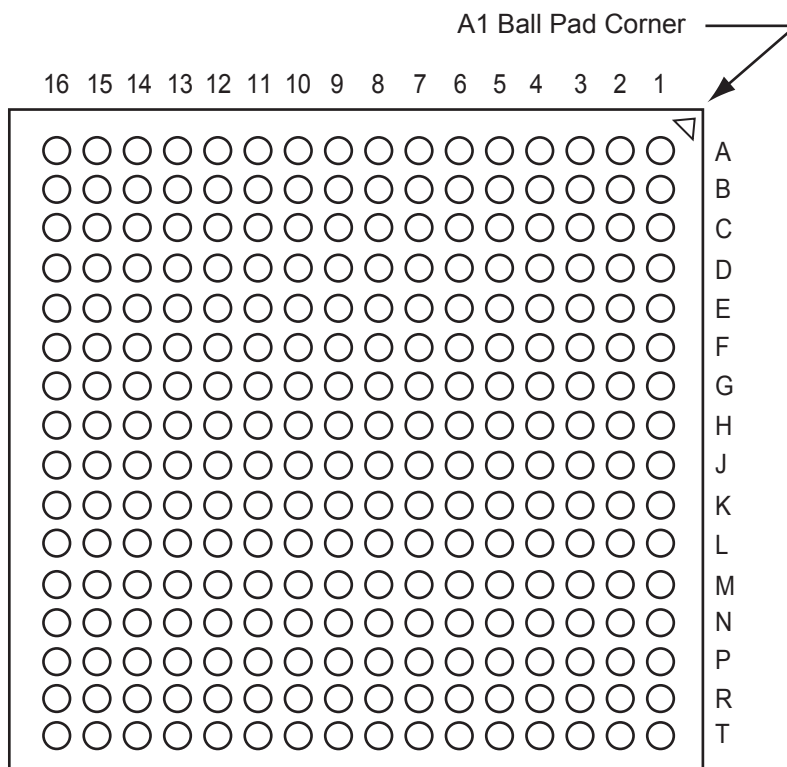
FG144	
Pin Number	A3P060 Function
K1	GEB0/IO74RSB1
K2	GEA1/IO73RSB1
K3	GEA0/IO72RSB1
K4	GEA2/IO71RSB1
K5	IO65RSB1
K6	IO64RSB1
K7	GND
K8	IO57RSB1
K9	GDC2/IO56RSB1
K10	GND
K11	GDA0/IO50RSB0
K12	GDB0/IO48RSB0
L1	GND
L2	VMV1
L3	GEB2/IO70RSB1
L4	IO67RSB1
L5	VCCIB1
L6	IO62RSB1
L7	IO59RSB1
L8	IO58RSB1
L9	TMS
L10	VJTAG
L11	VMV1
L12	TRST
M1	GNDQ
M2	GEC2/IO69RSB1
M3	IO68RSB1
M4	IO66RSB1
M5	IO63RSB1
M6	IO61RSB1
M7	IO60RSB1
M8	NC
M9	TDI
M10	VCCIB1
M11	VPUMP
M12	GNDQ

FG144	
Pin Number	A3P125 Function
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO11RSB0
A6	GND
A7	IO18RSB0
A8	VCC
A9	IO25RSB0
A10	GBA0/IO39RSB0
A11	GBA1/IO40RSB0
A12	GNDQ
B1	GAB2/IO69RSB1
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO08RSB0
B6	IO14RSB0
B7	IO19RSB0
B8	IO22RSB0
B9	GBB0/IO37RSB0
B10	GBB1/IO38RSB0
B11	GND
B12	VMV0
C1	IO132RSB1
C2	GFA2/IO120RSB1
C3	GAC2/IO131RSB1
C4	VCC
C5	IO10RSB0
C6	IO12RSB0
C7	IO21RSB0
C8	IO24RSB0
C9	IO27RSB0
C10	GBA2/IO41RSB0
C11	IO42RSB0
C12	GBC2/IO45RSB0

FG144	
Pin Number	A3P125 Function
D1	IO128RSB1
D2	IO129RSB1
D3	IO130RSB1
D4	GAA2/IO67RSB1
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO35RSB0
D8	GBC1/IO36RSB0
D9	GBB2/IO43RSB0
D10	IO28RSB0
D11	IO44RSB0
D12	GCB1/IO53RSB0
E1	VCC
E2	GFC0/IO125RSB1
E3	GFC1/IO126RSB1
E4	VCCIB1
E5	IO68RSB1
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO51RSB0
E9	VCCIB0
E10	VCC
E11	GCA0/IO56RSB0
E12	IO46RSB0
F1	GFB0/IO123RSB1
F2	VCOMPLF
F3	GFB1/IO124RSB1
F4	IO127RSB1
F5	GND
F6	GND
F7	GND
F8	GCC0/IO52RSB0
F9	GCB0/IO54RSB0
F10	GND
F11	GCA1/IO55RSB0
F12	GCA2/IO57RSB0

FG144	
Pin Number	A3P125 Function
G1	GFA1/IO121RSB1
G2	GND
G3	VCCPLF
G4	GFA0/IO122RSB1
G5	GND
G6	GND
G7	GND
G8	GDC1/IO61RSB0
G9	IO48RSB0
G10	GCC2/IO59RSB0
G11	IO47RSB0
G12	GCB2/IO58RSB0
H1	VCC
H2	GFB2/IO119RSB1
H3	GFC2/IO118RSB1
H4	GEC1/IO112RSB1
H5	VCC
H6	IO50RSB0
H7	IO60RSB0
H8	GDB2/IO71RSB1
H9	GDC0/IO62RSB0
H10	VCCIB0
H11	IO49RSB0
H12	VCC
J1	GEB1/IO110RSB1
J2	IO115RSB1
J3	VCCIB1
J4	GEC0/IO111RSB1
J5	IO116RSB1
J6	IO117RSB1
J7	VCC
J8	TCK
J9	GDA2/IO70RSB1
J10	TDO
J11	GDA1/IO65RSB0
J12	GDB1/IO63RSB0

FG256 – Bottom View



Note

For more information on package drawings, see [PD3068: Package Mechanical Drawings](#).

FG256	
Pin Number	A3P600 Function
P9	IO107RSB2
P10	IO104RSB2
P11	IO97RSB2
P12	VMV1
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO88NDB1
R1	GEA1/IO144PDB3
R2	GEA0/IO144NDB3
R3	IO139RSB2
R4	GEC2/IO141RSB2
R5	IO132RSB2
R6	IO127RSB2
R7	IO121RSB2
R8	IO114RSB2
R9	IO109RSB2
R10	IO105RSB2
R11	IO98RSB2
R12	IO96RSB2
R13	GDB2/IO90RSB2
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO137RSB2
T3	GEB2/IO142RSB2
T4	IO134RSB2
T5	IO125RSB2
T6	IO123RSB2
T7	IO118RSB2
T8	IO115RSB2
T9	IO111RSB2
T10	IO106RSB2
T11	IO102RSB2
T12	GDC2/IO91RSB2

FG256	
Pin Number	A3P600 Function
T13	IO93RSB2
T14	GDA2/IO89RSB2
T15	TMS
T16	GND

FG484	
Pin Number	A3P400 Function
R17	GDB1/IO78UPB1
R18	GDC1/IO77UDB1
R19	IO75NDB1
R20	VCC
R21	NC
R22	NC
T1	NC
T2	NC
T3	NC
T4	IO140NDB3
T5	IO138PPB3
T6	GEC1/IO137PPB3
T7	IO131RSB2
T8	GNDQ
T9	GEA2/IO134RSB2
T10	IO117RSB2
T11	IO111RSB2
T12	IO99RSB2
T13	IO94RSB2
T14	IO87RSB2
T15	GNDQ
T16	IO93RSB2
T17	VJTAG
T18	GDC0/IO77VDB1
T19	GDA1/IO79UDB1
T20	NC
T21	NC
T22	NC
U1	NC
U2	NC
U3	NC
U4	GEB1/IO136PDB3
U5	GEB0/IO136NDB3
U6	VMV2
U7	IO129RSB2
U8	IO128RSB2

FG484	
Pin Number	A3P400 Function
U9	IO122RSB2
U10	IO115RSB2
U11	IO110RSB2
U12	IO98RSB2
U13	IO95RSB2
U14	IO88RSB2
U15	IO84RSB2
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO79VDB1
U20	NC
U21	NC
U22	NC
V1	NC
V2	NC
V3	GND
V4	GEA1/IO135PDB3
V5	GEA0/IO135NDB3
V6	IO127RSB2
V7	GEC2/IO132RSB2
V8	IO123RSB2
V9	IO118RSB2
V10	IO112RSB2
V11	IO106RSB2
V12	IO100RSB2
V13	IO96RSB2
V14	IO89RSB2
V15	IO85RSB2
V16	GDB2/IO81RSB2
V17	TDI
V18	NC
V19	TDO
V20	GND
V21	NC
V22	NC

FG484	
Pin Number	A3P400 Function
W1	NC
W2	NC
W3	NC
W4	GND
W5	IO126RSB2
W6	GEB2/IO133RSB2
W7	IO124RSB2
W8	IO116RSB2
W9	IO113RSB2
W10	IO107RSB2
W11	IO105RSB2
W12	IO102RSB2
W13	IO97RSB2
W14	IO92RSB2
W15	GDC2/IO82RSB2
W16	IO86RSB2
W17	GDA2/IO80RSB2
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	VCCIB3
Y2	NC
Y3	NC
Y4	NC
Y5	GND
Y6	NC
Y7	NC
Y8	VCC
Y9	VCC
Y10	NC
Y11	NC
Y12	NC
Y13	NC
Y14	VCC

FG484	
Pin Number	A3P600 Function
Y15	VCC
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	VCCIB1
AA1	GND
AA2	VCCIB3
AA3	NC
AA4	NC
AA5	NC
AA6	IO135RSB2
AA7	IO133RSB2
AA8	NC
AA9	NC
AA10	NC
AA11	NC
AA12	NC
AA13	NC
AA14	NC
AA15	NC
AA16	IO101RSB2
AA17	NC
AA18	NC
AA19	NC
AA20	NC
AA21	VCCIB1
AA22	GND
AB1	GND
AB2	GND
AB3	VCCIB2
AB4	NC
AB5	NC
AB6	IO130RSB2

FG484	
Pin Number	A3P600 Function
AB7	IO128RSB2
AB8	IO122RSB2
AB9	IO116RSB2
AB10	NC
AB11	NC
AB12	IO113RSB2
AB13	IO112RSB2
AB14	NC
AB15	NC
AB16	IO100RSB2
AB17	IO95RSB2
AB18	NC
AB19	NC
AB20	VCCIB2
AB21	GND
AB22	GND

Revision	Changes	Page
Revision 5 (Aug 2008) DC and Switching Characteristics v1.3	T _J , Maximum Junction Temperature, was changed to 100° from 110° in the "Thermal Characteristics" section and EQ 1. The calculated result of Maximum Power Allowed has thus changed to 1.463 W from 1.951 W.	2-6
	Values for the A3P015 device were added to Table 2-7 • Quiescent Supply Current Characteristics.	2-7
	Values for the A3P015 device were added to Table 2-14 • Different Components Contributing to Dynamic Power Consumption in ProASIC3 Devices. P _{AC14} was removed. Table 2-15 • Different Components Contributing to the Static Power Consumption in ProASIC3 Devices is new.	2-11, 2-12
	The "PLL Contribution—P _{PLL} " section was updated to change the P _{PLL} formula from P _{AC13} + P _{AC14} * F _{CLKOUT} to P _{DC4} + P _{AC13} * F _{CLKOUT} .	2-14
	Both fall and rise values were included for t _{DDRISUD} and t _{DDRIHD} in Table 2-102 • Input DDR Propagation Delays.	2-78
	Table 2-107 • A3P015 Global Resource is new.	2-86
	The typical value for Delay Increments in Programmable Delay Blocks was changed from 160 to 200 in Table 2-115 • ProASIC3 CCC/PLL Specification.	2-90
Revision 4 (Jun 2008) DC and Switching Characteristics v1.2	Table note references were added to Table 2-2 • Recommended Operating Conditions 1, and the order of the table notes was changed.	2-2
	The title for Table 2-4 • Overshoot and Undershoot Limits 1 was modified to remove "as measured on quiet I/Os." Table note 1 was revised to remove "estimated SSO density over cycles." Table note 2 was revised to remove "refers only to overshoot/undershoot limits for simultaneous switching I/Os."	2-3
	The "Power per I/O Pin" section was updated to include 3 additional tables pertaining to input buffer power and output buffer power.	2-7
	Table 2-29 • I/O Output Buffer Maximum Resistances 1 was revised to include values for 3.3 V PCI/PCI-X.	2-27
	Table 2-90 • LVDS Minimum and Maximum DC Input and Output Levels was updated.	2-66
Revision 3 (Jun 2008) Packaging v1.3	Pin numbers were added to the "QN68 – Bottom View" package diagram. Note 2 was added below the diagram.	4-3
	The "QN132 – Bottom View" package diagram was updated to include D1 to D4. In addition, note 1 was changed from top view to bottom view, and note 2 is new.	4-6
Revision 2 (Feb 2008) Product Brief v1.0	This document was divided into two sections and given a version number, starting at v1.0. The first section of the document includes features, benefits, ordering information, and temperature and speed grade offerings. The second section is a device family overview.	N/A
	This document was updated to include A3P015 device information. QN68 is a new package that was added because it is offered in the A3P015. The following sections were updated: "Features and Benefits" "ProASIC3 Ordering Information" "Temperature Grade Offerings" "ProASIC3 Flash Family FPGAs" "A3P015 and A3P030" note Introduction and Overview (NA)	N/A