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### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	16 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/z8f011ahh020eg">https://www.e-xfl.com/product-detail/zilog/z8f011ahh020eg</a>

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- Up to 8 ports capable of direct LED drive with no current limit resistor required
- On-Chip Debugger (OCD)
- Voltage Brown-Out (VBO) protection
- Programmable low battery detection (LVD) (8-pin devices only)
- Bandgap generated precision voltage references available for the ADC, comparator, VBO and LVD
- Power-On Reset (POR)
- 2.7V to 3.6V operating voltage
- 8-, 20- and 28-pin packages
- 0°C to +70°C and –40°C to +105°C for operating temperature ranges

## Part Selection Guide

Table 1 identifies the basic features and package styles available for each device within the Z8 Encore! XP F082A Series product line.

**Table 1. Z8 Encore! XP F082A Series Family Part Selection Guide**

Part Number	Flash (KB)	RAM (B)	NVDS <sup>1</sup> (B)	I/O	Comparator	Advanced Analog <sup>2</sup>	ADC Inputs	Packages
Z8F082A	8	1024	0	6–23	Yes	Yes	4–8	8-, 20- and 28-pin
Z8F081A	8	1024	0	6–25	Yes	No	0	8-, 20- and 28-pin
Z8F042A	4	1024	128	6–23	Yes	Yes	4–8	8-, 20- and 28-pin
Z8F041A	4	1024	128	6–25	Yes	No	0	8-, 20- and 28-pin
Z8F022A	2	512	64	6–23	Yes	Yes	4–8	8-, 20- and 28-pin
Z8F021A	2	512	64	6–25	Yes	No	0	8-, 20- and 28-pin
Z8F012A	1	256	16	6–23	Yes	Yes	4–8	8-, 20- and 28-pin
Z8F011A	1	256	16	6–25	Yes	No	0	8-, 20- and 28-pin

Notes:

1. Non-volatile data storage.

2. Advanced Analog includes ADC, temperature sensor and low-power operational amplifier.

# Register Map

Table 7 provides the address map for the Register File of the Z8 Encore! XP F082A Series devices. Not all devices and package styles in the Z8 Encore! XP F082A Series support the ADC, or all of the GPIO Ports. Consider registers for unimplemented peripherals as Reserved.

**Table 7. Register File Address Map**

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page
<b>General-Purpose RAM</b>				
<b>Z8F082A/Z8F081A Devices</b>				
000–3FF	General-Purpose Register File RAM	—	XX	
400–EFF	Reserved	—	XX	
<b>Z8F042A/Z8F041A Devices</b>				
000–3FF	General-Purpose Register File RAM	—	XX	
400–EFF	Reserved	—	XX	
<b>Z8F022A/Z8F021A Devices</b>				
000–1FF	General-Purpose Register File RAM	—	XX	
200–EFF	Reserved	—	XX	
<b>Z8F012A/Z8F011A Devices</b>				
000–0FF	General-Purpose Register File RAM	—	XX	
100–EFF	Reserved	—	XX	
<b>Timer 0</b>				
F00	Timer 0 High Byte	T0H	00	<u>90</u>
F01	Timer 0 Low Byte	T0L	01	<u>90</u>
F02	Timer 0 Reload High Byte	T0RH	FF	<u>91</u>
F03	Timer 0 Reload Low Byte	T0RL	FF	<u>91</u>
F04	Timer 0 PWM High Byte	T0PWMH	00	<u>92</u>
F05	Timer 0 PWM Low Byte	T0PWML	00	<u>92</u>
F06	Timer 0 Control 0	T0CTL0	00	<u>85</u>
F07	Timer 0 Control 1	T0CTL1	00	<u>86</u>

Notes:

1. XX = Undefined.
2. Refer to the [eZ8 CPU Core User Manual \(UM0128\)](#).

## Shared Debug Pin

On the 8-pin version of this device only, the Debug pin shares function with the PA0 GPIO pin. This pin performs as a general purpose input pin on power-up, but the debug logic monitors this pin during the reset sequence to determine if the unlock sequence occurs. If the unlock sequence is present, the debug function is unlocked and the pin no longer functions as a GPIO pin. If it is not present, the debug feature is disabled until/unless another reset event occurs. For more details, see the [On-Chip Debugger](#) chapter on page 180.

## Crystal Oscillator Override

For systems using a crystal oscillator, PA0 and PA1 are used to connect the crystal. When the crystal oscillator is enabled, the GPIO settings are overridden and PA0 and PA1 are disabled. See the [Oscillator Control Register Definitions](#) section on page 196 for details.

## 5V Tolerance

All six I/O pins on the 8-pin devices are 5 V-tolerant, unless the programmable pull-ups are enabled. If the pull-ups are enabled and inputs higher than  $V_{DD}$  are applied to these parts, excessive current flows through those pull-up devices and can damage the chip.

---

► **Note:** In the 20- and 28-pin versions of this device, any pin which shares functionality with an ADC, crystal or comparator port is not 5 V-tolerant, including PA[1:0], PB[5:0] and PC[2:0]. All other signal pins are 5 V-tolerant and can safely handle inputs higher than  $V_{DD}$  except when the programmable pull-ups are enabled.

---

## External Clock Setup

For systems using an external TTL drive, PB3 is the clock source for 20- and 28-pin devices. In this case, configure PB3 for alternate function CLKIN. Write the Oscillator Control (OSCCTL) Register such that the external oscillator is selected as the system clock. See the [Oscillator Control Register Definitions](#) section on page 196 for details. For 8-pin devices, use PA1 instead of PB3.

Table 15. Port Alternate Function Mapping (Non 8-Pin Parts) (Continued)

Port	Pin	Mnemonic	Alternate Function Description	Alternate Function Set Register AFS1
Port C <sup>5</sup>	PC0	Reserved		AFS1[0]: 0
		ANA4/CINP	ADC or Comparator Input	AFS1[0]: 1
	PC1	Reserved		AFS1[1]: 0
		ANA5/CINN	ADC or Comparator Input	AFS1[1]: 1
	PC2	Reserved		AFS1[2]: 0
		ANA6/V <sub>REF</sub> <sup>4</sup>	ADC Analog Input or ADC Voltage Reference	AFS1[2]: 1
	PC3	COUT	Comparator Output	AFS1[3]: 0
		Reserved		AFS1[3]: 1
	PC4	Reserved		AFS1[4]: 0
				AFS1[4]: 1
	PC5	Reserved		AFS1[5]: 0
				AFS1[5]: 1
	PC6	Reserved		AFS1[6]: 0
				AFS1[6]: 1
	PC7	Reserved		AFS1[7]: 0
				AFS1[7]: 1
Port D <sup>6</sup>	PD0	RESET	External Reset	N/A

## Notes:

1. Because there is only a single alternate function for each Port A pin, the Alternate Function Set registers are not implemented for Port A. Enabling alternate function selections automatically enables the associated alternate function. See the [Port A–D Alternate Function Subregisters \(PxAF\)](#) section on page 47 for details.
2. Whether PA0/PA6 takes on the timer input or timer output complement function depends on the timer configuration. See the [Timer Pin Signal Operation](#) section on page 84 for details.
3. Because there are at most two choices of alternate function for any pin of Port B, the Alternate Function Set Register AFS2 is not used to select the function. Alternate function selection must also be enabled. See the [Port A–D Alternate Function Subregisters \(PxAF\)](#) section on page 47 for details.
4. V<sub>REF</sub> is available on PB5 in 28-pin products and on PC2 in 20-pin parts.
5. Because there are at most two choices of alternate function for any pin of Port C, the Alternate Function Set Register AFS2 is not used to select the function. Alternate function selection must also be enabled. See the [Port A–D Alternate Function Subregisters \(PxAF\)](#) section on page 47 for details.
6. Because there is only a single alternate function for the Port PD0 pin, the Alternate Function Set registers are not implemented for Port D. Enabling alternate function selections automatically enables the associated alternate function. See the [Port A–D Alternate Function Subregisters \(PxAF\)](#) section on page 47 for details.



**Table 23. Port A–D Output Control Subregisters (PxOC)**

Bit	7	6	5	4	3	2	1	0
Field	POC7	POC6	POC5	POC4	POC3	POC2	POC1	POC0
RESET	00H (Ports A-C); 01H (Port D)							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	If 03H in Port A–D Address Register, accessible through the Port A–D Control Register							

Bit	Description
[7:0] POCx	<b>Port Output Control</b> These bits function independently of the alternate function bit and always disable the drains if set to 1. 0 = The source current is enabled for any output mode unless overridden by the alternate function (push-pull output). 1 = The source current for the associated pin is disabled (open-drain mode).

Note: x indicates the specific GPIO port pin number (7–0).

### Port A–D High Drive Enable Subregisters

The Port A–D High Drive Enable Subregister, shown in Table 24, is accessed through the port A–D Control Register by writing 04H to the Port A–D Address Register. Setting the bits in the Port A–D High Drive Enable subregisters to 1 configures the specified port pins for high current output drive operation. The Port A–D High Drive Enable subregister affects the pins directly and, as a result, alternate functions are also affected.

**Table 24. Port A–D High Drive Enable Subregisters (PxHDE)**

Bit	7	6	5	4	3	2	1	0
Field	PHDE7	PHDE6	PHDE5	PHDE4	PHDE3	PHDE2	PHDE1	PHDE0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	If 04H in Port A–D Address Register, accessible through the Port A–D Control Register							

Bit	Description
[7:0] PHDEx	<b>Port High Drive Enabled</b> 0 = The port pin is configured for standard output current drive. 1 = The port pin is configured for high output current drive.

Note: x indicates the specific GPIO port pin number (7–0).

## GPIO Mode Interrupt Controller

The interrupt controller on the Z8 Encore! XP F082A Series products prioritizes the interrupt requests from the on-chip peripherals and the GPIO port pins. The features of interrupt controller include:

- 20 possible interrupt sources with 18 unique interrupt vectors:
  - Twelve GPIO port pin interrupt sources (two interrupt vectors are shared)
  - Eight on-chip peripheral interrupt sources (two interrupt vectors are shared)
- Flexible GPIO interrupts:
  - Eight selectable rising and falling edge GPIO interrupts
  - Four dual-edge interrupts
- Three levels of individually programmable interrupt priority
- Watchdog Timer and LVD can be configured to generate an interrupt
- Supports vectored and polled interrupts

Interrupt requests (IRQs) allow peripheral devices to suspend CPU operation in an orderly manner and force the CPU to start an interrupt service routine (ISR). Usually this interrupt service routine is involved with the exchange of data, status information, or control information between the CPU and the interrupting peripheral. When the service routine is completed, the CPU returns to the operation from which it was interrupted.

The eZ8 CPU supports both vectored and polled interrupt handling. For polled interrupts, the interrupt controller has no effect on operation. For more information about interrupt servicing by the eZ8 CPU, refer to the [eZ8 CPU Core User Manual \(UM0128\)](#), which is available for download on [www.zilog.com](http://www.zilog.com).

### Interrupt Vector Listing

Table 34 lists all of the interrupts available in order of priority. The interrupt vector is stored with the most-significant byte (MSB) at the even Program Memory address and the least-significant byte (LSB) at the following odd Program Memory address.

---

► **Note:** Some port interrupts are not available on the 8- and 20-pin packages. The ADC interrupt is unavailable on devices not containing an ADC.

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**Table 34. Trap and Interrupt Vectors in Order of Priority**

<b>Priority</b>	<b>Program Memory Vector Address</b>	<b>Interrupt or Trap Source</b>
Highest	0002H	Reset (not an interrupt)
	0004H	Watchdog Timer (see Watchdog Timer)
	003AH	Primary Oscillator Fail Trap (not an interrupt)
	003CH	Watchdog Oscillator Fail Trap (not an interrupt)
	0006H	Illegal Instruction Trap (not an interrupt)
	0008H	Reserved
	000AH	Timer 1
	000CH	Timer 0
	000EH	UART 0 receiver
	0010H	UART 0 transmitter
	0012H	Reserved
	0014H	Reserved
	0016H	ADC
	0018H	Port A Pin 7, selectable rising or falling input edge or LVD (see Reset, Stop Mode Recovery and Low Voltage Detection)
	001AH	Port A Pin 6, selectable rising or falling input edge or Comparator Output
	001CH	Port A Pin 5, selectable rising or falling input edge
	001EH	Port A Pin 4, selectable rising or falling input edge
	0020H	Port A Pin 3, selectable rising or falling input edge
	0022H	Port A Pin 2, selectable rising or falling input edge
	0024H	Port A Pin 1, selectable rising or falling input edge
	0026H	Port A Pin 0, selectable rising or falling input edge
	0028H	Reserved
	002AH	Reserved
	002CH	Reserved
	002EH	Reserved
	0030H	Port C Pin 3, both input edges
	0032H	Port C Pin 2, both input edges
	0034H	Port C Pin 1, both input edges
Lowest	0036H	Port C Pin 0, both input edges
	0038H	Reserved

## PWM SINGLE OUTPUT Mode

In PWM SINGLE OUTPUT Mode, the timer outputs a Pulse-Width Modulator (PWM) output signal through a GPIO port pin. The timer input is the system clock. The timer first counts up to the 16-bit PWM match value stored in the Timer PWM High and Low Byte registers. When the timer count value matches the PWM value, the Timer Output toggles. The timer continues counting until it reaches the reload value stored in the Timer Reload High and Low Byte registers. Upon reaching the reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes.

If the TPOL bit in the Timer Control Register is set to 1, the Timer Output signal begins as a High (1) and transitions to a Low (0) when the timer value matches the PWM value. The Timer Output signal returns to a High (1) after the timer reaches the reload value and is reset to 0001H.

If the TPOL bit in the Timer Control Register is set to 0, the Timer Output signal begins as a Low (0) and transitions to a High (1) when the timer value matches the PWM value. The Timer Output signal returns to a Low (0) after the timer reaches the reload value and is reset to 0001H.

Observe the following steps for configuring a timer for PWM SINGLE OUTPUT Mode and initiating the PWM operation:

1. Write to the Timer Control Register to:
  - Disable the timer
  - Configure the timer for PWM SINGLE OUTPUT Mode
  - Set the prescale value
  - Set the initial logic level (High or Low) and PWM High/Low transition for the Timer Output alternate function
2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H). This only affects the first pass in PWM mode. After the first timer reset in PWM mode, counting always begins at the reset value of 0001H.
3. Write to the PWM High and Low Byte registers to set the PWM value.
4. Write to the Timer Reload High and Low Byte registers to set the reload value (PWM period). The reload value must be greater than the PWM value.
5. If appropriate, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
6. Configure the associated GPIO port pin for the Timer Output alternate function.
7. Write to the Timer Control Register to enable the timer and initiate counting.

- Set or clear the CTSE bit to enable or disable control from the remote receiver using the  $\overline{\text{CTS}}$  pin
6. Check the TDRE bit in the UART Status 0 Register to determine if the Transmit Data Register is empty (indicated by a 1). If empty, continue to [Step 7](#). If the Transmit Data Register is full (indicated by a 0), continue to monitor the TDRE bit until the Transmit Data Register becomes available to receive new data.
  7. Write the UART Control 1 Register to select the outgoing address bit.
  8. Set the Multiprocessor Bit Transmitter (MPBT) if sending an address byte, clear it if sending a data byte.
  9. Write the data byte to the UART Transmit Data Register. The transmitter automatically transfers the data to the Transmit Shift Register and transmits the data.
  10. Make any changes to the Multiprocessor Bit Transmitter (MPBT) value, if appropriate and MULTIPROCESSOR Mode is enabled.
  11. To transmit additional bytes, return to [Step 5](#).

## Transmitting Data using the Interrupt-Driven Method

The UART Transmitter interrupt indicates the availability of the Transmit Data Register to accept new data for transmission. Observe the following steps to configure the UART for interrupt-driven data transmission:

1. Write to the UART Baud Rate High and Low Byte registers to set the appropriate baud rate.
2. Enable the UART pin functions by configuring the associated GPIO port pins for alternate function operation.
3. Execute a DI instruction to disable interrupts.
4. Write to the Interrupt control registers to enable the UART Transmitter interrupt and set the acceptable priority.
5. Write to the UART Control 1 Register to enable MULTIPROCESSOR (9-bit) Mode functions, if MULTIPROCESSOR Mode is appropriate.
6. Set the MULTIPROCESSOR Mode Select (MPEN) to Enable MULTIPROCESSOR Mode.
7. Write to the UART Control 0 Register to:
  - Set the transmit enable bit (TEN) to enable the UART for data transmission
  - Enable parity, if appropriate and if MULTIPROCESSOR Mode is not enabled and select either even or odd parity

Bit	Description (Continued)
[2] TDRE	<b>TDRE—Transmitter Data Register Empty</b> This bit indicates that the UART Transmit Data Register is empty and ready for additional data. Writing to the UART Transmit Data Register resets this bit. 0 = Do not write to the UART Transmit Data Register. 1 = The UART Transmit Data Register is ready to receive an additional byte to be transmitted.
[1] TXE	<b>Transmitter Empty</b> This bit indicates that the Transmit Shift Register is empty and character transmission is finished. 0 = Data is currently transmitting. 1 = Transmission is complete.
[0] CTS	<b>CTS Signal</b> When this bit is read it returns the level of the $\overline{\text{CTS}}$ signal. This signal is active Low.

## UART Status 1 Register

This register contains multiprocessor control and status bits.

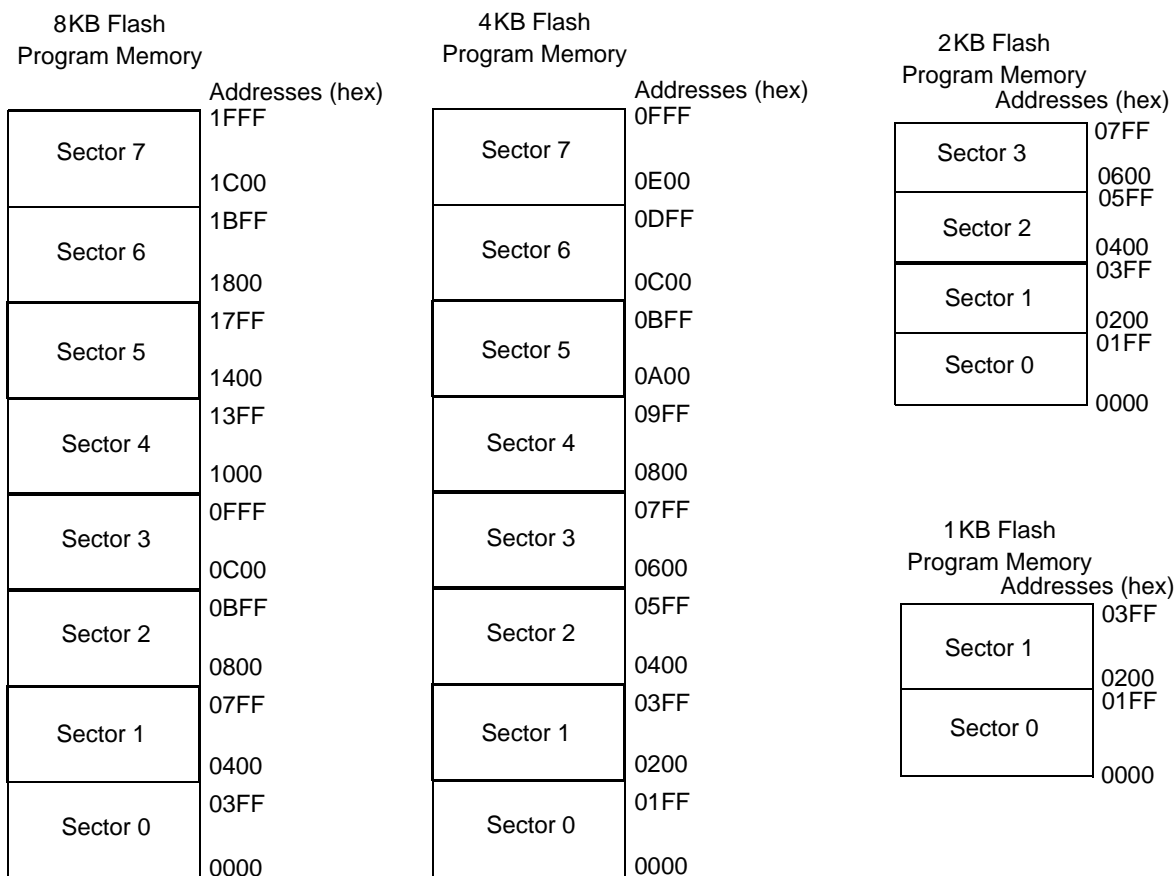
**Table 66. UART Status 1 Register (U0STAT1)**

Bit	7	6	5	4	3	2	1	0
Field	Reserved						NEWFRM	MPRX
RESET	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R/W	R/W	R	R
Address	F44H							

Bit	Description
[7:2]	<b>Reserved</b> These bits are reserved and must be programmed to 000000.
[1] NEWFRM	<b>New Frame</b> A status bit denoting the start of a new frame. Reading the UART Receive Data Register resets this bit to 0. 0 = The current byte is not the first data byte of a new frame. 1 = The current byte is the first data byte of a new frame.
[0] MPRX	<b>Multiprocessor Receive</b> Returns the value of the most recent multiprocessor bit received. Reading from the UART Receive Data Register resets this bit to 0.

## UART Transmit Data Register

Data bytes written to the UART Transmit Data (UxTXD) Register, shown in Table 67, are shifted out on the TXDx pin. The Write-only UART Transmit Data Register shares a Register File address with the read-only UART Receive Data Register.



**Figure 21. Flash Memory Arrangement**

## Flash Information Area

The Flash information area is separate from Program Memory and is mapped to the address range FE00H to FFFFH. This area is readable but cannot be erased or overwritten. Factory trim values for the analog peripherals are stored here. Factory calibration data for the ADC is also stored here.

## Operation

The Flash Controller programs and erases Flash memory. The Flash Controller provides the proper Flash controls and timing for Byte Programming, Page Erase and Mass Erase of Flash memory.

The Flash Controller contains several protection mechanisms to prevent accidental programming or erasure. These mechanism operate on the page, sector and full-memory levels.

## Trim Bit Address 0002H

Table 92. Trim Option Bits at 0002H (TIPO)

Bit	7	6	5	4	3	2	1	0
Field	IPO_TRIM							
RESET	U							
R/W	R/W							
Address	Information Page Memory 0022H							
Note: U = Unchanged by Reset. R/W = Read/Write.								

Bit	Description
[7:0]	<b>Internal Precision Oscillator Trim Byte</b>
IPO_TRIM	Contains trimming bits for the Internal Precision Oscillator.

## Trim Bit Address 0003H

► **Note:** The LVD is available on 8-pin devices only.

Table 93. Trim Option Bits at Address 0003H (TLVD)

Bit	7	6	5	4	3	2	1	0
Field	Reserved			LVD_TRIM				
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Information Page Memory 0023H							
Note: U = Unchanged by Reset. R/W = Read/Write.								

Bit	Description
[7:5]	<b>Reserved</b> These bits are reserved and must be programmed to 111.
[4:0]	<b>Low Voltage Detect Trimm</b>
LVD_TRIM	This trimming affects the low voltage detection threshold. Each LSB represents a 50mV change in the threshold level. Alternatively, the low voltage threshold may be computed from the options bit value by the following equation:  $\text{LVD\_LVL} = 3.6 \text{ V} - \text{LVD\_TRIM} \times 0.05 \text{ V}$ <p>These values are tabulated in Table 94.</p>



Table 107. NVDS Read Time

Operation	Minimum Latency	Maximum Latency
Read (16 byte array)	875	9961
Read (64 byte array)	876	8952
Read (128 byte array)	883	7609
Write (16 byte array)	4973	5009
Write (64 byte array)	4971	5013
Write (128 byte array)	4984	5023
Illegal Read	43	43
Illegal Write	31	31

If NVDS read performance is critical to your software architecture, you can optimize your code for speed. Try the first suggestion below before attempting the second.

1. Periodically refresh all addresses that are used. The optimal use of NVDS in terms of speed is to rotate the writes evenly among all addresses planned to use, bringing all reads closer to the minimum read time. Because the minimum read time is much less than the write time, however, actual speed benefits are not always realized.
2. Use as few unique addresses as possible to optimize the impact of refreshing, plus minimize the requirement for it.

Serial Break leaves the device in DEBUG Mode if that is the current mode. The OCD is held in Reset until the end of the Serial Break when the DBG pin returns High. Because of the open-drain nature of the DBG pin, the host can send a Serial Break to the OCD even if the OCD is transmitting a character.

## OCD Unlock Sequence (8-Pin Devices Only)

Because of pin-sharing on the 8-pin device, an unlock sequence must be performed to access the DBG pin. If this sequence is not completed during a system reset, then the PA0/DBG pin functions only as a GPIO pin.

The following sequence unlocks the DBG pin:

1. Hold PA2/RESET Low.
2. Wait 5ms for the internal reset sequence to complete.
3. Send the following bytes serially to the debug pin:  
DBG ← 80H (autobaud)  
DBG ← EBH  
DBG ← 5AH  
DBG ← 70H  
DBG ← CDH (32-bit unlock key)
4. Release PA2/RESET. The PA0/DBG pin is now identical in function to that of the DBG pin on the 20-/28-pin device. To enter DEBUG Mode, reautobaud and write 80H to the OCD Control Register (see the On-Chip Debugger Commands section on page 186).

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**! Caution:** Between Steps 3 and 4, there is an interval during which the 8-pin device is neither in RESET nor DEBUG Mode. If a device has been erased or has not yet been programmed, all program memory bytes contain FFH. The CPU interprets this value as an illegal instruction; therefore some irregular behavior can occur before entering DEBUG Mode, and the register values after entering DEBUG Mode will differ from their specified reset values. However, none of these irregularities prevent the programming of Flash memory. Before beginning system debug, Zilog recommends that some legal code be programmed into the 8-pin device and that a RESET occurs.

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## Breakpoints

Execution Breakpoints are generated using the BRK instruction (opcode 00H). When the eZ8 CPU decodes a BRK instruction, it signals the On-Chip Debugger. If Breakpoints are enabled, the OCD enters DEBUG Mode and idles the eZ8 CPU. If Breakpoints are not

## Ordering Information

Order your F082A Series products from Zilog using the part numbers shown in Table 148. For more information about ordering, please consult your local Zilog sales office. The [Sales Location](#) page on the Zilog website lists all regional offices.

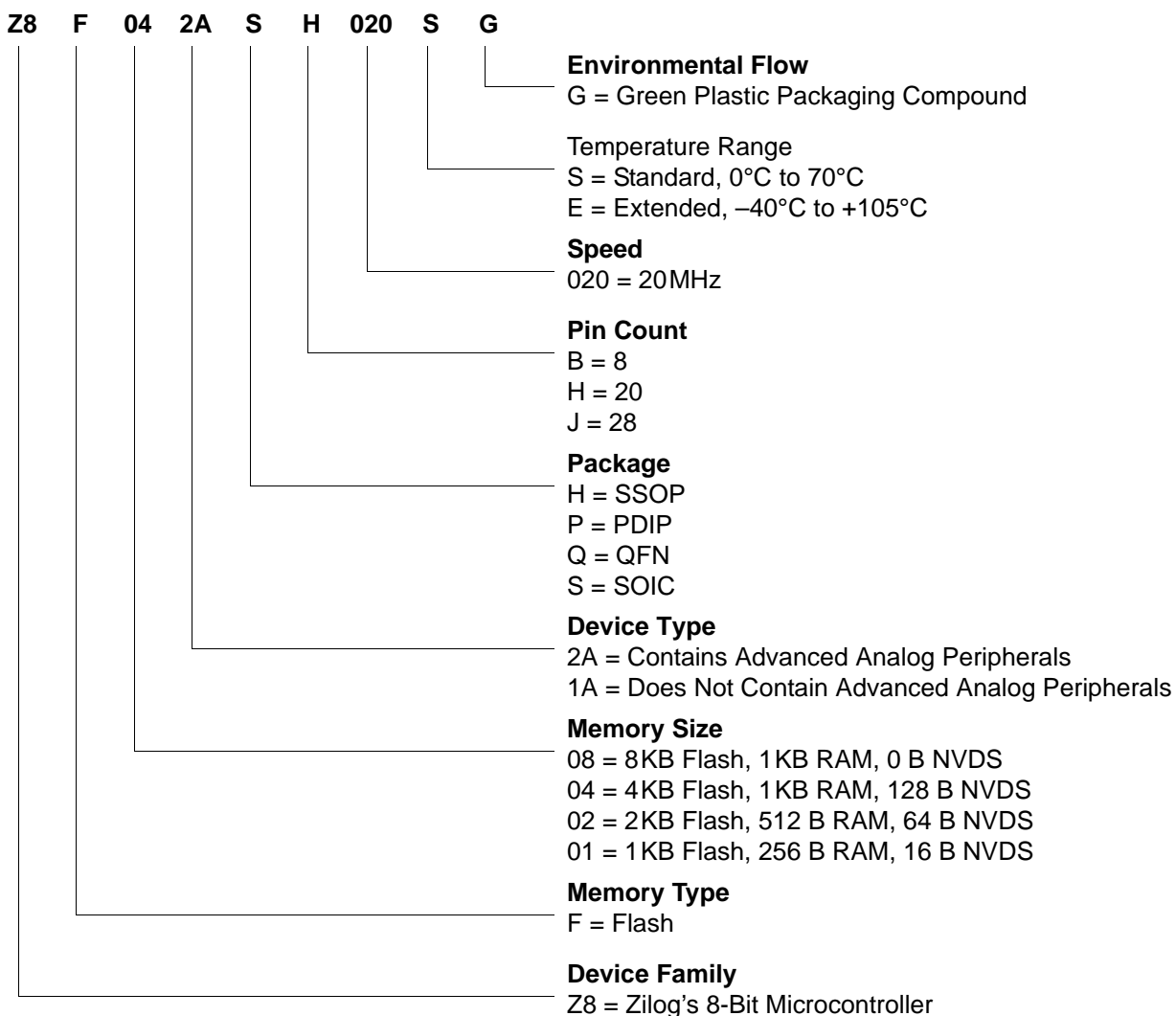
**Table 148. Z8 Encore! XP F082A Series Ordering Matrix**

Part Number	Flash	RAM	NVDS	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description
<b>Z8 Encore! XP F082A Series with 8KB Flash, 10-Bit Analog-to-Digital Converter</b>											
<b>Standard Temperature: 0°C to 70°C</b>											
Z8F082APB020SG	8KB	1KB	0	6	14	2	4	1	1	1	PDIP 8-pin package
Z8F082AQB020SG	8KB	1KB	0	6	14	2	4	1	1	1	QFN 8-pin package
Z8F082ASB020SG	8KB	1KB	0	6	14	2	4	1	1	1	SOIC 8-pin package
Z8F082ASH020SG	8KB	1KB	0	17	20	2	7	1	1	1	SOIC 20-pin package
Z8F082AHH020SG	8KB	1KB	0	17	20	2	7	1	1	1	SSOP 20-pin package
Z8F082APH020SG	8KB	1KB	0	17	20	2	7	1	1	1	PDIP 20-pin package
Z8F082ASJ020SG	8KB	1KB	0	23	20	2	8	1	1	1	SOIC 28-pin package
Z8F082AHJ020SG	8KB	1KB	0	23	20	2	8	1	1	1	SSOP 28-pin package
Z8F082APJ020SG	8KB	1KB	0	23	20	2	8	1	1	1	PDIP 28-pin package
<b>Extended Temperature: -40°C to 105°C</b>											
Z8F082APB020EG	8KB	1KB	0	6	14	2	4	1	1	1	PDIP 8-pin package
Z8F082AQB020EG	8KB	1KB	0	6	14	2	4	1	1	1	QFN 8-pin package
Z8F082ASB020EG	8KB	1KB	0	6	14	2	4	1	1	1	SOIC 8-pin package
Z8F082ASH020EG	8KB	1KB	0	17	20	2	7	1	1	1	SOIC 20-pin package
Z8F082AHH020EG	8KB	1KB	0	17	20	2	7	1	1	1	SSOP 20-pin package
Z8F082APH020EG	8KB	1KB	0	17	20	2	7	1	1	1	PDIP 20-pin package
Z8F082ASJ020EG	8KB	1KB	0	23	20	2	8	1	1	1	SOIC 28-pin package
Z8F082AHJ020EG	8KB	1KB	0	23	20	2	8	1	1	1	SSOP 28-pin package
Z8F082APJ020EG	8KB	1KB	0	23	20	2	8	1	1	1	PDIP 28-pin package

## Part Number Suffix Designations

Zilog part numbers consist of a number of components, as indicated in the following example.

**Example.** Part number Z8F042ASH020SG is an 8-bit Flash MCU with 4KB of Program Memory, equipped with advanced analog peripherals in a 20-pin SOIC package, operating within a 0°C to +70°C temperature range and built using lead-free solder.



LD 210  
 LDC 210  
 LDCI 209, 210  
 LDE 210  
 LDEI 209  
 LDX 210  
 LEA 210  
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 MULT 208  
 NOP 209  
 OR 210  
 ORX 210  
 POP 210  
 POPX 210  
 program control 211  
 PUSH 210  
 PUSHX 210  
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 RET 211  
 RL 211  
 RLC 211  
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 RR 211  
 RRC 211  
 SBC 208  
 SCF 209, 210  
 SRA 211  
 SRL 211  
 SRP 210  
 STOP 210  
 SUB 208  
 SUBX 208  
 SWAP 211  
 TCM 209  
 TCMX 209  
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 TRAP 211  
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 XOR 210  
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 IR 206  
 Ir 206  
 IrDA  
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   block diagram 120  
   control register definitions 123  
   operation 120  
   receiving data 122  
   transmitting data 121  
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 IRQ1 enable high and low bit registers 64  
 IRQ2 enable high and low bit registers 65  
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 Irr 206

## **J**

JP 211  
 jump, conditional, relative, and relative conditional  
 211

## **L**

LD 210  
 LDC 210  
 LDCI 209, 210  
 LDE 210  
 LDEI 209, 210  
 LDX 210