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Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	16 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.173", 4.40mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f011ahj020sg

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Z8 Encore! XP[®] F082A Series Product Specification

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Signal Descriptions

Table 2 describes the Z8 Encore! XP F082A Series signals. See the <u>Pin Configurations</u> section on page 8 to determine the signals available for the specific package styles.

Signal Mnemonic	I/O	Description
General-Purpose I/C) Ports	A–D
PA[7:0]	I/O	Port A. These pins are used for general-purpose I/O.
PB[7:0]	I/O	Port B. These pins are used for general-purpose I/O. PB6 and PB7 are available only in those devices without an ADC.
PC[7:0]	I/O	Port C. These pins are used for general-purpose I/O.
PD[0]	I/O	Port D. This pin is used for general-purpose output only.
UART Controllers		
TXD0	0	Transmit Data. This signal is the transmit output from the UART and IrDA.
RXD0	I	Receive Data. This signal is the receive input for the UART and IrDA.
CTS0	Ι	Clear To Send. This signal is the flow control input for the UART.
DE	0	Driver Enable. This signal allows automatic control of external RS-485 drivers. This signal is approximately the inverse of the TXE (Transmit Empty) bit in the UART Status 0 Register. The DE signal may be used to ensure the external RS-485 driver is enabled when data is transmitted by the UART.
Timers		
T0OUT/T1OUT	0	Timer Output 0–1. These signals are outputs from the timers.
T0OUT/T1OUT	0	Timer Complement Output 0–1. These signals are output from the timers in PWM Dual Output mode.
T0IN/T1IN	I	Timer Input 0–1. These signals are used as the capture, gating and counter inputs.
Comparator		
CINP/CINN	Ι	Comparator Inputs. These signals are the positive and negative inputs to the comparator.
COUT	0	Comparator Output.
Notes:		

Table 2. Signal Descriptions

1. PB6 and PB7 are only available in 28-pin packages without ADC. In 28-pin packages with ADC, they are replaced by AV_{DD} and AV_{SS} .

2. The AV_{DD} and AV_{SS} signals are available only in 28-pin packages with ADC. They are replaced by PB6 and PB7 on 28-pin packages without ADC.

Signal Mnemonic	I/O	Description
Analog		
ANA[7:0]	Ι	Analog Port. These signals are used as inputs to the analog-to-digital converter (ADC).
VREF	I/O	Analog-to-digital converter reference voltage input, or buffered output for internal reference.
Low-Power Operati	ional Ar	nplifier (LPO)
AMPINP/AMPINN	Ι	LPO inputs. If enabled, these pins drive the positive and negative amplifier inputs respectively.
AMPOUT	0	LPO output. If enabled, this pin is driven by the on-chip LPO.
Oscillators		
XIN	I	External Crystal Input. This is the input pin to the crystal oscillator. A crystal can be connected between it and the X_{OUT} pin to form the oscillator. In addition, this pin is used with external RC networks or external clock drivers to provide the system clock.
X _{OUT}	0	External Crystal Output. This pin is the output of the crystal oscillator. A crystal can be connected between it and the XIN pin to form the oscillator.
Clock Input		
CLKIN	Ι	Clock Input Signal. This pin may be used to input a TTL-level signal to be used as the system clock.
LED Drivers		
LED	0	Direct LED drive capability. All port C pins have the capability to drive an LED without any other external components. These pins have programmable drive strengths set by the GPIO block.
On-Chip Debugger		
DBG	I/O	Debug. This signal is the control and data input and output to and from the On-Chip Debugger.
		Caution: The DBG pin is open-drain and requires a pull-up resistor to ensure proper operation.
Notes: 1. PB6 and PB7 are	only ava	ensure proper operation.

Table 2. Signal Descriptions (Continued)

replaced by AV_{DD} and AV_{SS} . 2. The AV_{DD} and AV_{SS} signals are available only in 28-pin packages with ADC. They are replaced by PB6 and PB7 on 28-pin packages without ADC.

Architecture

Figure 7 displays a simplified block diagram of a GPIO port pin. In this figure, the ability to accommodate alternate functions and variable port current drive strength is not displayed.



Figure 7. GPIO Port Pin Block Diagram

GPIO Alternate Functions

Many of the GPIO port pins can be used for general-purpose I/O and access to on-chip peripheral functions such as the timers and serial communication devices. The Port A–D Alternate Function subregisters configure these pins for either General-Purpose I/O or alternate function operation. When a pin is configured for alternate function, control of the port pin direction (input/output) is passed from the Port A–D Data Direction registers to the alternate function assigned to this pin. <u>Table 15</u> on page 40 lists the alternate functions possible with each port pin. For those pins with more one alternate function, the alternate function is defined through Alternate Function Sets subregisters AFS1 and AFS2.

The crystal oscillator functionality is not controlled by the GPIO block. When the crystal oscillator is enabled in the oscillator control block, the GPIO functionality of PA0 and PA1 is overridden. In that case, those pins function as input and output for the crystal oscillator.

Port A–D Pull-up Enable Subregisters

The Port A–D Pull-up Enable Subregister, shown in Table 26, is accessed through the Port A–D Control Register by writing 06H to the Port A–D Address Register. Setting the bits in the Port A–D Pull-up Enable subregisters enables a weak internal resistive pull-up on the specified port pins.

Bit	7	6	5	4	3	2	1	0
Field	PPUE7	PPUE6	PPUE5	PPUE4	PPUE3	PPUE2	PPUE1	PPUE0
RESET		00H (Ports A-C); 01H (Port D); 04H (Port A of 8-pin device)						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	If 06H in Port A–D Address Register, accessible through the Port A–D Control Register							
Bit	Descriptio	n						

Table	20			D	Frable	Culture al			ì
lable A	26.	Port	A-D	Pull-Up	Enable	Subregi	sters (PXPUE	.)

Bit	Description
[7:0]	Port Pull-up Enabled
PPUEx	0 = The weak pull-up on the port pin is disabled.
	1 = The weak pull-up on the port pin is enabled.
Note: x ii	ndicates the specific GPIO port pin number (7–0).

Port A–D Alternate Function Set 1 Subregisters

The Port A–D Alternate Function Set1 Subregister, shown in Table 27, is accessed through the Port A–D Control Register by writing 07H to the Port A–D Address Register. The Alternate Function Set 1 subregisters selects the alternate function available at a port pin. Alternate Functions selected by setting or clearing bits of this register are defined in the <u>GPIO Alternate Functions</u> section on page 37.

Note: Alternate function selection on port pins must also be enabled as described in the <u>Port A</u>– <u>D Alternate Function Subregisters</u> section on page 47.

Bit Description (Continued)

[6] Timer Input/Output Polarity

TPOL Operation of this bit is a function of the current operating mode of the timer.

ONE-SHOT Mode

When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer Reload.

CONTINUOUS Mode

When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer Reload.

COUNTER Mode

If the timer is enabled the Timer Output signal is complemented after timer reload.

- 0 = Count occurs on the rising edge of the Timer Input signal.
- 1 = Count occurs on the falling edge of the Timer Input signal.

PWM SINGLE OUTPUT Mode

- 0 = Timer Output is forced Low (0) when the timer is disabled. When enabled, the Timer Output is forced High (1) upon PWM count match and forced Low (0) upon reload.
- 1 = Timer Output is forced High (1) when the timer is disabled. When enabled, the Timer Output is forced Low (0) upon PWM count match and forced High (1) upon reload.

CAPTURE Mode

0 = Count is captured on the rising edge of the Timer Input signal.

1 = Count is captured on the falling edge of the Timer Input signal.

COMPARE Mode

When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer Reload.

Timer Reload High and Low Byte Registers

The Timer 0–1 Reload High and Low Byte (TxRH and TxRL) registers, shown in Tables 54 and 55, store a 16-bit reload value, {TRH[7:0], TRL[7:0]}. Values written to the Timer Reload High Byte Register are stored in a temporary holding register. When a write to the Timer Reload Low Byte Register occurs, the temporary holding register value is written to the Timer High Byte Register. This operation allows simultaneous updates of the 16-bit Timer reload value.

In COMPARE Mode, the Timer Reload High and Low Byte registers store the 16-bit Compare value.

Bit	7	6	5	4	3	2	1	0	
Field	TRH								
RESET	1	1	1	1	1	1	1	1	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address		F02H, F0AH							

Table 54. Timer 0–1 Reload High Byte Register (TxRH)

Bit	7	6	5	4	3	2	1	0	
Field	TRL								
RESET	1	1	1	1	1	1	1	1	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address				F03H,	F0BH				

Bit	Description
[7:0]	Timer Reload Register High and Low
TRH, TRL	These two bytes form the 16-bit reload value, {TRH[7:0], TRL[7:0]}. This value sets the max- imum count value which initiates a timer reload to 0001H. In COMPARE Mode, these two bytes form the 16-bit Compare value.

Timer 0–1 PWM High and Low Byte Registers

The Timer 0–1 PWM High and Low Byte (TxPWMH and TxPWML) registers, shown in Tables 56 and 57, control Pulse-Width Modulator (PWM) operations. These registers also store the Capture values for the CAPTURE and CAPTURE/COMPARE modes.

Bit	7	6	5	4	3	2	1	0
Field	PWMH							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F04H, F0CH							

Table 56. Timer 0–1 PWM High Byte Register (TxPWMH)

Table 57. Timer 0–1 PWM Low Byte Register (TxPWML)

Bit	7	6	5	4	3	2	1	0	
Field		PWML							
RESET	0	0	0	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address				F05H,	F0DH				

Bit Description

[7:0]	Pulse-Width Modulator High and Low Bytes
PWMH,	These two bytes, {PWMH[7:0], PWML[7:0]}, form a 16-bit value that is compared to the current
PWML	16-bit timer count. When a match occurs, the PWM output changes state. The PWM output
	value is set by the TPOL bit in the Timer Control Register (TxCTL1) Register.

The TxPWMH and TxPWML registers also store the 16-bit captured timer value when operating in CAPTURE or CAPTURE/COMPARE modes.

Watchdog Timer Reload Upper, High and Low Byte Registers

The Watchdog Timer Reload Upper, High and Low Byte (WDTU, WDTH, WDTL) registers, shown in Tables 60 through 62, form the 24-bit reload value that is loaded into the Watchdog Timer when a WDT instruction executes. The 24-bit reload value ranges across bits [23:0] to encompass the three bytes {WDTU[7:0], WDTH[7:0], WDTL[7:0]}. Writing to these registers sets the appropriate reload value. Reading from these registers returns the current Watchdog Timer count value.

Caution: The 24-bit WDT reload value must not be set to a value less than 000004H.

Bit	7	6	5	4	3	2	1	0		
Field		WDTU								
RESET				00)H					
R/W				R/	W*					
Address		FF1H								
Note: A re	Note: A read returns the current WDT count value; a write sets the appropriate reload value.									

Table 60. Watchdog Timer Reload Upper Byte Register (WDTU)

Bit	Description
[7:0]	WDT Reload Upper Byte
WDTU	Most-significant byte (MSB): bits[23:16] of the 24-bit WDT reload value.

Table 61. Watchdog Timer Reload High Byte Register (WDTH)

Bit	7	6	5	4	3	2	1	0	
Field	WDTH								
RESET				04	ιH				
R/W				R/	W*				
Address	FF2H								
Note: A re	ad returns th	e current WD	T count value	e; a write sets	the appropria	ate reload val	ue.		

Bit	Description
[7:0]	WDT Reload High Byte
WDTH	Middle byte; bits[15:8] of the 24-bit WDT reload value.



Figure 11. UART Asynchronous Data Format without Parity



Figure 12. UART Asynchronous Data Format with Parity

Transmitting Data using the Polled Method

Observe the following steps to transmit data using the polled method of operation:

- 1. Write to the UART Baud Rate High and Low Byte registers to set the required baud rate.
- 2. Enable the UART pin functions by configuring the associated GPIO port pins for alternate function operation.
- 3. Write to the UART Control 1 Register, if MULTIPROCESSOR Mode is appropriate, to enable MULTIPROCESSOR (9-bit) Mode functions.
- 4. Set the Multiprocessor Mode Select (MPEN) bit to enable MULTIPROCESSOR Mode.
- 5. Write to the UART Control 0 Register to:
 - Set the transmit enable bit (TEN) to enable the UART for data transmission
 - Set the parity enable bit (PEN), if parity is appropriate and MULTIPROCESSOR Mode is not enabled and select either even or odd parity (PSEL)

byte indicating an overrun error, the Receive Data Register must be read again to clear the error bits is the UART Status 0 Register. Updates to the Receive Data Register occur only when the next data word is received.

UART Data and Error Handling Procedure

Figure 15 displays the recommended procedure for use in UART receiver interrupt service routines.



Figure 15. UART Receiver Interrupt Service Routine Flow

Baud Rate Generator Interrupts

If the baud rate generator (BRG) interrupt enable is set, the UART Receiver interrupt asserts when the UART Baud Rate Generator reloads. This condition allows the Baud

The window remains open until the count again reaches 8 (that is, 24 baud clock periods since the previous pulse was detected), giving the Endec a sampling window of minus four baud rate clocks to plus eight baud rate clocks around the expected time of an incoming pulse. If an incoming pulse is detected inside this window this process is repeated. If the incoming data is a logical 1 (no pulse), the Endec returns to the initial state and waits for the next falling edge. As each falling edge is detected, the Endec clock counter is reset, resynchronizing the Endec to the incoming signal, allowing the Endec to tolerate jitter and baud rate errors in the incoming datastream. Resynchronizing the Endec does not alter the operation of the UART, which ultimately receives the data. The UART is only synchronized to the incoming data stream when a Start bit is received.

Infrared Encoder/Decoder Control Register Definitions

All infrared endec configuration and status information is set by the UART Control registers as defined in the <u>Universal Asynchronous Receiver/Transmitter</u> section on page 99.

Caution: To prevent spurious signals during IrDA data transmission, set the IREN bit in the UART Control 1 Register to 1 to enable the Infrared Encoder/Decoder before enabling the GPIO Port alternate function for the corresponding pin.

Comparator

The Z8 Encore! XP F082A Series devices feature a general purpose comparator that compares two analog input signals. These analog signals may be external stimulus from a pin (CINP and/or CINN) or internally generated signals. Both a programmable voltage reference and the temperature sensor output voltage are available internally. The output is available as an interrupt source or can be routed to an external pin.



Figure 20. Comparator Block Diagram

Operation

When the positive comparator input exceeds the negative input by more than the specified hysteresis, the output is a logic High. When the negative input exceeds the positive by more than the hysteresis, the output is a logic Low. Otherwise, the comparator output retains its present value. See <u>Table 141</u> on page 238 for details.

The comparator may be powered down to reduce supply current. See the <u>Power Control</u> <u>Register 0</u> section on page 33 for details.

Caution: Because of the propagation delay of the comparator, Zilog does not recommend enabling or reconfiguring the comparator without first disabling the interrupts and waiting for the comparator output to settle. Doing so can result in spurious interrupts.

Bit	Description (Continued)
[5:4] OSC_SEL[1:0]	 Oscillator Mode Selection 00 = On-chip oscillator configured for use with external RC networks (<4MHz). 01 = Minimum power for use with very low frequency crystals (32kHz to 1.0MHz). 10 = Medium power for use with medium frequency crystals or ceramic resonators (0.5MHz to 5.0MHz). 11 = Maximum power for use with high frequency crystals (5.0MHz to 20.0MHz). This setting is the default for unprogrammed (erased) Flash.
[3] VBO_AO	 Voltage Brown-Out Protection Always On 0 = Voltage Brown-Out Protection can be disabled in STOP Mode to reduce total power consumption. For the block to be disabled, the power control register bit must also be written (see the <u>Power Control Register Definitions</u> section on page 33). 1 = Voltage Brown-Out Protection is always enabled including during STOP Mode. This setting is the default for unprogrammed (erased) Flash.
[2] FRP	 Flash Read Protect 0 = User program code is inaccessible. Limited control features are available through the On-Chip Debugger. 1 = User program code is accessible. All On-Chip Debugger commands are enabled. This setting is the default for unprogrammed (erased) Flash.
[1]	Reserved This bit is reserved and must be programmed to 1.
[0] FWP	 Flash Write Protect This Option Bit provides Flash Program Memory protection: 0 = Programming and erasure disabled for all of Flash Program Memory. Programming, Page Erase and Mass Erase through User Code is disabled. Mass Erase is available using the On-Chip Debugger. 1 = Programming, Page Erase and Mass Erase are enabled for all of Flash program memory.

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Trim Bit Address Space

All available Trim bit addresses and their functions are listed in Table 90 through Table 95.

Trim Bit Address 0000H

Bit	7	6	5	4	3	2	1	0		
Field		Reserved								
RESET	U	U	U	U	U	U	U	U		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Address			Infor	mation Page	e Memory 00	020H				
Note: U =	Unchanged b	by Reset. R/W	/ = Read/Writ	e.						
Bit	Descriptio	n								
[7:0]	Reserved									

Table 90. Trim Options Bits at Address 0000H

These bits are reserved; altering this register may result in incorrect device operation.

Trim Bit Address 0001H

Table 91. Trim Option Bits at 0001H

Bit	7	6	5	4	3	2	1	0	
Field		Reserved							
RESET	U	U	U	U	U	U	U	U	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address	Information Page Memory 0021H								
Note: U =	Note: U = Unchanged by Reset. R/W = Read/Write.								

Bit Description [7:0] Reserved These bits are reserved; altering this register may result in incorrect device operation.

ADC Calibration Data

Table 96. ADC Calibration Bits

Bit	7	6	5	4	3	2	1	0	
Field				ADC	_CAL				
RESET	U	U	U	U	U	U	U	U	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address		Information Page Memory 0060H–007DH							
Noto: II -	Linchanged k		/ - Pood/Mrit	0					

Note: U = Unchanged by Reset. R/W = Read/Write.

Bit Description

[7:0] Analog-to-Digital Converter Calibration Values
 ADC_CAL Contains factory-calibrated values for ADC gain and offset compensation. Each of the ten supported modes has one byte of offset calibration and two bytes of gain calibration. These values are read by the software to compensate ADC measurements as described in the Software Compensation Procedure Using Factory Calibration Data section on page 129. The location of each calibration byte is provided in Table 97.

Info Page	Memory			
Address	Address	Compensation Usage	ADC Mode	Reference Type
60	FE60	Offset	Single-Ended Unbuffered	Internal 2.0 V
08	FE08	Gain High Byte	Single-Ended Unbuffered	Internal 2.0 V
09	FE09	Gain Low Byte	Single-Ended Unbuffered	Internal 2.0 V
63	FE63	Offset	Single-Ended Unbuffered	Internal 1.0 V
0A	FE0A	Gain High Byte	Single-Ended Unbuffered	Internal 1.0 V
0B	FE0B	Gain Low Byte	Single-Ended Unbuffered	Internal 1.0 V
66	FE66	Offset	Single-Ended Unbuffered	External 2.0 V
0C	FE0C	Gain High Byte	Single-Ended Unbuffered	External 2.0 V
0D	FE0D	Gain Low Byte	Single-Ended Unbuffered	External 2.0 V
69	FE69	Offset	Single-Ended 1x Buffered	Internal 2.0 V
0E	FE0E	Gain High Byte	Single-Ended 1x Buffered	Internal 2.0 V
0F	FE0F	Gain Low Byte	Single-Ended 1x Buffered	Internal 2.0 V
6C	FE6C	Offset	Single-Ended 1x Buffered	External 2.0 V
10	FE10	Gain High Byte	Single-Ended 1x Buffered	External 2.0 V
11	FE11	Gain Low Byte	Single-Ended 1x Buffered	External 2.0 V
6F	FE6F	Offset	Differential Unbuffered	Internal 2.0 V

Table 97. ADC Calibration Data Location

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Table 101. Watchdog Calibration Low Byte at 007FH (WDTCALL)

Bit	7	6	5	4	3	2	1	0		
Field		WDTCALL								
RESET	U	U	U	U	U	U	U	U		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Address	Information Page Memory 007FH									
Note: U =	Note: U = Unchanged by Reset. R/W = Read/Write.									

Bit	Description
[7:0]	Watchdog Timer Calibration Low Byte
WDTCALL	The WDTCALH and WDTCALL bytes, when loaded into the Watchdog Timer reload regis-
	ters result in a one second time-out at room temperature and 3.3V supply voltage. To use
	the Watchdog Timer calibration, user code must load WDTU with 0x00, WDTH with WDT-
	CALH and WDTL with WDTCALL.

Serialization Data

Table 102. Serial Number at 001C - 001F (S_NUM)

Bit	7	6	5	4	3	2	1	0
Field	S_NUM							
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Address Information Page Memory 001C-001F							
Note: U = Unchanged by Reset. R/W = Read/Write.								

Bit	Description
[7:0]	Serial Number Byte
S NUM	The serial number is a unique four-byte binary value. See Table 103.

Table 103. Serialization Data Locations

Info Page Address	Memory Address	Usage
1C	FE1C	Serial Number Byte 3 (most significant).
1D	FE1D	Serial Number Byte 2.
1E	FE1E	Serial Number Byte 1.
1F	FE1F	Serial Number Byte 0 (least significant).

Read Memory, Write Register, Read Register, Read Memory CRC, Step Instruction, Stuff Instruction and Execute Instruction commands.

DBG \leftarrow 03H DBG \rightarrow RuntimeCounter[15:8] DBG \rightarrow RuntimeCounter[7:0]

Write OCD Control Register (04H). The Write OCD Control Register command writes the data that follows to the OCDCTL Register. When the Flash Read Protect Option Bit is enabled, the DBGMODE bit (OCDCTL[7]) can only be set to 1, it cannot be cleared to 0 and the only method of returning the device to normal operating mode is to reset the device.

DBG \leftarrow 04H DBG \leftarrow OCDCTL[7:0]

Read OCD Control Register (05H). The Read OCD Control Register command reads the value of the OCDCTL Register.

DBG \leftarrow 05H DBG \rightarrow OCDCTL[7:0]

Write Program Counter (06H). The Write Program Counter command writes the data that follows to the eZ8 CPU's Program Counter (PC). If the device is not in DEBUG Mode or if the Flash Read Protect Option bit is enabled, the Program Counter (PC) values are discarded.

DBG ← 06H
DBG ← ProgramCounter[15:8]
DBG ← ProgramCounter[7:0]

Read Program Counter (07H). The Read Program Counter command reads the value in the eZ8 CPU's Program Counter (PC). If the device is not in DEBUG Mode or if the Flash Read Protect Option bit is enabled, this command returns FFFFH.

```
DBG \leftarrow 07H
DBG \rightarrow ProgramCounter[15:8]
DBG \rightarrow ProgramCounter[7:0]
```

Write Register (08H). The Write Register command writes data to the Register File. Data can be written 1–256 bytes at a time (256 bytes can be written by setting size to 0). If the device is not in DEBUG Mode, the address and data values are discarded. If the Flash Read Protect Option bit is enabled, only writes to the Flash Control registers are allowed and all other register write data values are discarded.

DBG \leftarrow 08H DBG \leftarrow {4'h0,Register Address[11:8]} DBG \leftarrow Register Address[7:0] DBG \leftarrow Size[7:0] DBG \leftarrow 1-256 data bytes

eZ8 CPU Instruction Summary

Table 128 summarizes the eZ8 CPU instructions. The table identifies the addressing modes employed by the instruction, the effect upon the Flags Register, the number of CPU clock cycles required for the instruction fetch and the number of CPU clock cycles required for the instruction.

Assembly		Add Mc	ress ode	_ Opcode(s)			Fla	ags			Fetch Cvcle	Instr. Cvcle
Mnemonic	Symbolic Operation	dst	src	(Hex)	С	Ζ	S	۷	D	Н	S	S
ADC dst, src	$dst \gets dst + src + C$	r	r	12	*	*	*	*	0	*	2	3
		r	lr	13	-						2	4
		R	R	14							3	3
		R	IR	15							3	4
		R	IM	16							3	3
		IR	IM	17							3	4
ADCX dst, src	$dst \gets dst + src + C$	ER	ER	18	*	*	*	*	0	*	4	3
		ER	IM	19							4	3
ADD dst, src	$dst \leftarrow dst + src$	r	r	02	*	*	*	*	0	*	2	3
		r	lr	03	-						2	4
		R	R	04	-						3	3
		R	IR	05	-						3	4
		R	IM	06	-						3	3
		IR	IM	07							3	4
ADDX dst, src	$dst \gets dst + src$	ER	ER	08	*	*	*	*	0	*	4	3
		ER	IM	09	-						4	3

Table 128. eZ8 CPU Instruction Summary

Note: Flags Notation: * = Value is a function of the result of the operation.

- = Unaffected.

X = Undefined.

0 = Reset to 0.

1 = Set to 1.

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On-Chip Debugger Timing

Figure 36 and Table 145 provide timing information for the DBG pin. The DBG pin timing specifications assume a 4 ns maximum rise and fall time.



Figure 36. On-Chip Debugger Timing

		Delay (ns)					
Parameter	Abbreviation	Minimum	Maximum				
DBG							
T ₁	X _{IN} Rise to DBG Valid Delay	_	15				
T ₂	X _{IN} Rise to DBG Output Hold Time	2	_				
T ₃	DBG to XIN Rise Input Setup Time	5	_				
T ₄	DBG to XIN Rise Input Hold Time	5	_				

Table 145. On-Chip Debugger Timing