



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, Temp Sensor, WDT
Number of I/O	6
Program Memory Size	1KB (1K × 8)
Program Memory Type	FLASH
EEPROM Size	16 × 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	8-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f012apb020eg

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

ADC Data High Byte Register	. 136 . 137
Low Power Operational Amplifier	. 139 . 139
Comparator	. 140 . 140 . 141
Temperature Sensor Temperature Sensor Operation	. 144 . 144
Flash Memory Architecture Flash Information Area Operation Flash Operation Timing Using the Flash Frequency Registers	. 146 . 146 . 147 . 147 . 149
Flash Code Protection Against External Access Flash Code Protection Against Accidental Program and Erasure Byte Programming	. 149 . 149 151
Dyte Programming Page Erase Mass Erase The information in the programming	. 151 . 152 . 152
Flash Controller Bypass Flash Controller Behavior in DEBUG Mode Flash Control Register Definitions Flash Control Register Definitions	. 152 . 153 . 153
Flash Control Register Flash Status Register	. 153 . 153 . 155
Flash Page Select Register Flash Sector Protect Register Elash Frequency High and Low Byte Registers	. 156 . 157 . 157
Flash Option Bits	. 157
Operation Option Bit Configuration By Reset Option Bit Types	. 159 . 159 . 160
Flash Option Bit Control Register Definitions	. 161 . 161 . 161
Trim Bit Data Register	. 161 . 162 . 162
Flash Program Memory Address 0000HFlash Program Memory Address 0001H	. 162 . 164
Trim Bit Address Space	. 165

)	Table 4. Pin Characteristics (8-Pin Devices)										
Symbol Mnemonic	Direction	Reset Direction	Active Low or Active High	Tristate Output	Internal Pull-up or Pull-down	Schmitt- Trigger Input	Open Drain Output	5V Tolerance			
PA0/DBG	I/O	I (but can change during reset if key sequence detected)	N/A	Yes	Programma- ble Pull-up	Yes	Yes, Programma- ble	Yes, unless pull-ups enabled			
PA1	I/O	I	N/A	Yes	Programma- ble Pull-up	Yes	Yes, Programma- ble	Yes, unless pull-ups enabled			
RESET/ PA2	I/O	I/O (defaults to RESET)	Low (in Reset mode)	Yes	Programma- ble for PA2; alw <u>ays on f</u> or RESET	Yes	Programma- ble for PA2; alw <u>ays on f</u> or RESET	Yes, unless pull-ups enabled			
PA[5:3]	I/O	I	N/A	Yes	Programma- ble Pull-up	Yes	Yes, Programma- ble	Yes, unless pull-ups enabled			
V _{DD}	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A			
V _{SS}	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A			

Register Map

Table 7 provides the address map for the Register File of the Z8 Encore! XP F082A Series devices. Not all devices and package styles in the Z8 Encore! XP F082A Series support the ADC, or all of the GPIO Ports. Consider registers for unimplemented peripherals as Reserved.

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page
General-Purpos	e RAM			
Z8F082A/Z8F08	1A Devices			
000–3FF	General-Purpose Register File RAM	—	XX	
400–EFF	Reserved	—	XX	
Z8F042A/Z8F04	1A Devices			
000–3FF	General-Purpose Register File RAM	—	XX	
400–EFF	Reserved	—	XX	
Z8F022A/Z8F02	1A Devices			
000–1FF	General-Purpose Register File RAM	—	XX	
200–EFF	Reserved	—	XX	
Z8F012A/Z8F01	1A Devices			
000–0FF	General-Purpose Register File RAM	_	XX	
100–EFF	Reserved	—	XX	
Timer 0				
F00	Timer 0 High Byte	T0H	00	<u>90</u>
F01	Timer 0 Low Byte	TOL	01	<u>90</u>
F02	Timer 0 Reload High Byte	TORH	FF	<u>91</u>
F03	Timer 0 Reload Low Byte	TORL	FF	<u>91</u>
F04	Timer 0 PWM High Byte	TOPWMH	00	<u>92</u>
F05	Timer 0 PWM Low Byte	TOPWML	00	<u>92</u>
F06	Timer 0 Control 0	T0CTL0	00	<u>85</u>
F07	Timer 0 Control 1	T0CTL1	00	<u>86</u>
Notoo:				

Table 7. Register File Address Map

Notes: 1. XX = Undefined.

2. Refer to the <u>eZ8</u> CPU <u>Core User Manual (UM0128)</u>.



Figure 6. Voltage Brown-Out Reset Operation

The POR level is greater than the VBO level by the specified hysteresis value. This ensures that the device undergoes a Power-On Reset after recovering from a VBO condition.

Watchdog Timer Reset

If the device is operating in NORMAL or HALT Mode, the Watchdog Timer can initiate a System Reset at time-out if the WDT_RES Flash option bit is programmed to 1, i.e., the unprogrammed state of the WDT_RES Flash option bit. If the bit is programmed to 0, it configures the Watchdog Timer to cause an interrupt, not a System Reset, at time-out.

The WDT bit in the Reset Status (RSTSTAT) Register is set to signify that the reset was initiated by the Watchdog Timer.

External Reset Input

The $\overline{\text{RESET}}$ pin has a Schmitt-Triggered input and an internal pull-up resistor. Once the $\overline{\text{RESET}}$ pin is asserted for a minimum of four system clock cycles, the device progresses through the System Reset sequence. Because of the possible asynchronicity of the system clock and reset signals, the required reset duration may be as short as three clock periods

• Writing a 1 to the IRQE bit in the Interrupt Control Register

Interrupts are globally disabled by any of the following actions:

- Execution of a Disable Interrupt (DI) instruction
- eZ8 CPU acknowledgement of an interrupt service request from the interrupt controller
- Writing a 0 to the IRQE bit in the Interrupt Control Register
- Reset
- Execution of a Trap instruction
- Illegal Instruction Trap
- Primary Oscillator Fail Trap
- Watchdog Oscillator Fail Trap

Interrupt Vectors and Priority

The interrupt controller supports three levels of interrupt priority. Level 3 is the highest priority, Level 2 is the second highest priority and Level 1 is the lowest priority. If all of the interrupts are enabled with identical interrupt priority (all as Level 2 interrupts, for example), the interrupt priority is assigned from highest to lowest as specified in <u>Table 34</u> on page 56. Level 3 interrupts are always assigned higher priority than Level 2 interrupts which, in turn, always are assigned higher priority than Level 1 interrupts. Within each interrupt priority level (Level 1, Level 2, or Level 3), priority is assigned as specified in Table 34, above. Reset, Watchdog Timer interrupt (if enabled), Primary Oscillator Fail Trap, Watchdog Oscillator Fail Trap and Illegal Instruction Trap always have highest (level 3) priority.

Interrupt Assertion

Interrupt sources assert their interrupt requests for only a single system clock period (single pulse). When the interrupt request is acknowledged by the eZ8 CPU, the corresponding bit in the Interrupt Register is cleared until the next interrupt occurs. Writing a 0 to the corresponding bit in the Interrupt Request Register likewise clears the interrupt request.

Caution: Zilog recommends not using a coding style that clears bits in the Interrupt Request registers. All incoming interrupts received between execution of the first LDX command and the final LDX command are lost. See Example 1, which follows. delay ensures a time gap between the deassertion of one PWM output to the assertion of its complement.

Observe the following steps for configuring a timer for PWM DUAL OUTPUT Mode and initiating the PWM operation:

- 1. Write to the Timer Control Register to:
 - Disable the timer
 - Configure the timer for PWM DUAL OUTPUT Mode by writing the TMODE bits in the TxCTL1 Register and the TMODEHI bit in TxCTL0 Register
 - Set the prescale value
 - Set the initial logic level (High or Low) and PWM High/Low transition for the Timer Output alternate function
- 2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H). This only affects the first pass in PWM mode. After the first timer reset in PWM mode, counting always begins at the reset value of 0001H.
- 3. Write to the PWM High and Low Byte registers to set the PWM value.
- 4. Write to the PWM Control Register to set the PWM dead band delay value. The deadband delay must be less than the duration of the positive phase of the PWM signal (as defined by the PWM high and low byte registers). It must also be less than the duration of the negative phase of the PWM signal (as defined by the difference between the PWM registers and the Timer Reload registers).
- 5. Write to the Timer Reload High and Low Byte registers to set the reload value (PWM period). The reload value must be greater than the PWM value.
- 6. If appropriate, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
- 7. Configure the associated GPIO port pin for the Timer Output and Timer Output Complement alternate functions. The Timer Output Complement function is shared with the Timer Input function for both timers. Setting the timer mode to Dual PWM automatically switches the function from Timer In to Timer Out Complement.
- 8. Write to the Timer Control Register to enable the timer and initiate counting.

The PWM period is represented by the following equation:

PWM Period (s) = $\frac{\text{Reload Value xPrescale}}{\text{System Clock Frequency (Hz)}}$

If an initial starting value other than 0001H is loaded into the Timer High and Low Byte registers, the ONE-SHOT Mode equation determines the first PWM time-out period.

Watchdog Timer Reload Upper, High and Low Byte Registers

The Watchdog Timer Reload Upper, High and Low Byte (WDTU, WDTH, WDTL) registers, shown in Tables 60 through 62, form the 24-bit reload value that is loaded into the Watchdog Timer when a WDT instruction executes. The 24-bit reload value ranges across bits [23:0] to encompass the three bytes {WDTU[7:0], WDTH[7:0], WDTL[7:0]}. Writing to these registers sets the appropriate reload value. Reading from these registers returns the current Watchdog Timer count value.

Caution: The 24-bit WDT reload value must not be set to a value less than 000004H.

Bit	7	6	5	4	3	2	1	0		
Field		WDTU								
RESET		00H								
R/W		R/W*								
Address				FF	1H					
Note: A re	Note: A read returns the current WDT count value; a write sets the appropriate reload value.									

Table 60. Watchdog Timer Reload Upper Byte Register (WDTU)

Bit	Description
[7:0]	WDT Reload Upper Byte
WDTU	Most-significant byte (MSB): bits[23:16] of the 24-bit WDT reload value.

Table 61. Watchdog Timer Reload High Byte Register (WDTH)

Bit	7	6	5	4	3	2	1	0
Field	WDTH							
RESET		04H						
R/W	R/W*							
Address				FF	2H			
Note: A re	ad returns th	e current WD	T count value	e; a write sets	the appropria	ate reload val	ue.	

Bit	Description
[7:0]	WDT Reload High Byte
WDTH	Middle byte; bits[15:8] of the 24-bit WDT reload value.

Bit	7	6	5	4	3	2	1	0		
Field	MPMD[1]	MPEN		MPBT	DEPOL		RDAIRQ	IREN		
RESET	0	0	0	0	0	0	0	0		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Address				F4	3H					
Bit Description										
[6] MPEN	 [7,5] MULTIPROCESSOR Mode MPMD[1,0] If MULTIPROCESSOR (9-bit) Mode is enabled: 00 = The UART generates an interrupt request on all received bytes (data and address). 01 = The UART generates an interrupt request only on received address bytes. 10 = The UART generates an interrupt request when a received address byte matches the value stored in the Address Compare Register and on all successive data bytes until an address mismatch occurs. 11 = The UART generates an interrupt request on all received data bytes for which the most recent address byte matched the value in the Address Compare Register. [6] MULTIPROCESSOR (9-bit) Enable MPEN This bit is used to enable MULTIPROCESSOR (9-bit) Mode. 0 = Disable MULTIPROCESSOR (9-bit) Mode. 									
[4] MPBT	Multipro This bit is used by tion. 0 = Senc 1 = Senc	cessor Bit s applicable the receiving a 0 in the r a 1 in the r	Transmit only when M g device to c nultiprocess nultiprocess	MULTIPROC determine if or bit locatic or bit locatic	EESSOR (9- the data byte on of the data	bit) Mode is e contains a a stream (da a stream (ac	enabled. Th ddress or da ata byte). ddress byte).	ne 9th bit is ata informa-		
DEPOL	0 = DE s 1 = DE s	ignal is Acti	ve High. ve Low.							

Table 64. UART Control 1 Register (U0CTL1)

Low Power Operational Amplifier

The LPO is a general-purpose low power operational amplifier. Each of the three ports of the amplifier is accessible from the package pins. The LPO contains only one pin configuration: ANA0 is the output/feedback node, ANA1 is the inverting input and ANA2 is the noninverting input.

Operation

To use the LPO, it must be enabled in the Power Control Register 0 (PWRCTL0). The default state of the LPO is OFF. To use the LPO, the LPO bit must be cleared by turning it ON (for details, see the <u>Power Control Register 0</u> section on page 33). When making normal ADC measurements on ANA0 (i.e., measurements not involving the LPO output), the LPO bit must be turned OFF. Turning the LPO bit ON interferes with normal ADC measurements.

Caution: The LPO bit enables the amplifier even in STOP Mode. If the amplifier is not required in STOP Mode, disable it. Failing to perform this results in STOP Mode currents higher than necessary.

As with other ADC measurements, any pins used for analog purposes must be configured as such in the GPIO registers. See the <u>Port A–D Alternate Function Subregisters</u> section on page 47 for details.

LPO output measurements are made on ANA0, as selected by the ANAIN[3:0] bits of ADC Control Register 0. It is also possible to make single-ended measurements on ANA1 and ANA2 while the amplifier is enabled, which is often useful for determining offset conditions. Differential measurements between ANA0 and ANA2 may be useful for noise cancellation purposes.

If the LPO output is routed to the ADC, then the BUFFMODE[2:0] bits of ADC Control/Status Register 1 must also be configured for unity-gain buffered operation. Sampling the LPO in an unbuffered mode is not recommended.

When either input is overdriven, the amplifier output saturates at the positive or negative supply voltage. No instability results.

Caution: The byte at each address of the Flash memory cannot be programmed (any bits written to 0) more than twice before an erase cycle occurs. Doing so may result in corrupted data at the target byte.

Page Erase

The Flash memory can be erased one page (512 bytes) at a time. Page Erasing the Flash memory sets all bytes in that page to the value FFH. The Flash Page Select Register identifies the page to be erased. Only a page residing in an unprotected sector can be erased. With the Flash Controller unlocked and the active page set, writing the value 95h to the Flash Control Register initiates the Page Erase operation. While the Flash Controller executes the Page Erase operation, the eZ8 CPU idles but the system clock and on-chip peripherals continue to operate. The eZ8 CPU resumes operation after the Page Erase operation completes. If the Page Erase operation is performed using the On-Chip Debugger, poll the Flash Status Register to determine when the Page Erase operation is complete. When the Page Erase is complete, the Flash Controller returns to its locked state.

Mass Erase

The Flash memory can also be Mass Erased using the Flash Controller, but only by using the On-Chip Debugger. Mass Erasing the Flash memory sets all bytes to the value FFH. With the Flash Controller unlocked and the Mass Erase successfully enabled, writing the value 63H to the Flash Control Register initiates the Mass Erase operation. While the Flash Controller executes the Mass Erase operation, the eZ8 CPU idles but the system clock and on-chip peripherals continue to operate. Using the On-Chip Debugger, poll the Flash Status Register to determine when the Mass Erase operation is complete. When the Mass Erase is complete, the Flash Controller returns to its locked state.

Flash Controller Bypass

The Flash Controller can be bypassed and the control signals for the Flash memory brought out to the GPIO pins. Bypassing the Flash Controller allows faster Row Programming algorithms by controlling the Flash programming signals directly.

Row programming is recommended for gang programming applications and large volume customers who do not require in-circuit initial programming of the Flash memory. Page Erase operations are also supported when the Flash Controller is bypassed.

For more information about bypassing the Flash Controller, refer to the <u>Third-Party Flash</u> <u>Programming Support for Z8 Encore! MCUs Application Note (AN0117)</u>, which is available for download on <u>www.zilog.com</u>.

Bit	7	6	5	4	3	2	1	0	
Field		FCMD							
RESET	0	0	0	0	0	0	0	0	
R/W	W	W	W	W	W	W	W	W	
Address				FF	8H				

Table 80. Flash Control Register (FCTL)

Bit	Description
DIL	Description

[7:0] Flash Command

FCMD 73H = First unlock command.

8CH = Second unlock command.

95H = Page Erase command (must be third command in sequence to initiate Page Erase).

63H = Mass Erase command (must be third command in sequence to initiate Mass Erase).

5EH = Enable Flash Sector Protect Register Access

Flash Status Register

The Flash Status (FSTAT) Register indicates the current state of the Flash Controller. This register can be read at any time. The read-only Flash Status Register shares its Register File address with the Write-only Flash Control Register.

Table 81. Flash Status Register (FSTAT)

Bit	7	6	5	4	3	2	1	0
Field Reserved		FSTAT						
RESET	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R
Address	FF8H							

Bit	Description
[7:6]	These bits are reserved and must be programmed to 00.
[5:0] FSTAT	Flash Controller Status000000 = Flash Controller locked.000001 = First unlock command received (73H written).000010 = Second unlock command received (8CH written).000011 = Flash Controller unlocked.000100 = Sector protect register selected.001xxx = Program operation in progress.010xxx = Page erase operation in progress.100xxx = Mass erase operation in progress.

Temperature Sensor Calibration Data

Table 98. Temperature Sensor Calibration High Byte at 003A (TSCALH)

Bit	7	6	5	4	3	2	1	0				
Field	TSCALH											
RESET	U	U	U	U	U	U	U	U				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				
Address	Information Page Memory 003A											
Note: U =	Unchanged b	by Reset. R/W	/ = Read/Writ	e.								

Bit Description [7:0] **Temperature Sensor Calibration High Byte** TSCALH The TSCALH and TSCALL bytes combine to form the 12-bit temperature sensor offset calibra-

tion value. For more details, see Temperature Sensor Operation on page 139.

Table 99. Temperature Sensor Calibration Low Byte at 003B (TSCALL)

Bit	7	6	5	4	3	2	1	0				
Field	TSCALL											
RESET	U	U			U	U						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				
Address	Information Page Memory 003B											
Note: U =	Unchanged b	by Reset. R/W	/ = Read/Writ	e.								

Bit Description

[7:0]	Temperature Sensor Calibration Low Byte
TSCALL	The TSCALH and TSCALL bytes combine to form the 12-bit temperature sensor offset calibra-
	tion value. For usage details, see the <u>Temperature Sensor Operation</u> section on page 144.

Nonvolatile Data Storage

The Z8 Encore! XP F082A Series devices contain a nonvolatile data storage (NVDS) element of up to 128 bytes. This memory can perform over 100,000 write cycles.

Operation

The NVDS is implemented by special purpose Zilog software stored in areas of program memory, which are not user-accessible. These special-purpose routines use the Flash memory to store the data. The routines incorporate a dynamic addressing scheme to maximize the write/erase endurance of the Flash.

Note: Different members of the Z8 Encore! XP F082A Series feature multiple NVDS array sizes; see the <u>Part Selection Guide</u> section on page 2 for details. Devices containing 8KB of Flash memory do not include the NVDS feature.

NVDS Code Interface

Two routines are required to access the NVDS: a write routine and a read routine. Both of these routines are accessed with a CALL instruction to a predefined address outside of the user-accessible program memory. Both the NVDS address and data are single-byte values. Because these routines disturb the working register set, user code must ensure that any required working register values are preserved by pushing them onto the stack or by changing the working register pointer just prior to NVDS execution.

During both read and write accesses to the NVDS, interrupt service is NOT disabled. Any interrupts that occur during the NVDS execution must take care not to disturb the working register and existing stack contents or else the array may become corrupted. Disabling interrupts before executing NVDS operations is recommended.

Use of the NVDS requires 15 bytes of available stack space. Also, the contents of the working register set are overwritten.

For correct NVDS operation, the Flash Frequency registers must be programmed based on the system clock frequency (see **the** <u>Flash Operation Timing Using the Flash Frequency</u> <u>Registers</u> **section on page 149**).

enabled, the OCD ignores the BRK signal and the BRK instruction operates as an NOP instruction.

Breakpoints in Flash Memory

The BRK instruction is opcode 00H, which corresponds to the fully programmed state of a byte in Flash memory. To implement a Breakpoint, write 00H to the required break address, overwriting the current instruction. To remove a Breakpoint, the corresponding page of Flash memory must be erased and reprogrammed with the original data.

Runtime Counter

The On-Chip Debugger contains a 16-bit Runtime Counter. It counts system clock cycles between Breakpoints. The counter starts counting when the On-Chip Debugger leaves DEBUG Mode and stops counting when it enters DEBUG Mode again or when it reaches the maximum count of FFFFH.

On-Chip Debugger Commands

The host communicates to the on-chip debugger by sending OCD commands using the DBG interface. During normal operation, only a subset of the OCD commands are available. In DEBUG Mode, all OCD commands become available unless the user code and control registers are protected by programming the Flash Read Protect Option bit (FRP). The Flash Read Protect Option bit prevents the code in memory from being read out of the Z8 Encore! XP F082A Series device. When this option is enabled, several of the OCD commands are disabled. See Table 109.

<u>Table 110</u> on page 191 is a summary of the on-chip debugger commands. Each OCD command is described in further detail in the bulleted list following this table. Table 110 also indicates those commands that operate when the device is not in DEBUG Mode (normal operation) and those commands that are disabled by programming the Flash Read Protect Option bit.

Debug Command	Command Byte	Enabled when Not in DEBUG Mode?	Disabled by Flash Read Protect Option Bit
Read OCD Revision	00H	Yes	-
Reserved	01H	-	-
Read OCD Status Register	02H	Yes	-
Read Runtime Counter	03H	_	-
Write OCD Control Register	04H	Yes	Cannot clear DBGMODE bit.
Read OCD Control Register	05H	Yes	_

Table 109.	Debug	Command	Enable/Disabl	e
				_

Oscillator Control

The Z8 Encore! XP F082A Series devices uses five possible clocking schemes, each user-selectable:

- Internal precision trimmed RC oscillator (IPO)
- On-chip oscillator using off-chip crystal or resonator
- On-chip oscillator using external RC network
- External clock drive
- On-chip low power Watchdog Timer oscillator
- Clock failure detection circuitry

In addition, Z8 Encore! XP F082A Series devices contain clock failure detection and recovery circuitry, allowing continued operation despite a failure of the system clock oscillator.

Operation

This chapter discusses the logic used to select the system clock and handle primary oscillator failures.

System Clock Selection

The oscillator control block selects from the available clocks. Table 112 details each clock source and its usage.

Register file size varies depending on the device type. See the device-specific Z8 Encore! XP Product Specification to determine the exact register file range available.

eZ8 CPU Instruction Notation

In the eZ8 CPU Instruction Summary and Description sections, the operands, condition codes, status flags and address modes are represented by a notational shorthand that is described in Table 118.

Notation	Description	Operand	Range
b	Bit	b	b represents a value from 0 to 7 (000B to 111B).
CC	Condition code	—	Refer to the Condition Codes section in the <u>eZ8</u> <u>CPU Core User Manual (UM0128)</u> .
DA	Direct address	Addrs	Represents a number in the range 0000H to FFFFH.
ER	Extended addressing register	Reg	Reg. represents a number in the range of 000H to FFFH.
IM	Immediate data	#Data	Data is a number between 00H to FFH.
lr	Indirect working register	@Rn	n = 0–15.
IR	Indirect register	@Reg	Reg. represents a number in the range of 00H to FFH.
Irr	Indirect working register pair	@RRp	p = 0, 2, 4, 6, 8, 10, 12, or 14.
IRR	Indirect register pair	@Reg	Reg. represents an even number in the range 00H to FEH.
р	Polarity	р	Polarity is a single bit binary value of either 0B or 1B.
r	Working register	Rn	n = 0 - 15.
R	Register	Reg	Reg. represents a number in the range of 00H to FFH.
RA	Relative address	Х	X represents an index in the range of +127 to – 128 which is an offset relative to the address of the next instruction.
rr	Working register pair	RRp	p = 0, 2, 4, 6, 8, 10, 12, or 14.
RR	Register pair	Reg	Reg. represents an even number in the range of 00H to FEH.

Table 118. Notational Shorthand

Assembly		Add Mo	ress de	_ Opcode(s)			Fla	ags			Fetch Cvcle	Instr. Cvcle
Mnemonic	Symbolic Operation	dst	src	(Hex)	С	Ζ	S	V	D	Н	S	S
DA dst	$dst \leftarrow DA(dst)$	R		40	*	*	*	Х	_	_	2	2
		IR		41	-						2	3
DEC dst	dst ← dst - 1	R		30	-	*	*	*	-	-	2	2
		IR		31	-						2	3
DECW dst	dst ← dst - 1	RR		80	-	*	*	*	-	-	2	5
		IRR		81	-						2	6
DI	$IRQCTL[7] \leftarrow 0$			8F	-	_	_	-	-	-	1	2
DJNZ dst, RA	$dst \leftarrow dst - 1$ if dst $\neq 0$ PC \leftarrow PC + X	r		0A-FA	_	_	_	_	_	_	2	3
EI	$IRQCTL[7] \leftarrow 1$			9F	-	-	-	-	-	-	1	2
HALT	Halt Mode			7F	_	-	-	-	-	-	1	2
INC dst	dst ← dst + 1	R		20	_	*	*	-	_	_	2	2
		IR		21	-						2	3
		r		0E-FE	-						1	2
INCW dst	dst ← dst + 1	RR		A0	_	*	*	*	_	_	2	5
		IRR		A1	-						2	6
IRET	$FLAGS \leftarrow @SP$ $SP \leftarrow SP + 1$ $PC \leftarrow @SP$ $SP \leftarrow SP + 2$ $IRQCTL[7] \leftarrow 1$			BF	*	*	*	*	*	*	1	5
JP dst	$PC \leftarrow dst$	DA		8D	-	-	-	-	-	-	3	2
		IRR		C4	-						2	3
JP cc, dst	if cc is true PC \leftarrow dst	DA		0D-FD	-	-	-	-	-	-	3	2

Table 128. eZ8 CPU Instruction Summary (Continued)

Note: Flags Notation:

* = Value is a function of the result of the operation.

- = Unaffected.

X = Undefined.

0 = Reset to 0.

1 =Set to 1.

Assembly		Add Mc	lress ode	_ Opcode(s)			Fla	ags			Fetch Cvcle	Instr. Cvcle
Mnemonic	Symbolic Operation	dst	src	(Hex)	С	Ζ	S	۷	D	Н	S	S
ORX dst, src	$dst \gets dst \ OR \ src$	ER	ER	48	-	*	*	0	_	_	4	3
		ER	IM	49	-						4	3
POP dst	dst ← @SP	R		50	_	_	_	_	_	_	2	2
	$SP \leftarrow SP + 1$	IR		51	-						2	3
POPX dst	dst $\leftarrow @SP$ SP \leftarrow SP + 1	ER		D8	-	-	-	-	-	-	3	2
PUSH src	$SP \leftarrow SP - 1$	R		70	-	_	_	-	_	_	2	2
	$@SP \leftarrow src$	IR		71	-						2	3
		IM		IF70	-						3	2
PUSHX src	$SP \leftarrow SP - 1$ @SP ← src	ER		C8	-	_	_	-	-	_	3	2
RCF	C ← 0			CF	0	-	-	-	-	_	1	2
RET	$\begin{array}{l} PC \leftarrow @SP \\ SP \leftarrow SP + 2 \end{array}$			AF	-	_	_	-	-	_	1	4
RL dst		R		90	*	*	*	*	-	-	2	2
	C	IR		91	-						2	3
RLC dst		R		10	*	*	*	*	_	_	2	2
	└─ <u> </u> C ← D7 D6 D5 D4 D3 D2 D1 D0 ← ^J dst	IR		11	-						2	3
RR dst]	R		E0	*	*	*	*	_	_	2	2
	► D7 D6 D5 D4 D3 D2 D1 D0 C	IR		E1	-						2	3

Table 128. eZ8 CPU Instruction Summary (Continued)

Note: Flags Notation:

* = Value is a function of the result of the operation.

- = Unaffected.

X = Undefined.

0 = Reset to 0.

1 = Set to 1.

Figure 33 displays the typical current consumption while operating with all peripherals disabled, at 30 °C, versus the system clock frequency.



Figure 33. Typical Active Mode I_{DD} Versus System Clock Frequency

		T _A =	–40°C to +			
Symbo	ol Parameter	Minimum	Typical ¹	Maximum	Units	Conditions
T _{RAMP}	Time for V_{DD} to transition from V_{SS} to V_{POR} to ensure valid Reset	0.10	-	100	ms	
T _{SMP}	Stop Mode Recovery pin pulse rejection period		20		ns	For any SMR pin or for the Reset pin when it is asserted in STOP Mode.
Note:	Data in the typical column is from character	rization at 3.3	/ and 30°C. 1	hese values a	re provid	ed for design

Table 135. Power-On Reset and Voltage Brown-Out Electrical Characteristics and Timing

ng
l

	V _{DD} = 2.7 V to 3.6 V T _A = -40°C to +105°C (unless otherwise stated)				
Parameter	Minimum	Typical	Maximum	Units	Notes
Flash Byte Read Time	100	_	_	ns	
Flash Byte Program Time	20	_	40	μs	
Flash Page Erase Time	10	_	-	ms	
Flash Mass Erase Time	200	_	_	ms	
Writes to Single Address Before Next Erase	-	-	2		
Flash Row Program Time	-	-	8	ms	Cumulative program time for single row cannot exceed limit before next erase. This parameter is only an issue when bypassing the Flash Controller.
Data Retention	100	_	_	years	25°C
Endurance	10,000	_	_	cycles	Program/erase cycles