

Welcome to **E-XFL.COM**

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, Temp Sensor, WDT
Number of I/O	6
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	16 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	8-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f012apb020sg

List of Tables

Table 1.	Z8 Encore! XP F082A Series Family Part Selection Guide
Table 2.	Signal Descriptions
Table 3.	Pin Characteristics (20- and 28-pin Devices)
Table 4.	Pin Characteristics (8-Pin Devices)
Table 5.	Z8 Encore! XP F082A Series Program Memory Maps
Table 6.	Z8 Encore! XP F082A Series Flash Memory Information Area Map 1
Table 7.	Register File Address Map
Table 8.	Reset and Stop Mode Recovery Characteristics and Latency
Table 9.	Reset Sources and Resulting Reset Type
Table 10.	Stop Mode Recovery Sources and Resulting Action
Table 11.	Reset Status Register (RSTSTAT)
Table 12.	Reset and Stop Mode Recovery Bit Descriptions
Table 13.	Power Control Register 0 (PWRCTL0)
Table 14.	Port Availability by Device and Package Type
Table 15.	Port Alternate Function Mapping (Non 8-Pin Parts)
Table 16.	Port Alternate Function Mapping (8-Pin Parts)
Table 17.	GPIO Port Registers and Subregisters
Table 18.	Port A–D GPIO Address Registers (PxADDR)
Table 19.	Port A–D GPIO Address Registers by Bit Description
Table 20.	Port A–D Control Registers (PxCTL)
Table 21.	Port A–D Data Direction Subregisters (PxDD)
Table 22.	Port A–D Alternate Function Subregisters (PxAF)
Table 23.	Port A–D Output Control Subregisters (PxOC)
Table 24.	Port A–D High Drive Enable Subregisters (PxHDE)
Table 25.	Port A–D Stop Mode Recovery Source Enable Subregisters (PxSMRE) 49
Table 26.	Port A–D Pull-Up Enable Subregisters (PxPUE)
Table 27.	Port A–D Alternate Function Set 2 Subregisters (PxAFS2) 5
Table 28.	Port A–D Alternate Function Set 1 Subregisters (PxAFS1) 5

Table 7. Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page	
Timer 1					
F08	Timer 1 High Byte	T1H	00	90	
F09	Timer 1 Low Byte	T1L	01	<u>90</u>	
F0A	Timer 1 Reload High Byte	T1RH	FF	<u>91</u>	
Timer 1 (cont'o	1)				
F0B	Timer 1 Reload Low Byte	T1RL	FF	<u>91</u>	
F0C	Timer 1 PWM High Byte	T1PWMH	00	<u>92</u>	
F0D	Timer 1 PWM Low Byte	T1PWML	00	<u>92</u>	
F0E	Timer 1 Control 0	T1CTL0	00	<u>85</u>	
F0F	Timer 1 Control 1	T1CTL1	00	<u>86</u>	
F10-F6F	Reserved	_	XX		
UART					
F40	UART Transmit/Receive Data registers	TXD, RXD	XX	<u>115</u>	
F41	UART Status 0 Register	U0STAT0	00	<u>114</u>	
F42	UART Control 0 Register	U0CTL0	00	<u>110</u>	
F43	UART Control 1 Register	U0CTL1	00	<u>110</u>	
F44	UART Status 1 Register	U0STAT1	00	<u>115</u>	
F45	UART Address Compare Register	U0ADDR	00	<u>116</u>	
F46	UART Baud Rate High Byte Register	U0BRH	FF	<u>117</u>	
F47	UART Baud Rate Low Byte Register	U0BRL	FF	<u>117</u>	
Analog-to-Digi	tal Converter (ADC)				
F70	ADC Control 0	ADCCTL0	00	<u>134</u>	
F71	ADC Control 1	ADCCTL1	80	<u>136</u>	
F72	ADC Data High Byte	ADCD_H	XX	<u>137</u>	
F73	ADC Data Low Byte	ADCD_L	XX	<u>137</u>	
F74–F7F	Reserved		XX		
Low Power Co	ntrol				
F80	Power Control 0	PWRCTL0	80	<u>34</u>	
F81	Reserved		XX		
LED Controller					
F82	LED Drive Enable	LEDEN	00	<u>53</u>	
F83	LED Drive Level High Byte	LEDLVLH	00	<u>53</u>	
F84	LED Drive Level Low Byte	LEDLVLL	00	<u>54</u>	

- 1. XX = Undefined.
- 2. Refer to the <u>eZ8 CPU Core User Manual (UM0128)</u>.

Table 8. Reset and Stop Mode Recovery Characteristics and Latency

	Reset Characteristics and Latency					
Reset Type	Control Registers	eZ8 CPU	Reset Latency (Delay)			
System Reset	Reset (as applicable)	Reset	66 Internal Precision Oscillator Cycles			
System Reset with Crystal Oscillator Enabled	Reset (as applicable)	Reset	5000 Internal Precision Oscillator Cycles			
Stop Mode Recovery	Unaffected, except WDT_CTL and OSC_CTL registers	Reset	66 Internal Precision Oscillator Cycles + IPO startup time			
Stop Mode Recovery with Crystal Oscillator Enabled	Unaffected, except WDT_CTL and OSC_CTL registers	Reset	5000 Internal Precision Oscillator Cycles			

During a System Reset or Stop Mode Recovery, the Internal Precision Oscillator requires 4 µs to start up. Then the Z8 Encore! XP F082A Series device is held in Reset for 66 cycles of the Internal Precision Oscillator. If the crystal oscillator is enabled in the Flash option bits, this reset period is increased to 5000 IPO cycles. When a reset occurs because of a low voltage condition or Power-On Reset (POR), this delay is measured from the time that the supply voltage first exceeds the POR level. If the external pin reset remains asserted at the end of the reset period, the device remains in reset until the pin is deas-serted.

At the beginning of Reset, all GPIO pins are configured as inputs with pull-up resistor disabled, except PD0 (or PA2 on 8-pin devices) which is shared with the reset pin. On reset, the PD0 is configured as a bidirectional open-drain reset. The pin is internally driven low during port reset, after which the user code may reconfigure this pin as a general purpose output.

During Reset, the eZ8 CPU and on-chip peripherals are idle; however, the on-chip crystal oscillator and Watchdog Timer oscillator continue to run.

Upon Reset, control registers within the Register File that have a defined Reset value are loaded with their reset values. Other control registers (including the Stack Pointer, Register Pointer and Flags) and general-purpose RAM are undefined following Reset. The eZ8 CPU fetches the Reset vector at Program Memory addresses 0002H and 0003H and loads that value into the Program Counter. Program execution begins at the Reset vector address.

As the control registers are reinitialized by a system reset, the system clock after reset is always the IPO. The software must reconfigure the oscillator control block, such that the correct system clock source is enabled and selected.

Reset Sources

Table 9 lists the possible sources of a system reset.

Table 9. Reset Sources and Resulting Reset Type

Operating Mode	Reset Source	Special Conditions		
NORMAL or HALT modes	Power-On Reset/Voltage Brown-Out	Reset delay begins after supply voltage exceeds POR level.		
	Watchdog Timer time-out when configured for Reset	None.		
	RESET pin assertion	All reset pulses less than three system clocks in width are ignored.		
	On-Chip Debugger initiated Reset (OCDCTL[0] set to 1)	System Reset, except the On-Chip Debugge is unaffected by the reset.		
STOP Mode	Power-On Reset/Voltage Brown-Out	Reset delay begins after supply voltage exceeds POR level.		
	RESET pin assertion	All reset pulses less than the specified analog delay are ignored. See Table 131 on page 229.		
_	DBG pin driven Low	None.		

Power-On Reset

Z8 Encore! XP F082A Series devices contain an internal Power-On Reset circuit. The POR circuit monitors the supply voltage and holds the device in the Reset state until the supply voltage reaches a safe operating level. After the supply voltage exceeds the POR voltage threshold (V_{POR}) , the device is held in the Reset state until the POR Counter has timed out. If the crystal oscillator is enabled by the option bits, this time-out is longer.

After the Z8 Encore! XP F082A Series device exits the Power-On Reset state, the eZ8 CPU fetches the Reset vector. Following Power-On Reset, the POR status bit in the Reset Status (RSTSTAT) Register is set to 1.

Figure 5 displays Power-On Reset operation. See Electrical Characteristics on page 221 for the POR threshold voltage (V_{POR}).

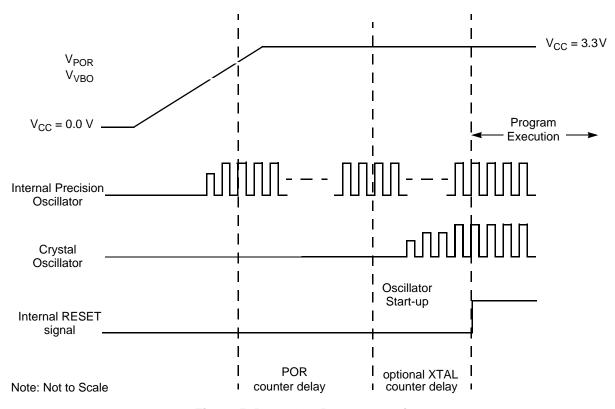


Figure 5. Power-On Reset Operation

Voltage Brown-Out Reset

The devices in the Z8 Encore! XP F082A Series provide low Voltage Brown-Out (VBO) protection. The VBO circuit senses when the supply voltage drops to an unsafe level (below the VBO threshold voltage) and forces the device into the Reset state. While the supply voltage remains below the Power-On Reset voltage threshold (V_{POR}), the VBO block holds the device in the Reset.

After the supply voltage again exceeds the Power-On Reset voltage threshold, the device progresses through a full System Reset sequence, as described in the Power-On Reset section. Following Power-On Reset, the POR status bit in the Reset Status (RSTSTAT) Register is set to 1. Figure 6 displays Voltage Brown-Out operation. See the <u>Electrical Characteristics</u> chapter on page 226 for the VBO and POR threshold voltages (V_{VBO} and V_{POR}).

The Voltage Brown-Out circuit can be either enabled or disabled during STOP Mode. Operation during STOP Mode is set by the VBO_AO Flash option bit. See the <u>Flash Option Bits</u> chapter on page 159 for information about configuring VBO_AO.

without initiating an interrupt (if enabled for that pin).

Stop Mode Recovery Using the External RESET Pin

When the Z8 Encore! XP F082A Series device is in STOP Mode and the external RESET pin is driven Low, a system reset occurs. Because of a glitch filter operating on the RESET pin, the Low pulse must be greater than the minimum width specified, or it is ignored. See the Electrical Characteristics chapter on page 226 for details.

Low Voltage Detection

In addition to the Voltage Brown-Out (VBO) Reset described above, it is also possible to generate an interrupt when the supply voltage drops below a user-selected value. For details about configuring the Low Voltage Detection (LVD) and the threshold levels available, see the <u>Trim Option Bits at Address 0003H (TLVD) Register</u> on page 166. The LVD function is available on the 8-pin product versions only.

When the supply voltage drops below the LVD threshold, the LVD bit of the Reset Status (RSTSTAT) Register is set to one. This bit remains one until the low-voltage condition goes away. Reading or writing this bit does not clear it. The LVD circuit can also generate an interrupt when so enabled, see the GPIO Mode Interrupt Controller chapter on page 55. The LVD bit is not latched; therefore, enabling the interrupt is the only way to guarantee detection of a transient low voltage event.

The LVD functionality depends on circuitry shared with the VBO block; therefore, disabling the VBO also disables the LVD.

Reset Register Definitions

The following sections define the Reset registers.

Reset Status Register

The read-only Reset Status (RSTSTAT) Register, shown in Table 11, indicates the source of the most recent Reset event, indicates a Stop Mode Recovery event and indicates a Watchdog Timer time-out. Reading this register resets the upper four bits to 0. This register shares its address with the write-only Watchdog Timer Control Register.

Table 12 lists the bit settings for Reset and Stop Mode Recovery events.

HALT Mode

Executing the eZ8 CPU's HALT instruction places the device into HALT Mode, which powers down the CPU but leaves all other peripherals active. In HALT Mode, the operating characteristics are:

- Primary oscillator is enabled and continues to operate
- System clock is enabled and continues to operate
- eZ8 CPU is stopped
- Program counter (PC) stops incrementing
- Watchdog Timer's internal RC oscillator continues to operate
- If enabled, the Watchdog Timer continues to operate
- All other on-chip peripherals continue to operate, if enabled

The eZ8 CPU can be brought out of HALT Mode by any of the following operations:

- Interrupt
- Watchdog Timer time-out (interrupt or reset)
- Power-On Reset
- Voltage Brown-Out reset
- External RESET pin assertion

To minimize current in HALT Mode, all GPIO pins that are configured as inputs must be driven to one of the supply rails (V_{CC} or GND).

Peripheral-Level Power Control

In addition to the STOP and HALT modes, it is possible to disable each peripheral on each of the Z8 Encore! XP F082A Series devices. Disabling a given peripheral minimizes its power consumption.

Power Control Register Definitions

The following sections define the Power Control registers.

Power Control Register 0

Each bit of the following registers disables a peripheral block, either by gating its system clock input or by removing power from the block. The default state of the low-power

Port A-C Input Data Registers

Reading from the Port A–C Input Data registers, shown in Table 29, return the sampled values from the corresponding port pins. The Port A–C Input Data registers are read-only. The value returned for any unused ports is 0. Unused ports include those missing on the 8-and 28-pin packages, as well as those missing on the ADC-enabled 28-pin packages.

Table 29. Port A-C Input Data Registers (PxIN)

Bit	7	6	5	4	3	2	1	0
Field	PIN7	PIN6	PIN5	PIN4	PIN3	PIN2	PIN1	PIN0
RESET	Х	Х	Х	Х	Х	Х	Х	Х
R/W	R	R	R	R	R	R	R	R
Address	FD2H, FD6H, FDAH							
X = Undefined.								

Bit	Description
[7:0]	Port Input Data
PxIN	Sampled data from the corresponding port pin input.
	0 = Input data is logical 0 (Low).
	1 = Input data is logical 1 (High).
Note:	x indicates the specific GPIO port pin number (7–0)

Port A–D Output Data Register

The Port A–D Output Data Register, shown in Table 30, controls the output data to the pins.

Table 30. Port A–D Output Data Register (PxOUT)

Bit	7	6	5	4	3	2	1	0
Field	POUT7	POUT6	POUT5	POUT4	POUT3	POUT2	POUT1	POUT0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FD3H, FD7H, FDBH, FDFH							

Bit	Description
[7:0] PxOUT	Port Output Data These bits contain the data to be driven to the port pins. The values are only driven if the corresponding pin is configured as an output and the pin is not configured for alternate function operation. 0 = Drive a logical 0 (Low). 1 = Drive a logical 1 (High). High value is not driven if the drain has been disabled by setting the corresponding Port Output Control Register bit to 1.

Note: x indicates the specific GPIO port pin number (7–0).

Table 46. IRQ2 Enable Low Bit Register (IRQ2ENL)

Bit	7	6	5	4	3	2	1	0
Field	Reserved			C3ENL	C2ENL	C1ENL	C0ENL	
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address		FC8H						

Bit	Description
[7:4]	Reserved
	These bits are reserved and must be programmed to 0000.
[3] C3ENL	Port C3 Interrupt Request Enable Low Bit
[2] C2ENL	Port C2 Interrupt Request Enable Low Bit
[1] C1ENL	Port C1 Interrupt Request Enable Low Bit
[0] C0ENL	Port C0 Interrupt Request Enable Low Bit

Interrupt Edge Select Register

The Interrupt Edge Select (IRQES) Register, shown in Table 47, determines whether an interrupt is generated for the rising edge or falling edge on the selected GPIO Port A input pin.

Table 47. Interrupt Edge Select Register (IRQES)

Bit	7	6	5	4	3	2	1	0
Field	IES7	IES6	IES5	IES4	IES3	IES2	IES1	IES0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address		FCDH						

Bit	Description
[7:0]	Interrupt Edge Select x
IES x	0 = An interrupt request is generated on the falling edge of the PAx input.
	1 = An interrupt request is generated on the rising edge of the PAx input.
Note:	x indicates the specific GPIO port pin number (0–7).

- Set or clear CTSE to enable or disable control from the remote receiver using the CTS pin
- 8. Execute an EI instruction to enable interrupts.

The UART is now configured for interrupt-driven data transmission. Because the UART Transmit Data Register is empty, an interrupt is generated immediately. When the UART Transmit interrupt is detected, the associated interrupt service routine (ISR) performs the following:

- 1. Write the UART Control 1 Register to select the multiprocessor bit for the byte to be transmitted:
- 2. Set the Multiprocessor Bit Transmitter (MPBT) if sending an address byte, clear it if sending a data byte.
- 3. Write the data byte to the UART Transmit Data Register. The transmitter automatically transfers the data to the Transmit Shift Register and transmits the data.
- 4. Clear the UART Transmit interrupt bit in the applicable Interrupt Request Register.
- 5. Execute the IRET instruction to return from the interrupt-service routine and wait for the Transmit Data Register to again become empty.

Receiving Data using the Polled Method

Observe the following steps to configure the UART for polled data reception:

- 1. Write to the UART Baud Rate High and Low Byte registers to set an acceptable baud rate for the incoming data stream.
- 2. Enable the UART pin functions by configuring the associated GPIO port pins for alternate function operation.
- 3. Write to the UART Control 1 Register to enable MULTIPROCESSOR Mode functions, if appropriate.
- 4. Write to the UART Control 0 Register to:
 - Set the receive enable bit (REN) to enable the UART for data reception
 - Enable parity, if appropriate and if Multiprocessor mode is not enabled and select either even or odd parity.
- 5. Check the RDA bit in the UART Status 0 Register to determine if the Receive Data Register contains a valid data byte (indicated by a 1). If RDA is set to 1 to indicate available data, continue to Step 5. If the Receive Data Register is empty (indicated by a 0), continue to monitor the RDA bit awaiting reception of the valid data.

Analog-to-Digital Converter

The analog-to-digital converter (ADC) converts an analog input signal to its digital representation. The features of this sigma-delta ADC include:

- 11-bit resolution in DIFFERENTIAL Mode
- 10-bit resolution in SINGLE-ENDED Mode
- Eight single-ended analog input sources are multiplexed with general-purpose I/O ports
- 9th analog input obtained from temperature sensor peripheral
- 11 pairs of differential inputs also multiplexed with general-purpose I/O ports
- Low-power operational amplifier (LPO)
- Interrupt on conversion complete
- Bandgap generated internal voltage reference with two selectable levels
- Manual in-circuit calibration is possible employing user code (offset calibration)
- Factory calibrated for in-circuit error compensation

Architecture

Figure 19 displays the major functional blocks of the ADC. An analog multiplexer network selects the ADC input from the available analog pins, ANA0 through ANA7.

The input stage of the ADC allows both differential gain and buffering. The following input options are available:

- Unbuffered input (SINGLE-ENDED and DIFFERENTIAL modes)
- Buffered input with unity gain (SINGLE-ENDED and DIFFERENTIAL modes)
- LPO output with full pin access to the feedback path

Bit	Description (Continued)
[1:0]	For 8-pin devices, the following voltages can be configured; for 20- and 28-pin devices, these
	bits are reserved.
	000000 = 0.00 V
	000001 = 0.05 V
	000010 = 0.10 V
	000011 = 0.15 V
	000100 = 0.20 V
	000101 = 0.25 V
	000110 = 0.30 V
	000111 = 0.35 V
	001000 = 0.40 V
	001001 = 0.45 V
	001010 = 0.50 V
	001011 = 0.55 V
	001100 = 0.60 V
	001101 = 0.65 V
	001110 = 0.70 V
	001111 = 0.75 V
	010000 = 0.80 V
	010001 = 0.85 V
	010010 = 0.90 V
	010011 = 0.95 V
	010100 = 1.00 V (Default)
	010101 = 1.05 V
	010110 = 1.10 V 010111 = 1.15 V
	011000 = 1.20 V
	011000 = 1.20 V 011001 = 1.25 V
	011010 = 1.23 V 011010 = 1.30 V
	011011 = 1.35 V
	011100 = 1.40 V
	011101 = 1.45 V
	011110 = 1.50 V
	011111 = 1.55 V
	100000 = 1.60 V
	100001 = 1.65 V
	100010 = 1.70 V
	100011 = 1.75 V
	100100 = 1.80 V

Z8 Encore! XP[®] F082A Series Product Specification

154

Debugger. Writing an invalid value or an invalid sequence returns the Flash Controller to its locked state. The Write-only Flash Control Register shares its Register File address with the read-only Flash Status Register.

Temperature Sensor Calibration Data

Table 98. Temperature Sensor Calibration High Byte at 003A (TSCALH)

Bit	7	6	5	4	3	2	1	0
Field				TSC	ALH			
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address			Info	rmation Pag	e Memory 0	03A		
Note: U =	Unchanged b	y Reset. R/W	/ = Read/Writ	e.				

Bit Description

[7:0] Temperature Sensor Calibration High Byte
TSCALH The TSCALH and TSCALL bytes combine to form the 12-bit temperature sensor offset calibration value. For more details, see Temperature Sensor Operation on page 139.

Table 99. Temperature Sensor Calibration Low Byte at 003B (TSCALL)

Bit	7	6	5	4	3	2	1	0
Field				TSC	ALL			
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address			Info	rmation Pag	e Memory 0	03B		
Note: U =	Unchanged b	y Reset. R/W	/ = Read/Writ	e.				

Bit	Description
[7:0]	Temperature Sensor Calibration Low Byte
TSCALL	The TSCALH and TSCALL bytes combine to form the 12-bit temperature sensor offset calibra-
	tion value. For usage details, see the <u>Temperature Sensor Operation</u> section on page 144.

eZ8 CPU Instruction Set

This chapter describes the following features of the eZ8 CPU instruction set:

Assembly Language Programming Introduction: see page 204

Assembly Language Syntax: see page 205
eZ8 CPU Instruction Notation: see page 206
eZ8 CPU Instruction Classes: see page 207
eZ8 CPU Instruction Summary: see page 212

Assembly Language Programming Introduction

The eZ8 CPU assembly language provides a means for writing an application program without concern for actual memory addresses or machine instruction formats. A program written in assembly language is called a source program. Assembly language allows the use of symbolic addresses to identify memory locations. It also allows mnemonic codes (opcodes and operands) to represent the instructions themselves. The opcodes identify the instruction while the operands represent memory locations, registers, or immediate data values.

Each assembly language program consists of a series of symbolic commands called statements. Each statement can contain labels, operations, operands and comments.

Labels can be assigned to a particular instruction step in a source program. The label identifies that step in the program as an entry point for use by other instructions.

The assembly language also includes assembler directives that supplement the machine instruction. The assembler directives, or pseudo-ops, are not translated into a machine instruction. Rather, the pseudo-ops are interpreted as directives that control or assist the assembly process.

The source program is processed (assembled) by the assembler to obtain a machine language program called the object code. The object code is executed by the eZ8 CPU. An example segment of an assembly language program is detailed in the following example.

Table 126. Program Control Instructions

Mnemonic	Operands	Instruction
BRK	_	On-Chip Debugger Break
BTJ	p, bit, src, DA	Bit Test and Jump
BTJNZ	bit, src, DA	Bit Test and Jump if Non-Zero
BTJZ	bit, src, DA	Bit Test and Jump if Zero
CALL	dst	Call Procedure
DJNZ	dst, src, RA	Decrement and Jump Non-Zero
IRET	_	Interrupt Return
JP	dst	Jump
JP cc	dst	Jump Conditional
JR	DA	Jump Relative
JR cc	DA	Jump Relative Conditional
RET	_	Return
TRAP	vector	Software Trap

Table 127. Rotate and Shift Instructions

Mnemonic	Operands	Instruction
BSWAP	dst	Bit Swap
RL	dst	Rotate Left
RLC	dst	Rotate Left through Carry
RR	dst	Rotate Right
RRC	dst	Rotate Right through Carry
SRA	dst	Shift Right Arithmetic
SRL	dst	Shift Right Logical
SWAP	dst	Swap Nibbles

Table 128. eZ8 CPU Instruction Summary (Continued)

Assembly			ress de	_ Opcode(s)			Fla	ags			Fetch Cycle	Instr. Cycle
Mnemonic	Symbolic Operation	dst	src	(Hex)		Z	S	٧	D	Н	S	S
CALL dst	SP ← SP -2	IRR		D4	-	-	-	-	-	-	2	6
	@SP ← PC PC ← dst	DA		D6							3	3
CCF	C ← ~C			EF	*	-	-	-	-		1	2
CLR dst	dst ← 00H	R		В0	-	-	-	-	-	_	2	2
		IR		B1							2	3
COM dst	dst ← ~dst	R		60	_	*	*	0	-	_	2	2
		IR		61							2	3
CP dst, src	dst - src	r	r	A2	*	*	*	*	_	_	2	3
		r	lr	А3	-						2	4
		R	R	A4	-						3	3
		R	IR	A5							3	4
		R	IM	A6	-						3	3
		IR	IM	A7							3	4
CPC dst, src	dst - src - C	r	r	1F A2	*	*	*	*	_	_	3	3
		r	lr	1F A3	-						3	4
		R	R	1F A4	="						4	3
		R	IR	1F A5	-						4	4
		R	IM	1F A6	-						4	3
		IR	IM	1F A7	-						4	4
CPCX dst, src	dst - src - C	ER	ER	1F A8	*	*	*	*	-	_	5	3
		ER	IM	1F A9	-						5	3
CPX dst, src	dst - src	ER	ER	A8	*	*	*	*	-	_	4	3
		ER	IM	A9	-						4	3

Note: Flags Notation:

^{* =} Value is a function of the result of the operation.

⁻ = Unaffected.

X = Undefined.

^{0 =} Reset to 0.

^{1 =} Set to 1.

Table 148. Z8 Encore! XP F082A Series Ordering Matrix

		70. <u>2</u> 0 i			UU _,			J. 4.0.			
Part Number	Flash	RAM	NVDS	VO Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description
Z8 Encore! XP F082	A Series	with 8 k	(B Flas	sh							
Standard Temperatu	re: 0°C t	to 70°C									
Z8F081APB020SG	8KB	1KB	0	6	13	2	0	1	1	0	PDIP 8-pin package
Z8F081AQB020SG	8KB	1KB	0	6	13	2	0	1	1	0	QFN 8-pin package
Z8F081ASB020SG	8KB	1KB	0	6	13	2	0	1	1	0	SOIC 8-pin package
Z8F081ASH020SG	8KB	1KB	0	17	19	2	0	1	1	0	SOIC 20-pin package
Z8F081AHH020SG	8KB	1KB	0	17	19	2	0	1	1	0	SSOP 20-pin package
Z8F081APH020SG	8KB	1KB	0	17	19	2	0	1	1	0	PDIP 20-pin package
Z8F081ASJ020SG	8KB	1KB	0	25	19	2	0	1	1	0	SOIC 28-pin package
Z8F081AHJ020SG	8KB	1KB	0	25	19	2	0	1	1	0	SSOP 28-pin package
Z8F081APJ020SG	8KB	1KB	0	25	19	2	0	1	1	0	PDIP 28-pin package
Extended Temperatu	ıre: –40°	C to 10	5°C								
Z8F081APB020EG	8KB	1KB	0	6	13	2	0	1	1	0	PDIP 8-pin package
Z8F081AQB020EG	8KB	1KB	0	6	13	2	0	1	1	0	QFN 8-pin package
Z8F081ASB020EG	8KB	1KB	0	6	13	2	0	1	1	0	SOIC 8-pin package
Z8F081ASH020EG	8KB	1KB	0	17	19	2	0	1	1	0	SOIC 20-pin package
Z8F081AHH020EG	8KB	1KB	0	17	19	2	0	1	1	0	SSOP 20-pin package
Z8F081APH020EG	8KB	1KB	0	17	19	2	0	1	1	0	PDIP 20-pin package
Z8F081ASJ020EG	8KB	1KB	0	25	19	2	0	1	1	0	SOIC 28-pin package
Z8F081AHJ020EG	8KB	1KB	0	25	19	2	0	1	1	0	SSOP 28-pin package
Z8F081APJ020EG	8KB	1KB	0	25	19	2	0	1	1	0	PDIP 28-pin package

G	indirect register pair 206
	indirect register pair 200 indirect working register 206
GATED mode 88	indirect working register 200
general-purpose I/O 36	infrared encoder/decoder (IrDA) 120
GPIO 6, 36	Instruction Set 204
alternate functions 37	
architecture 37	instruction set, eZ8 CPU 204 instructions
control register definitions 44	ADC 208
input data sample timing 240	
interrupts 44	ADCX 208
port A-C pull-up enable sub-registers 50, 51	ADD 208
port A-H address registers 45	ADDX 208
port A-H alternate function sub-registers 47	AND 210
port A-H control registers 46	ANDX 210
port A-H data direction sub-registers 46	arithmetic 208
port A-H high drive enable sub-registers 48	BCLR 209
port A-H input data registers 52	BIT 209
port A-H output control sub-registers 47	bit manipulation 209
port A-H output data registers 52, 53	block transfer 209
port A-H stop mode recovery sub-registers 49	BRK 211
port availability by device 36	BSET 209
port input timing 240	BSWAP 209, 211
port output timing 241	BTJ 211
	BTJNZ 211
	BTJZ 211
Н	CALL 211
H 207	CCF 209
HALT 209	CLR 210
halt mode 33, 209	COM 210
hexadecimal number prefix/suffix 207	CP 208
F	CPC 208
	CPCX 208
I	CPU control 209
I2C 6	CPX 208
IM 206	DA 208
immediate data 206	DEC 208
immediate operand prefix 207	DECW 208
INC 208	DI 209
increment 208	DJNZ 211
increment word 208	EI 209
	HALT 209
INCW 208	INC 208
indexed 207	INCW 208
indirect address prefix 207	IRET 211
indirect register 206	JP 211

UARTx control I (UxCTL1) 112 UARTx receive data (UxRXD) 116 UARTx status 0 (UxSTAT0) 114 SP 207 UARTx status 1 (UxSTAT1) 115 UARTx transmit data (UxTXD) 116 Watchdog Timer control (WDTCTL) 30, 96, 141, 196 Watchdog Timer reload high byte (WDTH) 97 Watchdog Timer reload low byte (WDTU) 97 Watchdog Timer reload upper byte (WDTU) 97 Watchdog Timer reload 22 stop mode 210 Stop Mode Recovery 22 sources 27 using a GPIO port pin transition 28 using Watchdog Timer time-out 28 stop mode recovery sources 29 using a GPIO port pin transition 29 SUB 208 subtract with carry 208 subtract with carry 208 subtract with carry 208 subtract with carry - extended addressing 208 SUBX 208 SWAP 211 swap nibbles 211 symbols, additional 207 TCM 209 TCMX 209 test complement under mask 209 test complement under mask - extended addressing 209 test under mask 209
UARTx status 1 (UxSTAT1) 115 UARTx transmit data (UXTXD) 116 Watchdog Timer control (WDTCTL) 30, 96, 141, 196 Watchdog Timer reload high byte (WDTH) 97 Watchdog Timer reload low byte (WDTL) 98 Watchdog Timer reload upper byte (WDTU) 98 Watchdog Timer reload upper byte (WDTU) 97 Watchdog Timer reload upper byte (WDTU) 98 Watchdog Timer reload upper byte (WDTU) 97 register file 15 register pair 206 register pointer 207 resest and stop mode characteristics 23 and Stop Mode Recovery 22 carry flag 209 sources 24 RET 211 return 211 RLC 211 rotate and shift instuctions 211 rotate left 211 rotate left 211 rotate left through carry 211 rotate right through carry 211 RR 207 RR 206, 211 TT 206 RRC 211 SRA 211 src 207 SRL 211 SRP 207 SRD 210 STOP mode 32 stop mode 210 Stop Mode Recovery sources 27 using a GPIO port pin transition 28 using a GPIO port pin transition 29 subtract 208 subtract 208 subtract 208 subtract with carry 208 subtract with carry 208 SWAP 211 swap nibbles 211 symbols, additional 207 TT TCMX 209 test complement under mask 209 test under mask 209 test under mask 209 test under mask 209
UARTx transmit data (UxTXD) 116 Watchdog Timer control (WDTCTL) 30, 96, 141, 196 Watchdog Timer reload high byte (WDTH) 97 Watchdog Timer reload low byte (WDTU) 97 Watchdog Timer reload upper byte (WDTU) 97 register file 15 register pair 206 register pointer 207 reset and stop mode characteristics 23 and Stop Mode Recovery 22 carry flag 209 sources 24 RET 211 return 211 RLC 211 RLC 211 RLC 211 RLC 211 rotate left through carry 211 rotate right through carry 211 rr 206 RRC 211 SBC 208 SBC 208 SRC 211 SRP 210 STOP mode 32 stop mode 210 Stop Mode Recovery sources 27 using a GPIO port pin transition 28 using a GPIO port pin transition 29 SUB 208 subtract 208 subtract 208 subtract 208 subtract with carry 208 subtract with carry - extended addressing 208 SWAP 211 swap nibbles 211 symbols, additional 207 T T T TCM 209 TCMX 209 test complement under mask 209 test under mask 209 TCMS 209 test under mask 209
Watchdog Timer control (WDTCTL) 30, 96, 141, 196 Watchdog Timer reload high byte (WDTH) 97 Watchdog Timer reload upper byte (WDTU) 97 register file 15 register pair 206 register pointer 207 reset and stop mode characteristics 23 and Stop Mode Recovery 22 carry flag 209 sources 24 RET 211 return 211 RL 21
141, 196 Watchdog Timer reload high byte (WDTH) 97 Watchdog Timer reload low byte (WDTL) 98 Watchdog Timer reload upper byte (WDTU) 97 register file 15 register pair 206 register pointer 207 reset and stop mode characteristics 23 and Stop Mode Recovery 22 carry flag 209 sources 24 REF 211 return 211 RL 211 RLC 211 rotate left 211 rotate left through carry 211 rotate left through carry 211 rotate right 11 RP 207 RR 206, 211 RF 206 RRC 211 SBC 208 SBC 208 SRP 210 stack pointer 207 stack pointer 207 stack pointer 207 STOP mode 32 stop mode 210 Stop Mode Recovery sources 27 using a GPIO port pin transition 28 using a GPIO port pin transition 29 SUB 208 subtract 208 subtract 208 subtract with carry 208 subtract with carry 208 subtract with carry - extended addressing 208 rotate and shift instuctions 211 swap nibbles 211 symbols, additional 207 TCM 209 TCMX 209 test complement under mask 209 test complement under mask - extended addressing 209 test under mask 209
Watchdog Timer reload high byte (WDTH) 97 Watchdog Timer reload low byte (WDTL) 98 Watchdog Timer reload low byte (WDTU) 97 register file 15 register pair 206 register pointer 207 reset and stop mode characteristics 23 and Stop Mode Recovery 22 carry flag 209 sources 24 RET 211 return 211 RL C 211 rotate left 211 rotate left through carry 211 rotate right 211 r
Watchdog Timer reload low byte (WDTL) 98 Watchdog Timer reload upper byte (WDTU) 97 1
Watchdog Timer reload upper byte (WDTU) 97 register file 15 register pair 206 register pointer 207 reset and stop mode characteristics 23 and Stop Mode Recovery 22 carry flag 209 sources 24 RET 211 return 211 RL 211 RL C 211 RL C 211 rotate end shift instuctions 211 rotate right 121 rotate right 121 rotate right through carry 211 RP 207 RR 206, 211 rT 206 RRC 211 STOP mode 32 stop mode 210 Stop Mode Recovery sources 27 using a GPIO port pin transition 28 using a GPIO port pin transition 29 SUB 208 subtract 208 subtract 208 subtract vith carry 208 subtract with carry 208 subtract with carry 208 SUBX 208 SWAP 211 swap nibbles 211 symbols, additional 207 TCM 209 TCMX 209 test complement under mask 209 test complement under mask 209 test complement under mask - extended addressing 209 sets tunder mask 209 test under mask 209
stop mode 210 Stop Mode Recovery sources 27 using a GPIO port pin transition 28 using Watchdog Timer time-out 28 stop mode recovery sources 27 using a GPIO port pin transition 28 using Watchdog Timer time-out 28 stop mode recovery sources 29 using a GPIO port pin transition 29 sources 24 SUB 208 RET 211 subtract 208 RET 211 subtract 208 REL 211 RL 211 RL 211 SUB 208 SU
register file 15 register pair 206 register pointer 207 reset and stop mode characteristics 23 and Stop Mode Recovery 22 carry flag 209 sources 24 RET 211 return 211 RL 208 SUBX 208 SUBX 208 SUBX 208 SUBX 208 TOtate left through carry 211 rotate left through carry 211 rotate right 211 rotate right through carry 211 rotate right through carry 211 RP 207 RR 206, 211 TCMX 209 test complement under mask 209 test complement under mask - extended addressing 209 RS C 208 SBC 208 L C 208
register pair 206 register pointer 207 reset and stop mode characteristics 23 and Stop Mode Recovery 22 carry flag 209 sources 24 RET 211 return 211 RL 211 RL C 211 RL C 211 rotate left through carry 211 rotate right 211 rotate right 211 rotate right through carry 211 rotate right through carry 211 rr 206 RRC 211 RRC 211 RRC 211 RRC 211 RRC 211 RRC 206 RRC 211 RRC 208 Sources 29 using a GPIO port pin transition 29 Sources 29 using a GPIO port pin transition 29 Sources 29 using a GPIO port pin transition 29 Sources 29 using a GPIO port pin transition 29 Sources 29 using a GPIO port pin transition 29 SUB 208 subtract 208 subtract 208 subtract 208 subtract 208 subtract with carry 208 subtract with carry 208 subtract with carry - extended addressing 208 SUBX 208 SWAP 211 swap nibbles 211 symbols, additional 207 T T T TCMX 209 test complement under mask 209 test complement under mask - extended addressing 209 test under mask 209 test under mask 209
register pointer 207 reset and stop mode characteristics 23 and Stop Mode Recovery 22 carry flag 209 sources 24 RET 211 subtract 208 return 211 RL 211 RLC 211 RLC 211 subtract with carry 208 rotate and shift instuctions 211 rotate left through carry 211 rotate right 211 rotate right 211 rotate right through carry 211 RRP 207 RR RR 206, 211 rr 206 RRC 211 SBC 208 using a GPIO port pin transition 28 stop mode recovery sources 29 using a GPIO port pin transition 29 SUB 208 subtract 208 subtract 208 subtract 208 subtract with carry 208 subtract with carry 208 subtract with carry - extended addressing 208 SWAP 211 swap nibbles 211 symbols, additional 207 T T T T TCMX 209 test complement under mask 209 test complement under mask - extended addressing 209 test under mask 209 test under mask 209
reset using Watchdog Timer time-out 28 stop mode characteristics 23 and Stop Mode Recovery 22 carry flag 209 sources 24 RET 211 return 211 RL 211 RL 211 RL 211 Subtract 208 subtract vith carry 208 soutcate left 211 rotate left through carry 211 rotate right through carry 211 RP 207 RR 206, 211 RR 206 RRC 211 SBC 208 stop mode recovery sources 29 using a GPIO port pin transition 29 SUB 208 subtract 208 subtract 208 subtract vith carry 208 subtract with carry 208 SWAP 211 swap nibbles 211 symbols, additional 207 T T T TCMX 209 test complement under mask 209 test complement under mask - extended addressing 209 test under mask 209 test under mask 209 test under mask 209 test under mask 209
and stop mode characteristics 23 and Stop Mode Recovery 22 carry flag 209 sources 24 RET 211 return 211 RL
and Stop Mode Recovery 22 carry flag 209 sources 24 RET 211 return 211 RL 211 RLC 211 RLC 211 rotate left through carry 211 rotate right 211 rotate right through carry 211 RP 207 RR 206, 211 RR 206 RRC 211 SBC 208 sources 29 using a GPIO port pin transition 29 SUB 208 subtract 208 subtract 208 subtract - extended addressing 208 subtract with carry 208 subtract with carry - extended addressing 208 SUBX 208 SWAP 211 swap nibbles 211 symbols, additional 207 T T T T T T T T T T T T T T T T T T
using a GPIO port pin transition 29 sources 24 RET 211 subtract 208 RET 211 subtract 208 RL 211 RL 211 subtract - extended addressing 208 REL 211 subtract with carry 208 SUBX 208 S
sources 24 RET 211 return 211 RL 211 RL 211 RL 211 Subtract 208 subtract 208 subtract - extended addressing 208 subtract with carry 208 subtract with carry - extended addressing 208 rotate and shift instuctions 211 rotate left 211 SWAP 211 swap nibbles 211 rotate right 211 rotate right through carry 211 RP 207 RR 206, 211 rr 206 RRC 211 T TCM 209 RRC 211 TCMX 209 test complement under mask 209 test complement under mask - extended addressing 208 SBC 208 SUBX 208 SUBX 208 SUBX 208 SUBX 208 TOMA 209 test complement under mask 209 test complement under mask - extended addressing 209 test under mask 209 test under mask 209
subtract 208 return 211 return 21
subtract - extended addressing 208 RL 211 RLC 211 subtract with carry 208 subtract with carry 208 subtract with carry - extended addressing 208 rotate and shift instuctions 211 subtract with carry - extended addressing 208 SUBX
RL 211 RLC 211 subtract with carry 208 subtract with carry 208 subtract with carry - extended addressing 208 rotate and shift instuctions 211 rotate left 211 rotate left through carry 211 rotate right 211 rotate right through carry 211 RP 207 RR 206, 211 Tr 206 RRC 211 TCMX 209 test complement under mask 209 test under mask 209 SBC 208 subtract with carry 208 subtract with carry 208 subtract with carry 208 subtract with carry 208 subtract with carry 208 subtract with carry 208 subtract with carry 208 subtract with carry 208 subtract with carry 208 subtract with carry - extended addressing 208 subtract with carry - extended addressing 209 subtract with carry - extended addressing 208 subtract with carry - extended addressing 209 subtract with carry - extended addressing 209 subtract with carry - extended addressing 208
subtract with carry - extended addressing 208 rotate and shift instructions 211 rotate left 211 swap nibbles 211 rotate right 211 rotate right through carry 211 RP 207 RR 206, 211 rr 206 RRC 211 TCMX 209 test complement under mask 209 test complement under mask - extended addressing 208 SBC 208 Subx 208 SUBX 208 SU
rotate and shift instuctions 211 rotate left 211 rotate left through carry 211 rotate right 211 rotate right through carry 211 RP 207 RR 206, 211 rr 206 RRC 211 TCMX 209 test complement under mask 209 test complement under mask - extended addressing 209 SBC 208 SBC 208 TSUBX 208 SWAP 211 swap nibbles 211 symbols, additional 207 TCM 209 TCMX 209 test complement under mask 209 test complement under mask 209 test under mask 209
rotate left 211 rotate left through carry 211 rotate right 211 rotate right 211 rotate right through carry 211 RP 207 RR 206, 211 rr 206 RRC 211 TCMX 209 test complement under mask 209 test complement under mask - extended addressing 209 test under mask 209 test under mask 209
rotate left through carry 211 rotate right 211 rotate right through carry 211 RP 207 RR 206, 211 rr 206 RRC 211 TCMX 209 test complement under mask 209 test complement under mask - extended addressing 209 SBC 208 Section 11 Swap nibbles 211 symbols, additional 207 T T T T T T T T T T T T T T T T T T
rotate right 211 rotate right through carry 211 RP 207 RR 206, 211 Tr 206 RRC 211 TCMX 209 test complement under mask 209 test complement under mask - extended addressing 209 SBC 208 test under mask 209
rotate right through carry 211 RP 207 RR 206, 211 Tr 206 RRC 211 TCMX 209 test complement under mask 209 test complement under mask - extended addressing 209 SBC 208 test under mask 209
RP 207 RR 206, 211 Tr 206 RRC 211 TCM 209 TCMX 209 test complement under mask 209 test complement under mask - extended addressing 209 SBC 208 test under mask 209
TCM 209 RRC 211 TCMX 209 TCMX 209 test complement under mask 209 test complement under mask - extended addressing 209 SBC 208 test under mask 209
TCM 209 RRC 211 TCMX 209 test complement under mask 209 test complement under mask - extended addressing 209 SBC 208 test under mask 209
TCMX 209 test complement under mask 209 test complement under mask - extended addressing 209 SBC 208 test under mask 209
test complement under mask 209 test complement under mask - extended addressing 209 SBC 208 test under mask 209
test complement under mask - extended addressing 209 SBC 208 test under mask 209
SBC 208 209 test under mask 209
SBC 208 209 test under mask 209
000 000 010
SCF 209, 210 test under mask - extended addressing 209
second opcode map after 1FH 225 timer signals 10
set carry flag 209, 210 timers 70
set register pointer 210 architecture 70
shift right arithmatic 211 block diagram 71