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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, Temp Sensor, WDT
Number of I/O	6
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	16 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f012asb020sg
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Z8 Encore! XP[®] F082A Series Product Specification

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Symbol Mnemonic	Direction	Reset Direction	Active Low or Active High	Tristate Output	Internal Pull-up or Pull-down	Schmitt- Trigger Input	Open Drain Output	5 V Tolerance			
AVDD	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A			
AVSS	N/A	N/A	N/A	N/A	N/A	N/A	N/A	NA			
DBG	I/O	I	N/A	Yes	Yes	Yes	Yes	No			
PA[7:0]	I/O	I	N/A	Yes	Programma- ble Pull-up	Yes	Yes, Programma- ble	PA[7:2] unless pul- lups enabled			
PB[7:0]	I/O	I	N/A	Yes	Programma- ble Pull-up	Yes	Yes, Programma- ble	PB[7:6] unless pul- lups enabled			
PC[7:0]	I/O	I	N/A	Yes	Programma- ble Pull-up	Yes	Yes, Programma- ble	PC[7:3] unless pul- lups enabled			
RESET/ PD0	I/O	I/O (defaults to RESET)	Low (in Reset mode)	Yes (PD0 only)	Programma- ble for PD0; alw <u>ays on f</u> or RESET	Yes	Programma- ble for PD0; alw <u>ays on f</u> or RESET	Yes, unless pul- lups enabled			
VDD	N/A	N/A	N/A	N/A			N/A	N/A			
VSS	N/A	N/A	N/A	N/A			N/A	N/A			

Table 3. Pin Characteristics (20- and 28-pin Devices)



Note: PB6 and PB7 are available only in those devices without ADC.

Reset Sources

Table 9 lists the possible sources of a system reset.

	Table 9. Reset Source	ces and Resulting Reset Type
_		

Operating Mode	Reset Source	Special Conditions	
NORMAL or HALT modes	Power-On Reset/Voltage Brown- Out	Reset delay begins after supply voltage exceeds POR level.	
	Watchdog Timer time-out when configured for Reset	None.	
	RESET pin assertion	All reset pulses less than three system clocks in width are ignored.	
	On-Chip Debugger initiated Reset (OCDCTL[0] set to 1)	System Reset, except the On-Chip Debugge is unaffected by the reset.	
STOP Mode	Power-On Reset/Voltage Brown- Out	Reset delay begins after supply voltage exceeds POR level.	
	RESET pin assertion	All reset pulses less than the specified analog delay are ignored. See Table 131 on page 229.	
	DBG pin driven Low	None.	

Power-On Reset

Z8 Encore! XP F082A Series devices contain an internal Power-On Reset circuit. The POR circuit monitors the supply voltage and holds the device in the Reset state until the supply voltage reaches a safe operating level. After the supply voltage exceeds the POR voltage threshold (VPOR), the device is held in the Reset state until the POR Counter has timed out. If the crystal oscillator is enabled by the option bits, this time-out is longer.

After the Z8 Encore! XP F082A Series device exits the Power-On Reset state, the eZ8 CPU fetches the Reset vector. Following Power-On Reset, the POR status bit in the Reset Status (RSTSTAT) Register is set to 1.

Figure 5 displays Power-On Reset operation. See Electrical Characteristics on page 221 for the POR threshold voltage (V_{POR}).

Port	Pin	Mnemonic	Alternate Function Description	Alternate Function Set Register AFS1
Port B ³	PB0	Reserved		AFS1[0]: 0
-		ANA0/AMPOUT	ADC Analog Input/LPO Output	AFS1[0]: 1
	PB1	Reserved		AFS1[1]: 0
		ANA1/AMPINN	ADC Analog Input/LPO Input (N)	AFS1[1]: 1
	PB2	Reserved		AFS1[2]: 0
		ANA2/AMPINP	ADC Analog Input/LPO Input (P)	AFS1[2]: 1
	PB3	CLKIN	External Clock Input	AFS1[3]: 0
		ANA3	ADC Analog Input	AFS1[3]: 1
	PB4	Reserved		AFS1[4]: 0
		ANA7	ADC Analog Input	AFS1[4]: 1
	PB5	Reserved		AFS1[5]: 0
		V _{REF} ⁴	ADC Voltage Reference	AFS1[5]: 1
	PB6	Reserved		AFS1[6]: 0
		Reserved		AFS1[6]: 1
	PB7	Reserved		AFS1[7]: 0
		Reserved		AFS1[7]: 1

Table 15. Port Alternate Function Mapping (Non 8-Pin Parts) (Continued)

Notes:

- Because there is only a single alternate function for each Port A pin, the Alternate Function Set registers are not implemented for Port A. Enabling alternate function selections automatically enables the associated alternate function. See the <u>Port A–D Alternate Function Subregisters (PxAF)</u> section on page 47 for details.
- 2. Whether PA0/PA6 takes on the timer input or timer output complement function depends on the timer configuration. See the <u>Timer Pin Signal Operation</u> section on page 84 for details.
- Because there are at most two choices of alternate function for any pin of Port B, the Alternate Function Set Register AFS2 is not used to select the function. Alternate function selection must also be enabled. See the <u>Port</u> <u>A–D Alternate Function Subregisters (PxAF)</u> section on page 47 for details.
- 4. V_{RFF} is available on PB5 in 28-pin products and on PC2 in 20-pin parts.
- Because there are at most two choices of alternate function for any pin of Port C, the Alternate Function Set Register AFS2 is not used to select the function. Alternate function selection must also be enabled. See the <u>Port</u> <u>A–D Alternate Function Subregisters (PxAF)</u> section on page 47 for details.
- Because there is only a single alternate function for the Port PD0 pin, the Alternate Function Set registers are not implemented for Port D. Enabling alternate function selections automatically enables the associated alternate function. See the <u>Port A–D Alternate Function Subregisters (PxAF)</u> section on page 47 for details.

Port A–D Address Registers

The Port A–D Address registers select the GPIO port functionality accessible through the Port A–D Control registers. The Port A–D Address and Control registers combine to provide access to all GPIO port controls; see Tables 18 and 19.

Bit	7	6	5	4	3	2	1	0
Field	PADDR[7:0]							
RESET	00H							
R/W	R/W	R/W R/W R/W R/W R/W R/W R/W						
Address	FD0H, FD4H, FD8H, FDCH							

Table 18. Port A–D GPIO Address Registers (PxADDR)

Bit	Description
[7:0]	Port Address
PADDRx	The Port Address selects one of the subregisters accessible through the Port Control Register.
Note: x inc	dicates the specific GPIO port pin number (7–0).

Table 19. Port A–D GPIO Address Registers by Bit Description

PADDR[7:0]	Port Control Subregister accessible using the Port A–D Control Registers
00H	No function. Provides some protection against accidental port reconfiguration.
01H	Data Direction.
02H	Alternate Function.
03H	Output Control (Open-Drain).
04H	High Drive Enable.
05H	Stop Mode Recovery Source Enable.
06H	Pull-up Enable.
07H	Alternate Function Set 1.
08H	Alternate Function Set 2.
09H–FFH	No function.

- Set the prescale value
- If using the Timer Output alternate function, set the initial output level (High or Low)
- 2. Write to the Timer High and Low Byte registers to set the starting count value (usually 0001H). This action only affects the first pass in CONTINUOUS Mode. After the first timer Reload in CONTINUOUS Mode, counting always begins at the reset value of 0001H.
- 3. Write to the Timer Reload High and Low Byte registers to set the reload value.
- 4. Enable the timer interrupt (if appropriate) and set the timer interrupt priority by writing to the relevant interrupt registers.
- 5. Configure the associated GPIO port pin (if using the Timer Output function) for the Timer Output alternate function.
- 6. Write to the Timer Control Register to enable the timer and initiate counting.

In CONTINUOUS Mode, the system clock always provides the timer input. The timer period is computed via the following equation:

CONTINUOUS Mode Time-Out Period (s) = $\frac{\text{Reload Value } \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$

If an initial starting value other than 0001H is loaded into the Timer High and Low Byte registers, use the ONE-SHOT Mode equation to determine the first time-out period.

COUNTER Mode

In COUNTER Mode, the timer counts input transitions from a GPIO port pin. The timer input is taken from the GPIO port pin Timer Input alternate function. The TPOL bit in the Timer Control Register selects whether the count occurs on the rising edge or the falling edge of the Timer Input signal. In COUNTER Mode, the prescaler is disabled.

Caution: The input frequency of the Timer Input signal must not exceed one-fourth the system clock frequency. Further, the high or low state of the input signal pulse must be no less than twice the system clock period. A shorter pulse may not be captured.

Upon reaching the reload value stored in the Timer Reload High and Low Byte registers, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. Also, if the Timer Output alternate function is

PWM SINGLE OUTPUT Mode

In PWM SINGLE OUTPUT Mode, the timer outputs a Pulse-Width Modulator (PWM) output signal through a GPIO port pin. The timer input is the system clock. The timer first counts up to the 16-bit PWM match value stored in the Timer PWM High and Low Byte registers. When the timer count value matches the PWM value, the Timer Output toggles. The timer continues counting until it reaches the reload value stored in the Timer Reload High and Low Byte registers. Upon reaching the reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes.

If the TPOL bit in the Timer Control Register is set to 1, the Timer Output signal begins as a High (1) and transitions to a Low (0) when the timer value matches the PWM value. The Timer Output signal returns to a High (1) after the timer reaches the reload value and is reset to 0001H.

If the TPOL bit in the Timer Control Register is set to 0, the Timer Output signal begins as a Low (0) and transitions to a High (1) when the timer value matches the PWM value. The Timer Output signal returns to a Low (0) after the timer reaches the reload value and is reset to 0001H.

Observe the following steps for configuring a timer for PWM SINGLE OUTPUT Mode and initiating the PWM operation:

- 1. Write to the Timer Control Register to:
 - Disable the timer
 - Configure the timer for PWM SINGLE OUTPUT Mode
 - Set the prescale value
 - Set the initial logic level (High or Low) and PWM High/Low transition for the Timer Output alternate function
- 2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H). This only affects the first pass in PWM mode. After the first timer reset in PWM mode, counting always begins at the reset value of 0001H.
- 3. Write to the PWM High and Low Byte registers to set the PWM value.
- 4. Write to the Timer Reload High and Low Byte registers to set the reload value (PWM period). The reload value must be greater than the PWM value.
- 5. If appropriate, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
- 6. Configure the associated GPIO port pin for the Timer Output alternate function.
- 7. Write to the Timer Control Register to enable the timer and initiate counting.

- 3. Write to the Timer Reload High and Low Byte registers to set the reload value.
- 4. Clear the Timer PWM High and Low Byte registers to 0000H. This allows the software to determine if interrupts were generated by either a capture event or a reload. If the PWM High and Low Byte registers still contain 0000H after the interrupt, the interrupt was generated by a Reload.
- 5. Enable the timer interrupt, if appropriate and set the timer interrupt priority by writing to the relevant interrupt registers. By default, the timer interrupt is generated for both input capture and reload events. If appropriate, configure the timer interrupt to be generated only at the input capture event or the reload event by setting TICONFIG field of the TxCTL0 Register.
- 6. Configure the associated GPIO port pin for the Timer Input alternate function.
- 7. Write to the Timer Control Register to enable the timer and initiate counting.

In CAPTURE Mode, the elapsed time from timer start to Capture event can be calculated using the following equation:

Capture Elapsed Time (s) = $\frac{(Capture Value - Start Value) \times Prescale}{System Clock Frequency (Hz)}$

COMPARE Mode

In COMPARE Mode, the timer counts up to the 16-bit maximum Compare value stored in the Timer Reload High and Low Byte registers. The timer input is the system clock. Upon reaching the Compare value, the timer generates an interrupt and counting continues (the timer value is not reset to 0001H). Also, if the Timer Output alternate function is enabled, the Timer Output pin changes state (from Low to High or from High to Low) upon Compare.

If the Timer reaches FFFFH, the timer rolls over to 0000H and continue counting.

Observe the following steps for configuring a timer for COMPARE Mode and initiating the count:

- 1. Write to the Timer Control Register to:
 - Disable the timer
 - Configure the timer for COMPARE Mode
 - Set the prescale value

UART Interrupts

The UART features separate interrupts for the transmitter and the receiver. In addition, when the UART primary functionality is disabled, the Baud Rate Generator can also function as a basic timer with interrupt capability.

Transmitter Interrupts

The transmitter generates a single interrupt when the Transmit Data Register Empty bit (TDRE) is set to 1. This indicates that the transmitter is ready to accept new data for transmission. The TDRE interrupt occurs after the Transmit Shift Register has shifted the first bit of data out. The Transmit Data Register can now be written with the next character to send. This action provides 7 bit periods of latency to load the Transmit Data Register before the Transmit Shift Register completes shifting the current character. Writing to the UART Transmit Data Register clears the TDRE bit to 0.

Receiver Interrupts

The receiver generates an interrupt when any of the following actions occur:

• A data byte is received and is available in the UART Receive Data Register. This interrupt can be disabled independently of the other receiver interrupt sources. The received data interrupt occurs after the receive character has been received and placed in the Receive Data Register. To avoid an overrun error, software must respond to this received data available condition before the next character is completely received.

Note: In MULTIPROCESSOR Mode (MPEN=1), the receive data interrupts are dependent on the multiprocessor configuration and the most recent address byte.

- A break is received.
- An overrun is detected.
- A data framing error is detected.

UART Overrun Errors

When an overrun error condition occurs the UART prevents overwriting of the valid data currently in the Receive Data Register. The Break Detect and Overrun status bits are not displayed until after the valid data has been read.

After the valid data has been read, the UART Status 0 Register is updated to indicate the overrun condition (and Break Detect, if applicable). The RDA bit is set to 1 to indicate that the Receive Data Register contains a data byte. However, because the overrun error occurred, this byte may not contain valid data and must be ignored. The BRKD bit indicates if the overrun was caused by a break condition on the line. After reading the status

Bit	7	6	5	4	3	2	1	0	
Field	REFSELH		Rese	Reserved			UFMODE[2:	0]	
RESET	1	0	0	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address				F7	1H				
Bit	Des	Description							
[/] REFSELH	 Voltage Reference Level Select High Bit In conjunction with the Low bit (REFSELL) in ADC Control Register 0, this determines the level of the internal voltage reference; the following details the effects of {REFSELI REFSELL}; this reference is independent of the Comparator reference. 00= Internal Reference Disabled, reference comes from external pin. 01= Internal Reference set to 1.0V. 10= Internal Reference set to 2.0V (default). 11= Reserved. 							etermines REFSELH,	
[6:3]	Reso Thes	Reserved These bits are reserved and must be programmed to 0000.							
[2:0] Input Buffer Mode Select BUFMODE[2:0] 000 = Single-ended, unbuffered input. 001 = Single-ended, buffered input with unity gain. 010 = Reserved. 011 = Reserved.									

Table 74. ADC Control/Status Register 1 (ADCCTL1)

100 = Differential, unbuffered input.101 = Differential, buffered input with unity gain.

110 = Reserved. 111 = Reserved.

ADC Data High Byte Register

The ADC Data High Byte (ADCD_H) Register contains the upper eight bits of the ADC output. The output is an 13-bit two's complement value. During a single-shot conversion, this value is invalid. Access to the ADC Data High Byte Register is read-only. Reading the ADC Data High Byte Register latches data in the ADC Low Bits Register.

Temperature Sensor

The on-chip Temperature Sensor allows you to measure temperature on the die with either the on-board ADC or on-board comparator. This block is factory calibrated for in-circuit software correction. Uncalibrated accuracy is significantly worse, therefore the temperature sensor is not recommended for uncalibrated use.

Temperature Sensor Operation

The on-chip temperature sensor is a Proportional to Absolute Temperature (PTAT) topology. A pair of Flash option bytes contain the calibration data. The temperature sensor can be disabled by a bit in the <u>Power Control Register 0</u> section on page 33 to reduce power consumption.

The temperature sensor can be directly read by the ADC to determine the absolute value of its output. The temperature sensor output is also available as an input to the comparator for threshold type measurement determination. The accuracy of the sensor when used with the comparator is substantially less than when measured by the ADC.

If the temperature sensor is routed to the ADC, the ADC must be configured in unity-gain buffered mode (for details, see the <u>Input Buffer Stage</u> section on page 133). The value read back from the ADC is a signed number, although it is always positive.

The sensor is factory-trimmed through the ADC using the external 2.0 V reference. Unless the sensor is retrimmed for use with a different reference, it is most accurate when used with the external 2.0 V reference.

Because this sensor is an on-chip sensor, Zilog recommends that the user account for the difference between ambient and die temperature when inferring ambient temperature conditions.

During normal operation, the die undergoes heating that causes a mismatch between the ambient temperature and that measured by the sensor. For best results, the Z8 Encore! XP device must be placed into STOP Mode for sufficient time such that the die and ambient temperatures converge (this time is dependent on the thermal design of the system). The temperature sensor measurement must then be made immediately after recovery from STOP Mode.

The following equation defines the transfer function between the temperature sensor output voltage and the die temperature. This is needed for comparator threshold measurements.

 $V = 0.01 \times T + 0.65$

Trim Bit Data Register

The Trim Bid Data (TRMDR) Register contains the read or write data for access to the trim option bits (Table 87).

Bit	7	6	5	4	3	2	1	0	
Field	TRMDR: Trim Bit Data								
RESET	0	0	0	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address	FF7H								

Table 87. Trim Bit Data Register (TRMDR)

Flash Option Bit Address Space

The first two bytes of Flash program memory at addresses 0000H and 0001H are reserved for the user-programmable Flash option bits.

Flash Program Memory Address 0000H

Bit	7	6	5	4	3	2	1	0		
Field	WDT_RES	WDT_AO	OSC_S	EL[1:0]	VBO_AO	FRP	Reserved	FWP		
RESET	U	U	U	U	U	U	U	U		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Address	s Program Memory 0000H									
Note: U =	Note: U = Unchanged by Reset, R/W = Read/Write.									

Table 88. Flash Option Bits at Program Memory Address 0000H

Note.	0 = 0 for angle by Reset. $R/W = Read/Whe.$
	

Bit	Description
[7] WDT_RES	 Watchdog Timer Reset 0 = Watchdog Timer time-out generates an interrupt request. Interrupts must be globally enabled for the eZ8 CPU to acknowledge the interrupt request. 1 = Watchdog Timer time-out causes a system reset. This setting is the default for unprogrammed (erased) Flash.
[6] WDT_AO	 Watchdog Timer Always On 0 = Watchdog Timer is automatically enabled upon application of system power. Watchdog Timer can not be disabled. 1 = Watchdog Timer is enabled upon execution of the WDT instruction. Once enabled, the Watchdog Timer can only be disabled by a Reset or Stop Mode Recovery. This setting is the default for unprogrammed (erased) Flash.

Trim Bit Address Space

All available Trim bit addresses and their functions are listed in Table 90 through Table 95.

Trim Bit Address 0000H

Bit	7	6	5	4	3	2	1	0			
Field		Reserved									
RESET	U	U	U	U	U	U	U	U			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
Address	Information Page Memory 0020H										
Note: U = Unchanged by Reset. R/W = Read/Write.											
Bit	Descriptio	Description									
[7:0]	Reserved										

Table 90. Trim Options Bits at Address 0000H

These bits are reserved; altering this register may result in incorrect device operation.

Trim Bit Address 0001H

Table 91. Trim Option Bits at 0001H

Bit	7	6	5	4	3	2	1	0	
Field	Reserved								
RESET	U	U	U	U	U	U	U	U	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address	Information Page Memory 0021H								
Note: U =	Note: U = Unchanged by Reset. R/W = Read/Write.								

Bit Description [7:0] Reserved These bits are reserved; altering this register may result in incorrect device operation.

Byte Write

To write a byte to the NVDS array, the user code must first push the address, then the data byte onto the stack. The user code issues a CALL instruction to the address of the byte-write routine (0x10B3). At the return from the sub-routine, the write status byte resides in working register R0. The bit fields of this status byte are defined in Table 106. The contents of the status byte are undefined for write operations to illegal addresses. Also, user code must pop the address and data bytes off the stack.

The write routine uses 13 bytes of stack space in addition to the two bytes of address and data pushed by the user. Sufficient memory must be available for this stack usage.

Because of the Flash memory architecture, NVDS writes exhibit a nonuniform execution time. In general, a write takes $251 \mu s$ (assuming a 20MHz system clock). Every 400 to 500 writes, however, a maintenance operation is necessary. In this rare occurrence, the write takes up to 61 ms to complete. Slower system clock speeds result in proportionally higher execution times.

NVDS byte writes to invalid addresses (those exceeding the NVDS array size) have no effect. Illegal write operations have a $2\mu s$ execution time.

Bit	7	6	5	4	3	2	1	0
Field	Reserved				RCPY	PF	AWE	DWE
Default Value	0	0	0	0	0	0	0	0

Table 106. Write Status Byte

Bit	Description
[7:4]	Reserved These bits are reserved and must be programmed to 0000.
[3]	Recopy Subroutine Executed
RCPY	A recopy subroutine was executed. These operations take significantly longer than a normal write operation.
[2]	Power Failure Indicator
PF	A power failure or system reset occurred during the most recent attempted write to the NVDS array.
[1]	Address Write Error
AWE	An address byte failure occurred during the most recent attempted write to the NVDS array.
[0]	Data Write Error
DWE	A data byte failure occurred during the most recent attempted write to the NVDS array.

 If the PA2/RESET pin is held Low while a 32-bit key sequence is issued to the PA0/ DBG pin, the DBG feature is unlocked. After releasing PA2/RESET, it is pulled High. At this point, the PA0/DBG pin may be used to autobaud and cause the device to enter DEBUG Mode. See the <u>OCD Unlock Sequence (8-Pin Devices Only) section on</u> page 185.

Exiting DEBUG Mode

The device exits DEBUG Mode following any of these operations:

- Clearing the DBGMODE bit in the OCD Control Register to 0
- Power-On Reset
- Voltage Brown-Out reset
- Watchdog Timer reset
- Asserting the RESET pin Low to initiate a Reset
- Driving the DBG pin Low while the device is in STOP Mode initiates a System Reset

OCD Data Format

The OCD interface uses the asynchronous data format defined for RS-232. Each character transmitted and received by the OCD consists of 1 Start bit, 8 data bits (least-significant bit first) and 1 Stop bit as displayed in Figure 26.

	START	D0	D1	D2	D3	D4	D5	D6	D7	STOP	
--	-------	----	----	----	----	----	----	----	----	------	--

Figure 26. OCD Data Format

Note: When responding to a request for data, the OCD may commence transmitting immediately after receiving the stop bit of an incoming frame. Therefore, when sending the stop bit, the host must not actively drive the DBG pin High for more than 0.5 bit times. Zilog recommends that, if possible, the host drives the DBG pin using an open drain output to avoid this issue.

OCD Auto-Baud Detector/Generator

To run over a range of baud rates (data bits per second) with various system clock frequencies, the On-Chip Debugger contains an Auto-Baud Detector/Generator. After a reset, the OCD is idle until it receives data. The OCD requires that the first character sent from the

Oscillator Control

The Z8 Encore! XP F082A Series devices uses five possible clocking schemes, each user-selectable:

- Internal precision trimmed RC oscillator (IPO)
- On-chip oscillator using off-chip crystal or resonator
- On-chip oscillator using external RC network
- External clock drive
- On-chip low power Watchdog Timer oscillator
- Clock failure detection circuitry

In addition, Z8 Encore! XP F082A Series devices contain clock failure detection and recovery circuitry, allowing continued operation despite a failure of the system clock oscillator.

Operation

This chapter discusses the logic used to select the system clock and handle primary oscillator failures.

System Clock Selection

The oscillator control block selects from the available clocks. Table 112 details each clock source and its usage.

Crystal Oscillator

The products in the Z8 Encore! XP F082A Series contain an on-chip crystal oscillator for use with external crystals with 32kHz to 20MHz frequencies. In addition, the oscillator supports external RC networks with oscillation frequencies up to 4MHz or ceramic resonators with frequencies up to 8MHz. The on-chip crystal oscillator can be used to generate the primary system clock for the internal eZ8 CPU and the majority of the on-chip peripherals. Alternatively, the X_{IN} input pin can also accept a CMOS-level clock input signal (32kHz–20MHz). If an external clock generator is used, the X_{OUT} pin must be left unconnected. The Z8 Encore! XP F082A Series products do not contain an internal clock divider. The frequency of the signal on the X_{IN} input pin determines the frequency of the system clock.

Note: Although the X_{IN} pin can be used as an input for an external clock generator, the CLKIN pin is better suited for such use (see the <u>System Clock Selection</u> section on page 193).

Operating Modes

The Z8 Encore! XP F082A Series products support four oscillator modes:

- Minimum power for use with very low frequency crystals (32kHz-1MHz)
- Medium power for use with medium frequency crystals or ceramic resonators (0.5 MHz to 8 MHz)
- Maximum power for use with high frequency crystals (8MHz to 20MHz)
- On-chip oscillator configured for use with external RC networks (<4MHz)

The oscillator mode is selected via user-programmable Flash option bits. See **the** <u>Flash</u> <u>Option Bits</u> chapter on page 159 for information.

Crystal Oscillator Operation

The XTLDIS Flash option bit controls whether the crystal oscillator is enabled during reset. The crystal may later be disabled after reset if a new oscillator has been selected as the system clock. If the crystal is manually enabled after reset through the OSCCTL Register, the user code must wait at least 1000 crystal oscillator cycles for the crystal to stabilize. After this, the crystal oscillator may be selected as the system clock.

Mnemonic	Operands	Instruction
BCLR	bit, dst	Bit Clear
BIT	p, bit, dst	Bit Set or Clear
BSET	bit, dst	Bit Set
BSWAP	dst	Bit Swap
CCF	—	Complement Carry Flag
RCF	_	Reset Carry Flag
SCF	—	Set Carry Flag
ТСМ	dst, src	Test Complement Under Mask
ТСМХ	dst, src	Test Complement Under Mask using Extended Addressing
ТМ	dst, src	Test Under Mask
TMX	dst, src	Test Under Mask using Extended Addressing

Table 121. Bit Manipulation Instructions

Table 122. Block Transfer Instructions

Mnemonic	Operands	Instruction
LDCI	dst, src	Load Constant to/from Program Memory and Auto- Increment Addresses
LDEI	dst, src	Load External Data to/from Data Memory and Auto- Increment Addresses

Table 123. CPU Control Instructions

Mnemonic	Operands	Instruction
ATM		Atomic Execution
CCF		Complement Carry Flag
DI	_	Disable Interrupts
EI	_	Enable Interrupts
HALT	_	Halt Mode
NOP		No Operation

		V _{DE}	_o = 2.7 V to 3	3.6 V		
Symbol	Parameter	Maximum Maximur Typical ¹ Std Temp ² Ext Temp		Maximum Ext Temp ³	Units	Conditions
I _{DD} ADCRef	ADC Internal Ref- erence Supply Cur- rent	0			μA	See Note 4.
I _{DD} CMP	Comparator sup- ply Current	150	180	190	μA	See Note 4.
I _{DD} LPO	Low-Power Opera- tional Amplifier Supply Current	3	5	5	μA	Driving a high-impedance load.
I _{DD} TS	Temperature Sen- sor Supply Current	60			μA	See Note 4.
I _{DD} BG	Band Gap Supply	320	480	500	μA	For 20-/28-pin devices.
	Current					For 8-pin devices.

Table 132. Power Consumption (Continued)

Notes:

1. Typical conditions are defined as $V_{DD} = 3.3 V$ and $+30^{\circ}C$.

2. Standard temperature is defined as $T_A = 0^{\circ}C$ to +70°C; these values not tested in production for worst case behavior, but are derived from product characterization and provided for design guidance only.

3. Extended temperature is defined as $T_A = -40^{\circ}$ C to +105°C; these values not tested in production for worst case behavior, but are derived from product characterization and provided for design guidance only.

4. For this block to operate, the bandgap circuit is automatically turned on and must be added to the total supply current. This bandgap current is only added once, regardless of how many peripherals are using it.

Z8 Encore! XP[®] F082A Series Product Specification

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