



Welcome to E-XFL.COM

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, Temp Sensor, WDT
Number of I/O	17
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	16 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f012ash020eg

Table 29.	Port A–C Input Data Registers (PxIN)	52
Table 30.	Port A–D Output Data Register (PxOUT)	52
Table 31.	LED Drive Enable (LEDEN)	53
Table 32.	LED Drive Level High Register (LEDLVLH)	53
Table 33.	LED Drive Level Low Register (LEDLVLL)	54
Table 34.	Trap and Interrupt Vectors in Order of Priority	56
Table 35.	Interrupt Request 0 Register (IRQ0)	60
Table 36.	Interrupt Request 1 Register (IRQ1)	61
Table 37.	Interrupt Request 2 Register (IRQ2)	62
Table 38.	IRQ0 Enable and Priority Encoding	62
Table 39.	IRQ0 Enable High Bit Register (IRQ0ENH)	63
Table 40.	IRQ0 Enable Low Bit Register (IRQ0ENL)	63
Table 41.	IRQ1 Enable and Priority Encoding	64
Table 42.	IRQ1 Enable Low Bit Register (IRQ1ENL)	65
Table 43.	IRQ1 Enable High Bit Register (IRQ1ENH)	65
Table 44.	IRQ2 Enable and Priority Encoding	66
Table 45.	IRQ2 Enable High Bit Register (IRQ2ENH)	66
Table 46.	Interrupt Edge Select Register (IRQES)	67
Table 47.	IRQ2 Enable Low Bit Register (IRQ2ENL)	67
Table 48.	Shared Interrupt Select Register (IRQSS)	68
Table 49.	Interrupt Control Register (IRQCTL)	69
Table 50.	Timer 0–1 Control Register 0 (TxCTL0)	85
Table 51.	Timer 0–1 Control Register 1 (TxCTL1)	86
Table 52.	Timer 0–1 High Byte Register (TxH)	90
Table 53.	Timer 0–1 Low Byte Register (TxL)	90
Table 54.	Timer 0–1 Reload High Byte Register (TxRH)	91
Table 55.	Timer 0–1 Reload Low Byte Register (TxRL)	91
Table 56.	Timer 0–1 PWM High Byte Register (TxPWMH)	92
Table 57.	Timer 0–1 PWM Low Byte Register (TxPWML)	92
Table 58.	Watchdog Timer Approximate Time-Out Delays	93

•

Internal Precision Oscillator

The internal precision oscillator (IPO) is a trimmable clock source that requires no external components.

Temperature Sensor

The optional temperature sensor produces an analog output proportional to the device temperature. This signal can be sent to either the ADC or the analog comparator.

Analog Comparator

The analog comparator compares the signal at an input pin with either an internal programmable voltage reference or a second input pin. The comparator output can be used to drive either an output pin or to generate an interrupt.

External Crystal Oscillator

The crystal oscillator circuit provides highly accurate clock frequencies with the use of an external crystal, ceramic resonator or RC network.

Low Voltage Detector

The low voltage detector (LVD) is able to generate an interrupt when the supply voltage drops below a user-programmable level. The LVD is available on 8-pin devices only.

On-Chip Debugger

The Z8 Encore! XP F082A Series products feature an integrated on-chip debugger (OCD) accessed via a single-pin interface. The OCD provides a rich-set of debugging capabilities, such as reading and writing registers, programming Flash memory, setting breakpoints and executing code.

Universal Asynchronous Receiver/Transmitter

The full-duplex universal asynchronous receiver/transmitter (UART) is included in all Z8 Encore! XP package types. The UART supports 8- and 9-bit data modes and selectable parity. The UART also supports multi-drop address processing in hardware. The UART baud rate generator (BRG) can be configured and used as a basic 16-bit timer.

Timers

Two enhanced 16-bit reloadable timers can be used for timing/counting events or for motor control operations. These timers provide a 16-bit programmable reload counter and

Table 2. Signal Descriptions (Continued)

Signal Mnemonic	I/O	Description
Reset		
$\overline{\text{RESET}}$	I/O	RESET. Generates a Reset when asserted (driven Low). Also serves as a reset indicator; the Z8 Encore! XP forces this pin low when in reset. This pin is open-drain and features an enabled internal pull-up resistor.
Power Supply		
V_{DD}	I	Digital Power Supply.
AV_{DD}	I	Analog Power Supply.
V_{SS}	I	Digital Ground.
AV_{SS}	I	Analog Ground.

Notes:

1. PB6 and PB7 are only available in 28-pin packages without ADC. In 28-pin packages with ADC, they are replaced by AV_{DD} and AV_{SS} .
2. The AV_{DD} and AV_{SS} signals are available only in 28-pin packages with ADC. They are replaced by PB6 and PB7 on 28-pin packages without ADC.

Pin Characteristics

Table 3 describes the characteristics for each pin available on the Z8 Encore! XP F082A Series 20- and 28-pin devices. Data in Table 3 is sorted alphabetically by the pin symbol mnemonic.

Table 4 on page 14 provides detailed information about the characteristics for each pin available on the Z8 Encore! XP F082A Series 8-pin devices.

► **Note:** All six I/O pins on the 8-pin packages are 5 V-tolerant (unless the pull-up devices are enabled). The column in Table 3 below describes 5 V-tolerance for the 20- and 28-pin packages only.

tor address. Following Stop

- Set the Capture edge (rising or falling) for the Timer Input
2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H).
 3. Write to the Timer Reload High and Low Byte registers to set the Compare value.
 4. Enable the timer interrupt, if appropriate and set the timer interrupt priority by writing to the relevant interrupt registers. By default, the timer interrupt are generated for both input capture and reload events. If appropriate, configure the timer interrupt to be generated only at the input capture event or the reload event by setting TICONFIG field of the TxCTL0 Register.
 5. Configure the associated GPIO port pin for the Timer Input alternate function.
 6. Write to the Timer Control Register to enable the timer.
 7. Counting begins on the first appropriate transition of the Timer Input signal. No interrupt is generated by this first edge.

In CAPTURE/COMPARE Mode, the elapsed time from timer start to Capture event can be calculated using the following equation:

$$\text{Capture Elapsed Time (s)} = \frac{(\text{Capture Value} - \text{Start Value}) \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

Reading the Timer Count Values

The current count value in the timers can be read while counting (enabled). This capability has no effect on timer operation. When the timer is enabled and the Timer High Byte Register is read, the contents of the Timer Low Byte Register are placed in a holding register. A subsequent read from the Timer Low Byte Register returns the value in the holding register. This operation allows accurate reads of the full 16-bit timer count value while enabled. When the timers are not enabled, a read from the Timer Low Byte Register returns the actual value in the counter.

Timer Pin Signal Operation

The timer output function is a GPIO port pin alternate function. The Timer Output is toggled every time the counter is reloaded.

Watchdog Timer

The Watchdog Timer (WDT) protects against corrupt or unreliable software, power faults and other system-level problems which may place the Z8 Encore! XP F082A Series devices into unsuitable operating states. The features of Watchdog Timer include:

Table 74. ADC Control/Status Register 1 (ADCCTL1)

Bit	7	6	5	4	3	2	1	0
Field	REFSELH	Reserved				BUFMODE[2:0]		
RESET	1	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F71H							

Bit	Description
[7] REFSELH	Voltage Reference Level Select High Bit In conjunction with the Low bit (REFSELL) in ADC Control Register 0, this determines the level of the internal voltage reference; the following details the effects of {REFSELH, REFSELL}; this reference is independent of the Comparator reference. 00= Internal Reference Disabled, reference comes from external pin. 01= Internal Reference set to 1.0V. 10= Internal Reference set to 2.0V (default). 11= Reserved.
[6:3]	Reserved These bits are reserved and must be programmed to 0000.
[2:0] BUFMODE[2:0]	Input Buffer Mode Select 000 = Single-ended, unbuffered input. 001 = Single-ended, buffered input with unity gain. 010 = Reserved. 011 = Reserved. 100 = Differential, unbuffered input. 101 = Differential, buffered input with unity gain. 110 = Reserved. 111 = Reserved.

ADC Data High Byte Register

The ADC Data High Byte (ADCD_H) Register contains the upper eight bits of the ADC output. The output is an 13-bit two's complement value. During a single-shot conversion, this value is invalid. Access to the ADC Data High Byte Register is read-only. Reading the ADC Data High Byte Register latches data in the ADC Low Bits Register.

Comparator

The Z8 Encore! XP F082A Series devices feature a general purpose comparator that compares two analog input signals. These analog signals may be external stimulus from a pin (CINP and/or CINN) or internally generated signals. Both a programmable voltage reference and the temperature sensor output voltage are available internally. The output is available as an interrupt source or can be routed to an external pin.

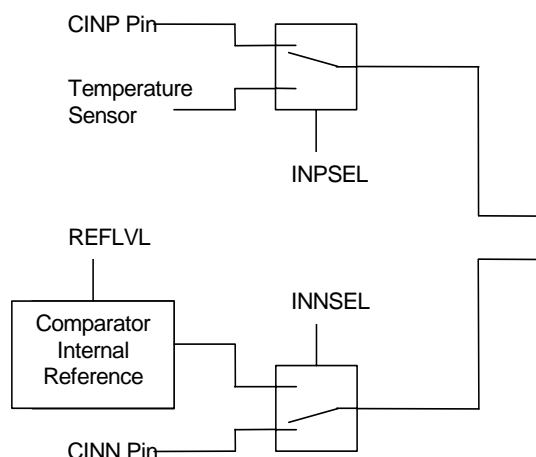


Figure 20. Comparator Block Diagram

Operation

When the positive comparator input exceeds the negative input by more than the specified hysteresis, the output is a logic High. When the negative input exceeds the positive by more than the hysteresis, the output is a logic Low. Otherwise, the comparator output retains its present value. See [Table 141](#) on page 238 for details.

The comparator may be powered down to reduce supply current. See the [Power Control Register 0](#) section on page 33 for details.

Because of the propagation delay of the comparator, Zilog does not recommend enabling or reconfiguring the comparator without first disabling the interrupts and waiting for the comparator output to settle. Doing so can result in spurious interrupts.

LEA 210
 load 210
 load constant 209
 load constant to/from program memory 210
 load constant with auto-increment addresses 210
 load effective address 210
 load external data 210
 load external data to/from data memory and auto-increment addresses 209
 load external to/from data memory and auto-increment addresses 210
 load using extended addressing 210
 logical AND 210
 logical AND/extended addressing 210
 logical exclusive OR 210
 logical exclusive OR/extended addressing 210
 logical instructions 210
 logical OR 210
 logical OR/extended addressing 210
 low power modes 32

M

master interrupt enable 57
 memory
 data 17
 program 15
 mode
 CAPTURE 87, 88
 CAPTURE/COMPARE 88
 CONTINUOUS 87
 COUNTER 87
 GATED 88
 ONE-SHOT 87
 PWM 87, 88
 modes 87
 MULT 208
 multiply 208
 multiprocessor mode, UART 105

N

NOP (no operation) 209
 notation

b 206
 cc 206
 DA 206
 ER 206
 IM 206
 IR 206
 Ir 206
 IRR 206
 Irr 206
 p 206
 R 206
 r 206
 RA 206
 RR 206
 rr 206
 vector 207
 X 207
 notational shorthand 206

O

OCD

architecture 180
 auto-baud detector/generator 183
 baud rate limits 184
 block diagram 180
 breakpoints 185
 commands 186
 control register 191
 data format 183
 DBG pin to RS-232 Interface 181
 debug mode 182
 debugger break 211
 interface 181
 serial errors 184
 status register 192
 timing 242

OCD commands

execute instruction (12H) 190
 read data memory (0DH) 190
 read OCD control register (05H) 188
 read OCD revision (00H) 187
 read OCD status register (02H) 187
 read program counter (07H) 188

- UARTx control 1 (UxCTL1) 112
- UARTx receive data (UxRXD) 116
- UARTx status 0 (UxSTAT0) 114
- UARTx status 1 (UxSTAT1) 115
- UARTx transmit data (UxTXD) 116
- Watchdog Timer control (WDTCTL) 30, 96, 141, 196
- Watchdog Timer reload high byte (WDTH) 97
- Watchdog Timer reload low byte (WDTL) 98
- Watchdog Timer reload upper byte (WDTU) 97
- register file 15
- register pair 206
- register pointer 207
- reset
 - and stop mode characteristics 23
 - and Stop Mode Recovery 22
 - carry flag 209
 - sources 24
- RET 211
- return 211
- RL 211
- RLC 211
- rotate and shift instructions 211
- rotate left 211
- rotate left through carry 211
- rotate right 211
- rotate right through carry 211
- RP 207
- RR 206, 211
- rr 206
- RRC 211

S

- SBC 208
- SCF 209, 210
- second opcode map after 1FH 225
- set carry flag 209, 210
- set register pointer 210
- shift right arithmetic 211
- shift right logical 211
- signal descriptions 10
- single-shot conversion (ADC) 126

- software trap 211
- source operand 207
- SP 207
- SRA 211
- src 207
- SRL 211
- SRP 210
- stack pointer 207
- STOP 210
- STOP mode 32
- stop mode 210
- Stop Mode Recovery
 - sources 27
 - using a GPIO port pin transition 28
 - using Watchdog Timer time-out 28
- stop mode recovery
 - sources 29
 - using a GPIO port pin transition 29
- SUB 208
- subtract 208
- subtract - extended addressing 208
- subtract with carry 208
- subtract with carry - extended addressing 208
- SUBX 208
- SWAP 211
- swap nibbles 211
- symbols, additional 207

T

- TCM 209
- TCMX 209
- test complement under mask 209
- test complement under mask - extended addressing 209
- test under mask 209
- test under mask - extended addressing 209
- timer signals 10
- timers 70
 - architecture 70
 - block diagram 71
 - CAPTURE mode 79, 80, 87, 88
 - CAPTURE/COMPARE mode 83, 88
 - COMPARE mode 81, 87