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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	64 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f021ahh020eg

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Revision History

Each instance in this document's revision history reflects a change from its previous edition. For more details, refer to the corresponding page(s) or appropriate links furnished in the table below.

Date	Revision Level	Chapter/Section	Description	Page No.
Dec 2012	27	Port Alternate Function Map- ping (Non 8-Pin Parts), Port Alternate Function Mapping (8- Pin Parts)	Added missing Port D data to Table 15; cor- rected active Low status (set overlines) for PA0 (TOOUT), PA2 (RESET) and PA5 (T1OUT) in Table 16.	<u>40, 43</u>
Sep 2011	26	LED Drive Enable Register	Clarified statement surrounding the Alternate Function Register as it relates to the LED function; revised Flash Sector Protect Regis- ter description; revised Packaging chapter.	<u>53,</u> <u>157,</u> <u>245</u>
Sep 2008	25	Overview, Address Space, Register Map, General-Pur- pose Input/Output, Available Packages, Ordering Informa- tion	Added references to F042A Series back in Table 1, Table 5, Table 7 and Table 14.	<u>2, 8,</u> <u>16, 18,</u> <u>36,</u> <u>246</u>
May 2008	24	Overview, Address Space, Register Map, General-Pur- pose Input/Output, Available Packages, Ordering Informa- tion	Changed title to Z8 Encore! XP F082A Series and removed references to F042A Series in Table 1, Table 5, Table 7 and Table 14.	<u>2, 8,</u> <u>16, 18,</u> <u>36,</u> <u>246</u>
Dec 2007	23	Pin Description, General-Pur- pose Input/Output, Watchdog Timer	Updated Figure 3, Table 15, Tables 60 through 62.	<u>9, 40,</u> <u>97</u>
Jul 2007	22	Electrical Characteristics	Updated Tables 16 and 132; power con- sumption data.	<u>43,</u> 229
Jun 2007	21	n/a	Revision number update.	All

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Block Diagram

Figure 1 displays the block diagram of the architecture of the Z8 Encore! XP F082A Series devices.





Internal Precision Oscillator

The internal precision oscillator (IPO) is a trimmable clock source that requires no external components.

Temperature Sensor

The optional temperature sensor produces an analog output proportional to the device temperature. This signal can be sent to either the ADC or the analog comparator.

Analog Comparator

The analog comparator compares the signal at an input pin with either an internal programmable voltage reference or a second input pin. The comparator output can be used to drive either an output pin or to generate an interrupt.

External Crystal Oscillator

The crystal oscillator circuit provides highly accurate clock frequencies with the use of an external crystal, ceramic resonator or RC network.

Low Voltage Detector

The low voltage detector (LVD) is able to generate an interrupt when the supply voltage drops below a user-programmable level. The LVD is available on 8-pin devices only.

On-Chip Debugger

The Z8 Encore! XP F082A Series products feature an integrated on-chip debugger (OCD) accessed via a single-pin interface. The OCD provides a rich-set of debugging capabilities, such as reading and writing registers, programming Flash memory, setting breakpoints and executing code.

Universal Asynchronous Receiver/Transmitter

The full-duplex universal asynchronous receiver/transmitter (UART) is included in all Z8 Encore! XP package types. The UART supports 8- and 9-bit data modes and selectable parity. The UART also supports multi-drop address processing in hardware. The UART baud rate generator (BRG) can be configured and used as a basic 16-bit timer.

Timers

Two enhanced 16-bit reloadable timers can be used for timing/counting events or for motor control operations. These timers provide a 16-bit programmable reload counter and



Figure 2. Z8F08xA, Z8F04xA, Z8F02xA and Z8F01xA in 8-Pin SOIC, QFN/MLF-S, or PDIP Package



Figure 3. Z8F08xA, Z8F04xA, Z8F02xA and Z8F01xA in 20-Pin SOIC, SSOP or PDIP Package



Figure 4. Z8F08xA, Z8F04xA, Z8F02xA and Z8F01xA in 28-Pin SOIC, SSOP or PDIP Package

GPIO Mode Interrupt Controller

The interrupt controller on the Z8 Encore! XP F082A Series products prioritizes the interrupt requests from the on-chip peripherals and the GPIO port pins. The features of interrupt controller include:

- 20 possible interrupt sources with 18 unique interrupt vectors:
 - Twelve GPIO port pin interrupt sources (two interrupt vectors are shared)
 - Eight on-chip peripheral interrupt sources (two interrupt vectors are shared)
- Flexible GPIO interrupts:
 - Eight selectable rising and falling edge GPIO interrupts
 - Four dual-edge interrupts
- Three levels of individually programmable interrupt priority
- Watchdog Timer and LVD can be configured to generate an interrupt
- Supports vectored and polled interrupts

Interrupt requests (IRQs) allow peripheral devices to suspend CPU operation in an orderly manner and force the CPU to start an interrupt service routine (ISR). Usually this interrupt service routine is involved with the exchange of data, status information, or control information between the CPU and the interrupting peripheral. When the service routine is completed, the CPU returns to the operation from which it was interrupted.

The eZ8 CPU supports both vectored and polled interrupt handling. For polled interrupts, the interrupt controller has no effect on operation. For more information about interrupt servicing by the eZ8 CPU, refer to the <u>eZ8 CPU Core User Manual (UM0128)</u>, which is available for download on <u>www.zilog.com</u>.

Interrupt Vector Listing

Table 34 lists all of the interrupts available in order of priority. The interrupt vector is stored with the most-significant byte (MSB) at the even Program Memory address and the least-significant byte (LSB) at the following odd Program Memory address.

Note: Some port interrupts are not available on the 8- and 20-pin packages. The ADC interrupt is unavailable on devices not containing an ADC.

into the Watchdog Timer Reload registers results in a one-second time-out at room temperature and 3.3V supply voltage. Time-outs other than one second may be obtained by scaling the calibration values up or down as required.

Note: The Watchdog Timer accuracy still degrades as temperature and supply voltage vary. See <u>Table 137</u> on page 235 for details.

Watchdog Timer Control Register Definitions

This section defines the features of the following Watchdog Timer Control registers.

Watchdog Timer Control Register (WDTCTL): see page 96

Watchdog Timer Reload Upper Byte Register (WDTU): see page 97

Watchdog Timer Reload High Byte Register (WDTH): see page 97

Watchdog Timer Reload Low Byte Register (WDTL): see page 98

Watchdog Timer Control Register

The Watchdog Timer Control (WDTCTL) Register is a write-only control register. Writing the 55H, AAH unlock sequence to the WDTCTL Register address unlocks the three Watchdog Timer Reload Byte registers (WDTU, WDTH and WDTL) to allow changes to the time-out period. These write operations to the WDTCTL Register address produce no effect on the bits in the WDTCTL Register. The locking mechanism prevents spurious writes to the reload registers. This register address is shared with the read-only Reset Status Register.

Bit	7	6	5	4	3	2	1	0
Field				WDT	JNLK			
RESET	Х	Х	Х	Х	Х	Х	Х	Х
R/W	W	W	W	W	W	W	W	W
Address	FF0H							
Note: X =	Note: X = Undefined.							

ы	Description
[7:0]	Watchdog Timer Unlock
WDTUNLK	The software must write the correct unlocking sequence to this register before it is allowed
	to modify the contents of the Watchdog Timer reload registers.

Description

Dit

Rate Generator to function as an additional counter if the UART functionality is not employed.

UART Baud Rate Generator

The UART Baud Rate Generator creates a lower frequency baud rate clock for data transmission. The input to the Baud Rate Generator is the system clock. The UART Baud Rate High and Low Byte registers combine to create a 16-bit baud rate divisor value (BRG[15:0]) that sets the data transmission rate (baud rate) of the UART. The UART data rate is calculated using the following equation:

UART Data Rate (bits/s) = $\frac{\text{System Clock Frequency (Hz)}}{16 \times \text{UART Baud Rate Divisor Value}}$

When the UART is disabled, the Baud Rate Generator functions as a basic 16-bit timer with an interrupt upon time-out. Observe the following steps to configure the Baud Rate Generator as a timer with an interrupt upon time-out:

- 1. Disable the UART by clearing the REN and TEN bits in the UART Control 0 Register to 0.
- 2. Load the acceptable 16-bit count value into the UART Baud Rate High and Low Byte registers.
- 3. Enable the Baud Rate Generator timer function and associated interrupt by setting the BRGCTL bit in the UART Control 1 Register to 1.

When configured as a general purpose timer, the interrupt interval is calculated using the following equation:

Interrupt Interval(s) = System Clock Period (s) \times BRG[15:0]

UART Control Register Definitions

The UART Control registers support the UART and the associated Infrared Encoder/ Decoders. For more information about infrared operation, see the <u>Infrared Encoder/</u><u>Decoder</u> chapter on page 120.

UART Control 0 and Control 1 Registers

The UART Control 0 (UxCTL0) and Control 1 (UxCTL1) registers, shown in Tables 63 and 64, configure the properties of the UART's transmit and receive operations. The UART Control registers must not be written while the UART is enabled.

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Compensation Steps:

1. Correct for Offset:

ADC LSB				
Offset LSB				
1				
#1 LSB				

2. Compute the absolute value of the offset-corrected ADC value *if negative*; the gain correction factor is computed assuming positive numbers, with sign restoration afterward.

|--|

Also compute the absolute value of the gain correction word, if negative.

AGain MSB AGain LSB

3. Multiply by the Gain Correction Word. If operating in DIFFERENTIAL Mode, there are two gain correction values: one for positive ADC values, another for negative ADC values. Use the appropriate Gain Correction Word based on the sign computed by byte #2.

#2 MSB	#2 LSB
*	

AGain MSB	AGain LSB

=

Bit	7	6	5	4	3	2	1	0
Field	ADCDH							
RESET	Х	Х	Х	Х	Х	Х	Х	Х
R/W	R	R	R	R	R	R	R	R
Address	F72H							
X = Undef	ined.							

Table 75. ADC Data High Byte Register (ADCD_H)

Bit Description [7:0] ADC Data High Byte ADCDH This byte contains the upper eight bits of the ADC output. These bits are not valid during a single-shot conversion. During a continuous conversion, the most recent conversion output is held in this register. These bits are undefined after a Reset.

ADC Data Low Byte Register

The ADC Data Low Byte (ADCD_L) Register contains the lower bits of the ADC output plus an overflow status bit. The output is a 13-bit two's complement value. During a single-shot conversion, this value is invalid. Access to the ADC Data Low Byte Register is read-only. Reading the ADC Data High Byte Register latches data in the ADC Low Bits Register.

Bit	7	6	5	4	3	2	1	0
Field	ADCDL					Rese	OVF	
RESET	Х	Х	Х	Х	Х	Х	Х	Х
R/W	R	R	R	R	R	R	R	R
Address	s F73H							
X = Undefined.								

Table 76. ADC Data Low Byte Register (ADCD_L)

Bit	Description
[7:3]	ADC Data Low Bits
ADCDL	These bits are the least significant five bits of the 13-bits of the ADC output. These bits are undefined after a Reset.

The following code example illustrates how to safely enable the comparator:

Comparator Control Register Definition

The Comparator Control Register (CMP0) configures the comparator inputs and sets the value of the internal voltage reference.

Bit	7	6	5	4	3	2	1	0
Field	INPSEL	INNSEL		REF	Reserved (20-/28-pin) REFLVL (8-pin)			
RESET	0	0	0	1	0	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F90H							

Table 77. Comparator Control Register (CMP0)

Bit	Description
[7] INPSEL	Signal Select for Positive Input 0 = GPIO pin used as positive comparator input. 1 = Temperature sensor used as positive comparator input.
[6] INNSEL	Signal Select for Negative Input 0 = Internal reference disabled, GPIO pin used as negative comparator input. 1 = Internal reference enabled as negative comparator input.

Flash Memory

The products in the Z8 Encore! XP F082A Series feature a nonvolatile Flash memory of 8KB (8192), 4 KB (4096), 2 KB (2048 bytes), or 1 KB (1024) with read/write/erase capability. The Flash Memory can be programmed and erased in-circuit by user code or through the On-Chip Debugger. The features include:

- User controlled read and write protect capability
- Sector-based write protection scheme
- Additional protection schemes against accidental program and erasure

Architecture

The Flash memory array is arranged in pages with 512 bytes per page. The 512-byte page is the minimum Flash block size that can be erased. Each page is divided into 8 rows of 64 bytes.

For program or data protection, the Flash memory is also divided into sectors. In the Z8 Encore! XP F082A Series, these sectors are either 1024 bytes (in the 8KB devices) or 512 bytes (all other memory sizes) in size. Page and sector sizes are not generally equal.

The first 2 bytes of Flash Program memory are used as Flash option bits. For more information about their operation, see the <u>Flash Option Bits</u> chapter on page 159.

Table 78 describes the Flash memory configuration for each device in the Z8 Encore! XP F082A Series. Figure 21 displays the Flash memory arrangement.

Part Number	Flash Size KB (Bytes)	Flash Pages	Program Memory Addresses	Flash Sector Size (Bytes)
Z8F08xA	8 (8192)	16	0000H–1FFFH	1024
Z8F04xA	4 (4096)	8	0000H-0FFFH	512
Z8F02xA	2 (2048)	4	0000H-07FFH	512
Z8F01xA	1 (1024)	2	0000H-03FFH	512

Table 78. Z8 Encore! XP F082A Series Flash Memory Configurations

Flash Program Memory Address 0001H

Table 89. Flash Options Bits at Program Memory Address 0001H

Bit	7	6	5	4	3	2	1	0
Field	Reserved			XTLDIS	Reserved			
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Program Memory 0001H							

Note: U = Unchanged by Reset. R/W = Read/Write.

Bit	Description
[7:5]	Reserved
	These bits are reserved and must be programmed to 111.
[4]	State of the Crystal Oscillator at Reset
XTLDIS	This bit only enables the crystal oscillator. Its selection as a system clock must be performed manually.
	0 = Crystal oscillator is enabled during reset, resulting in longer reset timing.
	1 = Crystal oscillator is disabled during reset, resulting in shorter reset timing.
	Caution: Programming the XTLDIS bit to zero on 8-pin versions of this device prevents any further communication via the debug pin due to the fact that the XIN and DBG functions are shared on pin 2 of this package. Do not program this bit to zero on 8-pin devices unless further debugging or Flash programming is not required.
[3:0]	Reserved These bits are reserved and must be programmed to 1111

Trim Bit Address Space

All available Trim bit addresses and their functions are listed in Table 90 through Table 95.

Trim Bit Address 0000H

Bit	7	6	5	4	3	2	1	0		
Field		Reserved								
RESET	U	U	U	U	U	U	U	U		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Address	Information Page Memory 0020H									
Note: U = Unchanged by Reset. R/W = Read/Write.										
Bit	Description									
[7:0]	Reserved									

Table 90. Trim Options Bits at Address 0000H

These bits are reserved; altering this register may result in incorrect device operation.

Trim Bit Address 0001H

Table 91. Trim Option Bits at 0001H

Bit	7	6	5	4	3	2	1	0	
Field	Reserved								
RESET	U	U	U	U	U	U	U	U	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address	Information Page Memory 0021H								
Note: U = Unchanged by Reset. R/W = Read/Write.									

Bit Description [7:0] Reserved These bits are reserved; altering this register may result in incorrect device operation.

Unlock and write Oscillator Control

Register (OSCCTL) to enable and

select oscillator at either 5.53MHz or

• Configure Flash option bits for correct

Unlock and write OSCCTL to enable

crystal oscillator, wait for it to stabilize and select as system clock (if the XTLDIS option bit has been deasserted, no waiting is required)

Configure Flash option bits for correct

Unlock and write OSCCTL to enable crystal oscillator and select as system

• Write GPIO registers to configure PB3

Unlock and write OSCCTL to select

Apply external clock signal to GPIO

· Enable WDT if not enabled and wait

until WDT Oscillator is operating Unlock and write Oscillator Control

pin for external clock function

external system clock

external oscillator mode

external oscillator mode

Very low power consumption	Register (OSCCTL) to enable an select oscillator			
Caution: Unintentional accesses to the Oscillator switching to a nonfunctioning oscillator. block employs a register unlocking/locki	Control Register can actually stop the chip To prevent this condition, the oscillator con ing scheme.			
OSC Control Register Unlocking/	/Locking			
To write the Oscillator Control Register, un Register with the values E7H followed by 1 changes the value of the actual register and	nlock it by making two writes to the OSCC 18H. A third write to the OSCCTL Register returns the register to a locked state. Any o			

Required Setup

32.8kHz

clock

stop the chip by oscillator control

> s to the OSCCTL CTL Register ed state. Any other sequence of Oscillator Control Register writes has no effect. The values written to unlock the register must be ordered correctly, but are not necessarily consecutive. It is possible to write to or read from other registers within the unlocking/locking operation.

Clock Source

RC Oscillator

Internal Precision

External Crystal/

External Clock

Internal Watchdog

Timer Oscillator

Resonator

tor

Drive

Characteristics

High accuracy

• 32kHz to 20MHz

ponents

0 to 20MHz

• 10kHz nominal

nents required

source

•

External RC Oscilla- • 32kHz to 4MHz

• 32.8kHz or 5.53MHz

No external components required

Very high accuracy (dependent on

· Accuracy dependent on external com-

Accuracy dependent on external clock

Low accuracy; no external compo-

crystal or resonator used)

Requires external components

When selecting a new clock source, the system clock oscillator failure detection circuitry and the Watchdog Timer oscillator failure circuitry must be disabled. If SOFEN and WOFEN are not disabled prior to a clock switch-over, it is possible to generate an interrupt for a failure of either oscillator. The Failure detection circuitry can be enabled anytime after a successful write of OSCSEL in the OSCCTL Register.

The internal precision oscillator is enabled by default. If the user code changes to a different oscillator, it may be appropriate to disable the IPO for power savings. Disabling the IPO does not occur automatically.

Clock Failure Detection and Recovery

Should an oscillator or timer fail, there are methods of recovery, as this section describes.

System Clock Oscillator Failure

The Z8F04xA family devices can generate nonmaskable interrupt-like events when the primary oscillator fails. To maintain system function in this situation, the clock failure recovery circuitry automatically forces the Watchdog Timer oscillator to drive the system clock. The Watchdog Timer oscillator must be enabled to allow the recovery. Although this oscillator runs at a much slower speed than the original system clock, the CPU continues to operate, allowing execution of a clock failure vector and software routines that either remedy the oscillator failure or issue a failure alert. This automatic switch-over is not available if the Watchdog Timer oscillator is disabled, though it is not necessary to enable the Watchdog Timer reset function (see the <u>Watchdog Timer</u> chapter on page 93).

The primary oscillator failure detection circuitry asserts if the system clock frequency drops below $1 \text{ kHz} \pm 50\%$. If an external signal is selected as the system oscillator, it is possible that a very slow but nonfailing clock can generate a failure condition. Under these conditions, do not enable the clock failure circuitry (SOFEN must be deasserted in the OSCCTL Register).

Watchdog Timer Failure

In the event of a Watchdog Timer oscillator failure, a similar nonmaskable interrupt-like event is issued. This event does not trigger an attendant clock switch-over, but alerts the CPU of the failure. After a Watchdog Timer failure, it is no longer possible to detect a primary oscillator failure. The failure detection circuitry does not function if the Watchdog Timer is used as the system clock oscillator or if the Watchdog Timer oscillator has been disabled. For either of these cases, it is necessary to disable the detection circuitry by deasserting the WDFEN bit of the OSCCTL Register.

The Watchdog Timer oscillator failure detection circuit counts system clocks while looking for a Watchdog Timer clock. The logic counts 8004 system clock cycles before determining that a failure has occurred. The system clock rate determines the speed at which

Crystal Oscillator

The products in the Z8 Encore! XP F082A Series contain an on-chip crystal oscillator for use with external crystals with 32kHz to 20MHz frequencies. In addition, the oscillator supports external RC networks with oscillation frequencies up to 4MHz or ceramic resonators with frequencies up to 8MHz. The on-chip crystal oscillator can be used to generate the primary system clock for the internal eZ8 CPU and the majority of the on-chip peripherals. Alternatively, the X_{IN} input pin can also accept a CMOS-level clock input signal (32kHz–20MHz). If an external clock generator is used, the X_{OUT} pin must be left unconnected. The Z8 Encore! XP F082A Series products do not contain an internal clock divider. The frequency of the signal on the X_{IN} input pin determines the frequency of the system clock.

Note: Although the X_{IN} pin can be used as an input for an external clock generator, the CLKIN pin is better suited for such use (see the <u>System Clock Selection</u> section on page 193).

Operating Modes

The Z8 Encore! XP F082A Series products support four oscillator modes:

- Minimum power for use with very low frequency crystals (32kHz-1MHz)
- Medium power for use with medium frequency crystals or ceramic resonators (0.5 MHz to 8 MHz)
- Maximum power for use with high frequency crystals (8MHz to 20MHz)
- On-chip oscillator configured for use with external RC networks (<4MHz)

The oscillator mode is selected via user-programmable Flash option bits. See **the** <u>Flash</u> <u>Option Bits</u> chapter on page 159 for information.

Crystal Oscillator Operation

The XTLDIS Flash option bit controls whether the crystal oscillator is enabled during reset. The crystal may later be disabled after reset if a new oscillator has been selected as the system clock. If the crystal is manually enabled after reset through the OSCCTL Register, the user code must wait at least 1000 crystal oscillator cycles for the crystal to stabilize. After this, the crystal oscillator may be selected as the system clock.

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Figure 32. Second Opcode Map after 1FH

		T _A =	–40°C to +			
Symbol	ol Parameter	Minimum	Typical ¹	Maximum	Units	Conditions
T _{RAMP}	Time for V_{DD} to transition from V_{SS} to V_{POR} to ensure valid Reset	0.10	-	100	ms	
T _{SMP}	Stop Mode Recovery pin pulse rejection period		20		ns	For any SMR pin or for the Reset pin when it is asserted in STOP Mode.
Note:	Data in the typical column is from character	rization at 3.3	/ and 30°C. 1	hese values a	re provid	ed for design

Table 135. Power-On Reset and Voltage Brown-Out Electrical Characteristics and Timing

ng
l

	V _{DD} T _A = · (unless	= 2.7 V to -40°C to + otherwise	3.6 V 105°C e stated)				
Parameter	Minimum	Typical	Maximum	Units	Notes		
Flash Byte Read Time	100	_	_	ns			
Flash Byte Program Time	20	_	40	μs			
Flash Page Erase Time	10	_	-	ms			
Flash Mass Erase Time	200	_	_	ms			
Writes to Single Address Before Next Erase	-	-	2				
Flash Row Program Time	-	-	8	ms	Cumulative program time for single row cannot exceed limit before next erase. This parameter is only an issue when bypassing the Flash Controller.		
Data Retention	100	_	_	years	25°C		
Endurance	10,000	_	_	cycles	Program/erase cycles		

Part Number	Flash	RAM	SDVN	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description
Z8 Encore! XP F082A Series with 2 KB Flash											
Standard Temperature: 0°C to 70°C											
Z8F021APB020SG	2 KB	512 B	64 B	6	13	2	0	1	1	0	PDIP 8-pin package
Z8F021AQB020SG	2 KB	512 B	64 B	6	13	2	0	1	1	0	QFN 8-pin package
Z8F021ASB020SG	2 KB	512 B	64 B	6	13	2	0	1	1	0	SOIC 8-pin package
Z8F021ASH020SG	2 KB	512 B	64 B	17	19	2	0	1	1	0	SOIC 20-pin package
Z8F021AHH020SG	2 KB	512 B	64 B	17	19	2	0	1	1	0	SSOP 20-pin package
Z8F021APH020SG	2 KB	512 B	64 B	17	19	2	0	1	1	0	PDIP 20-pin package
Z8F021ASJ020SG	2 KB	512 B	64 B	25	19	2	0	1	1	0	SOIC 28-pin package
Z8F021AHJ020SG	2 KB	512 B	64 B	25	19	2	0	1	1	0	SSOP 28-pin package
Z8F021APJ020SG	2 KB	512 B	64 B	25	19	2	0	1	1	0	PDIP 28-pin package
Extended Temperatu	ıre: –40°	°C to 10	5°C								
Z8F021APB020EG	2 KB	512 B	64 B	6	13	2	0	1	1	0	PDIP 8-pin package
Z8F021AQB020EG	2 KB	512 B	64 B	6	13	2	0	1	1	0	QFN 8-pin package
Z8F021ASB020EG	2 KB	512 B	64 B	6	13	2	0	1	1	0	SOIC 8-pin package
Z8F021ASH020EG	2 KB	512 B	64 B	17	19	2	0	1	1	0	SOIC 20-pin package
Z8F021AHH020EG	2 KB	512 B	64 B	17	19	2	0	1	1	0	SSOP 20-pin package
Z8F021APH020EG	2 KB	512 B	64 B	17	19	2	0	1	1	0	PDIP 20-pin package
Z8F021ASJ020EG	2 KB	512 B	64 B	25	19	2	0	1	1	0	SOIC 28-pin package
Z8F021AHJ020EG	2 KB	512 B	64 B	25	19	2	0	1	1	0	SSOP 28-pin package
Z8F021APJ020EG	2 KB	512 B	64 B	25	19	2	0	1	1	0	PDIP 28-pin package

Table 148. Z8 Encore! XP F082A Series Ordering Matrix

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Part Number	Flash	RAM	NVDS	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description
Z8 Encore! XP F082A Series Development Kit											
Z8F08A28100KITG		Z8 Enco	ore! XP	F082/	A Ser	ies 2	8-Pin	Deve	elopm	nent K	it
Z8F04A28100KITG		Z8 Enco	ore! XP	F042/	A Ser	ies 2	8-Pin	Deve	elopm	nent K	it
Z8F04A08100KITG		Z8 Enco	ore! XP	F042	A Ser	ies 8	-Pin I	Devel	opme	ent Kit	
ZUSBSC00100ZACG		USB Sm	nart Ca	ble Ac	cess	ory K	it				
ZUSBOPTSC01ZACG		USB Op	to-Isol	ated S	mart	Cabl	e Acc	cesso	ry Kit		
ZENETSC0100ZACG		Etherne	t Smar	t Cable	e Acc	esso	ry Kit				

Table 148. Z8 Encore! XP F082A Series Ordering Matrix