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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	64 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f021ahh020sg

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

## Z8 Encore! XP<sup>®</sup> F082A Series Product Specification

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## **Internal Precision Oscillator**

The internal precision oscillator (IPO) is a trimmable clock source that requires no external components.

## **Temperature Sensor**

The optional temperature sensor produces an analog output proportional to the device temperature. This signal can be sent to either the ADC or the analog comparator.

## **Analog Comparator**

The analog comparator compares the signal at an input pin with either an internal programmable voltage reference or a second input pin. The comparator output can be used to drive either an output pin or to generate an interrupt.

## **External Crystal Oscillator**

The crystal oscillator circuit provides highly accurate clock frequencies with the use of an external crystal, ceramic resonator or RC network.

## Low Voltage Detector

The low voltage detector (LVD) is able to generate an interrupt when the supply voltage drops below a user-programmable level. The LVD is available on 8-pin devices only.

## **On-Chip Debugger**

The Z8 Encore! XP F082A Series products feature an integrated on-chip debugger (OCD) accessed via a single-pin interface. The OCD provides a rich-set of debugging capabilities, such as reading and writing registers, programming Flash memory, setting breakpoints and executing code.

## **Universal Asynchronous Receiver/Transmitter**

The full-duplex universal asynchronous receiver/transmitter (UART) is included in all Z8 Encore! XP package types. The UART supports 8- and 9-bit data modes and selectable parity. The UART also supports multi-drop address processing in hardware. The UART baud rate generator (BRG) can be configured and used as a basic 16-bit timer.

## Timers

Two enhanced 16-bit reloadable timers can be used for timing/counting events or for motor control operations. These timers provide a 16-bit programmable reload counter and

## **Reset Sources**

Table 9 lists the possible sources of a system reset.

	Table 9. Reset Source	ces and Resulting Reset Type
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Operating Mode	Reset Source	Special Conditions
NORMAL or HALT modes	Power-On Reset/Voltage Brown- Out	Reset delay begins after supply voltage exceeds POR level.
	Watchdog Timer time-out when configured for Reset	None.
	RESET pin assertion	All reset pulses less than three system clocks in width are ignored.
	On-Chip Debugger initiated Reset (OCDCTL[0] set to 1)	System Reset, except the On-Chip Debugger is unaffected by the reset.
STOP Mode	Power-On Reset/Voltage Brown- Out	Reset delay begins after supply voltage exceeds POR level.
	RESET pin assertion	All reset pulses less than the specified analog delay are ignored. See Table 131 on page 229.
	DBG pin driven Low	None.

## **Power-On Reset**

Z8 Encore! XP F082A Series devices contain an internal Power-On Reset circuit. The POR circuit monitors the supply voltage and holds the device in the Reset state until the supply voltage reaches a safe operating level. After the supply voltage exceeds the POR voltage threshold (VPOR), the device is held in the Reset state until the POR Counter has timed out. If the crystal oscillator is enabled by the option bits, this time-out is longer.

After the Z8 Encore! XP F082A Series device exits the Power-On Reset state, the eZ8 CPU fetches the Reset vector. Following Power-On Reset, the POR status bit in the Reset Status (RSTSTAT) Register is set to 1.

Figure 5 displays Power-On Reset operation. See Electrical Characteristics on page 221 for the POR threshold voltage (V<sub>POR</sub>).

and as long as four. A reset pulse three clock cycles in duration might trigger a reset; a pulse four cycles in duration always triggers a reset.

While the RESET input pin is asserted Low, the Z8 Encore! XP F082A Series devices remain in the Reset state. If the RESET pin is held Low beyond the System Reset timeout, the device exits the Reset state on the system clock rising edge following RESET pin deassertion. Following a System Reset initiated by the external RESET pin, the EXT status bit in the Reset Status (RSTSTAT) Register is set to 1.

#### **External Reset Indicator**

During System Reset or when enabled by the GPIO logic (see <u>Table 20 on page 46</u>), the <u>RESET</u> pin functions as an open-drain (active Low) reset mode indicator in addition to the input functionality. This reset output feature allows a Z8 Encore! XP F082A Series device to reset other components to which it is connected, even if that reset is caused by internal sources such as POR, VBO or WDT events.

After an internal reset event occurs, the internal circuitry begins driving the RESET pin Low. The RESET pin is held Low by the internal circuitry until the appropriate delay listed in Table 8 has elapsed.

#### **On-Chip Debugger Initiated Reset**

A Power-On Reset can be initiated using the On-Chip Debugger by setting the RST bit in the OCD Control Register. The On-Chip Debugger block is not reset but the rest of the chip goes through a normal system reset. The RST bit automatically clears during the system reset. Following the system reset the POR bit in the Reset Status (RSTSTAT) Register is set.

## Stop Mode Recovery

STOP Mode is entered by execution of a STOP instruction by the eZ8 CPU. See the <u>Low-Power Modes</u> chapter on page 32 for detailed STOP Mode information. During Stop Mode Recovery (SMR), the CPU is held in reset for 66 IPO cycles if the crystal oscillator is disabled or 5000 cycles if it is enabled. The SMR delay (see <u>Table 135</u> on page 233)  $T_{SMR}$ , also includes the time required to start up the IPO.

Stop Mode Recovery does not affect on-chip registers other than the Watchdog Timer Control Register (WDTCTL) and the Oscillator Control Register (OSCCTL). After any Stop Mode Recovery, the IPO is enabled and selected as the system clock. If another system clock source is required, the Stop Mode Recovery code must reconfigure the oscillator control block such that the correct system clock source is enabled and selected.

The eZ8 CPU fetches the Reset vector at Program Memory addresses 0002H and 0003H and loads that value into the Program Counter. Program execution begins at the Reset vec-



**Note:** Asserting any power control bit disables the targeted block regardless of any enable bits contained in the target block's control registers.

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## Port A–C Input Data Registers

Reading from the Port A–C Input Data registers, shown in Table 29, return the sampled values from the corresponding port pins. The Port A–C Input Data registers are read-only. The value returned for any unused ports is 0. Unused ports include those missing on the 8-and 28-pin packages, as well as those missing on the ADC-enabled 28-pin packages.

Bit	7	6	5	4	3	2	1	0	
Field	PIN7	PIN6	PIN5	PIN4	PIN3	PIN2	PIN1	PIN0	
RESET	Х	Х	Х	Х	Х	Х	Х	Х	
R/W	R	R	R	R	R	R	R	R	
Address		FD2H, FD6H, FDAH							
X = Undef	X = Undefined.								

Table 29. Port A–C Input Data Registers (PxIN)

Bit	Description
[7:0]	Port Input Data
PxIN	Sampled data from the corresponding port pin input.
	0 = Input data is logical 0 (Low).
	1 = Input data is logical 1 (High).

Note: x indicates the specific GPIO port pin number (7–0).

## Port A–D Output Data Register

The Port A–D Output Data Register, shown in Table 30, controls the output data to the pins.

Bit	7	6	5	4	3	2	1	0
Field	POUT7	POUT6	POUT5	POUT4	POUT3	POUT2	POUT1	POUT0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address			F	D3H, FD7H,	FDBH, FDF	Ή		

Table 30. Port A–D Output Data Register (PxOUT)

#### Bit Description

[7:0] **Port Output Data** PxOUT These bits contain the data to be driven to the port pins. The values are only driven if the corresponding pin is configured as an output and the pin is not configured for alternate function operation. 0 = Drive a logical 0 (Low).

1 = Drive a logical 1 (High). High value is not driven if the drain has been disabled by setting the corresponding Port Output Control Register bit to 1.

Note: x indicates the specific GPIO port pin number (7–0).



## Operation

The timers are 16-bit up-counters. Minimum time-out delay is set by loading the value 0001H into the Timer Reload High and Low Byte registers and setting the prescale value to 1. Maximum time-out delay is set by loading the value 0000H into the Timer Reload High and Low Byte registers and setting the prescale value to 128. If the Timer reaches FFFFH, the timer rolls over to 0000H and continues counting.

## **Timer Operating Modes**

The timers can be configured to operate in the following modes:

#### **ONE-SHOT Mode**

In ONE-SHOT Mode, the timer counts up to the 16-bit reload value stored in the Timer Reload High and Low byte registers. The timer input is the system clock. Upon reaching the reload value, the timer generates an interrupt and the count value in the Timer High and Low Byte registers is reset to 0001H. The timer is automatically disabled and stops counting.

Also, if the Timer Output alternate function is enabled, the Timer Output pin changes state for one system clock cycle (from Low to High or from High to Low) upon timer Reload. If

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- 3. Write to the Timer Reload High and Low Byte registers to set the reload value.
- 4. Clear the Timer PWM High and Low Byte registers to 0000H. This allows the software to determine if interrupts were generated by either a capture event or a reload. If the PWM High and Low Byte registers still contain 0000H after the interrupt, the interrupt was generated by a Reload.
- 5. Enable the timer interrupt, if appropriate and set the timer interrupt priority by writing to the relevant interrupt registers. By default, the timer interrupt is generated for both input capture and reload events. If appropriate, configure the timer interrupt to be generated only at the input capture event or the reload event by setting TICONFIG field of the TxCTL0 Register.
- 6. Configure the associated GPIO port pin for the Timer Input alternate function.
- 7. Write to the Timer Control Register to enable the timer and initiate counting.

In CAPTURE Mode, the elapsed time from timer start to Capture event can be calculated using the following equation:

Capture Elapsed Time (s) =  $\frac{(Capture Value - Start Value) \times Prescale}{System Clock Frequency (Hz)}$ 

#### **COMPARE Mode**

In COMPARE Mode, the timer counts up to the 16-bit maximum Compare value stored in the Timer Reload High and Low Byte registers. The timer input is the system clock. Upon reaching the Compare value, the timer generates an interrupt and counting continues (the timer value is not reset to 0001H). Also, if the Timer Output alternate function is enabled, the Timer Output pin changes state (from Low to High or from High to Low) upon Compare.

If the Timer reaches FFFFH, the timer rolls over to 0000H and continue counting.

Observe the following steps for configuring a timer for COMPARE Mode and initiating the count:

- 1. Write to the Timer Control Register to:
  - Disable the timer
  - Configure the timer for COMPARE Mode
  - Set the prescale value

## **Timer Reload High and Low Byte Registers**

The Timer 0–1 Reload High and Low Byte (TxRH and TxRL) registers, shown in Tables 54 and 55, store a 16-bit reload value, {TRH[7:0], TRL[7:0]}. Values written to the Timer Reload High Byte Register are stored in a temporary holding register. When a write to the Timer Reload Low Byte Register occurs, the temporary holding register value is written to the Timer High Byte Register. This operation allows simultaneous updates of the 16-bit Timer reload value.

In COMPARE Mode, the Timer Reload High and Low Byte registers store the 16-bit Compare value.

Bit	7	6	5	4	3	2	1	0
Field	TRH							
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address				F02H,	F0AH			

#### Table 54. Timer 0–1 Reload High Byte Register (TxRH)

Bit	7	6	5	4	3	2	1	0	
Field		TRL							
RESET	1	1	1	1	1	1	1	1	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address				F03H,	F0BH				

Bit	Description
[7:0]	Timer Reload Register High and Low
TRH, TRL	These two bytes form the 16-bit reload value, {TRH[7:0], TRL[7:0]}. This value sets the max- imum count value which initiates a timer reload to 0001H. In COMPARE Mode, these two bytes form the 16-bit Compare value.





first. An even or odd parity bit can be added to the data stream. Each character begins with an active Low start bit and ends with either 1 or 2 active High stop bits. Figures 11 and 12 display the asynchronous data format employed by the UART without parity and with parity, respectively.



The UART is now configured for interrupt-driven data reception. When the UART Receiver interrupt is detected, the associated interrupt service routine (ISR) performs the following:

- 1. Checks the UART Status 0 Register to determine the source of the interrupt error, break, or received data.
- 2. Reads the data from the UART Receive Data Register if the interrupt was because of data available. If operating in MULTIPROCESSOR (9-bit) Mode, further actions may be required depending on the MULTIPROCESSOR Mode bits MPMD[1:0].
- 3. Clears the UART Receiver interrupt in the applicable Interrupt Request Register.
- 4. Executes the IRET instruction to return from the interrupt-service routine and await more data.

## Clear To Send (CTS) Operation

The CTS pin, if enabled by the CTSE bit of the UART Control 0 Register, performs flow control on the outgoing transmit datastream. The Clear To Send ( $\overline{\text{CTS}}$ ) input pin is sampled one system clock before beginning any new character transmission. To delay transmission of the next data character, an external receiver must deassert  $\overline{\text{CTS}}$  at least one system clock cycle before a new data transmission begins. For multiple character transmissions, this action is typically performed during Stop Bit transmission. If  $\overline{\text{CTS}}$  deasserts in the middle of a character transmission, the current character is sent completely.

## MULTIPROCESSOR (9-bit) Mode

The UART features a MULTIPROCESSOR (9-bit) Mode that uses an extra (9th) bit for selective communication when a number of processors share a common UART bus. In MULTIPROCESSOR Mode (also referred to as *9-bit Mode*), the multiprocessor bit (MP) is transmitted immediately following the 8-bits of data and immediately preceding the Stop bit(s) as displayed in Figure 13. The character format is:



Figure 13. UART Asynchronous MULTIPROCESSOR Mode Data Format

Acceptable Rate (kHz)	BRG Divisor (Decimal)	Actual Rate (kHz)	Error (%)	Acceptable Rate (kHz)	BRG Divisor (Decimal)	Actual Rate (kHz)	Error (%)
1250.0	N/A	N/A	N/A	1250.0	N/A	N/A	N/A
625.0	N/A	N/A	N/A	625.0	N/A	N/A	N/A
250.0	1	223.72	-10.51	250.0	N/A	N/A	N/A
115.2	2	111.9	-2.90	115.2	1	115.2	0.00
57.6	4	55.9	-2.90	57.6	2	57.6	0.00
38.4	6	37.3	-2.90	38.4	3	38.4	0.00
19.2	12	18.6	-2.90	19.2	6	19.2	0.00
9.60	23	9.73	1.32	9.60	12	9.60	0.00
4.80	47	4.76	-0.83	4.80	24	4.80	0.00
2.40	93	2.41	0.23	2.40	48	2.40	0.00
1.20	186	1.20	0.23	1.20	96	1.20	0.00
0.60	373	0.60	-0.04	0.60	192	0.60	0.00
0.30	746	0.30	-0.04	0.30	384	0.30	0.00

#### Table 72. UART Baud Rates (Continued)

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Figure 22 displays a basic Flash Controller flow. The following subsections provide details about the various operations displayed in Figure 22.



Figure 22. Flash Controller Operation Flow Chart

ter with 5EH. After the Flash Sector Protect Register is selected, it can be accessed at the Page Select Register address. When user code writes the Flash Sector Protect Register, bits can only be set to 1. Thus, sectors can be protected, but not unprotected, via register write operations. Writing a value other than 5EH to the Flash Control Register deselects the Flash Sector Protect Register and reenables access to the Page Select Register.

Observe the following procedure to setup the Flash Sector Protect Register from user code:

- 1. Write 00H to the Flash Control Register to reset the Flash Controller.
- 2. Write 5EH to the Flash Control Register to select the Flash Sector Protect Register.
- 3. Read and/or write the Flash Sector Protect Register which is now at Register File address FF9H.
- 4. Write 00H to the Flash Control Register to return the Flash Controller to its reset state.

The Sector Protect Register is initialized to 0 on reset, putting each sector into an unprotected state. When a bit in the Sector Protect Register is written to 1, the corresponding sector is no longer written or erased by the CPU. External Flash programming through the OCD or via the Flash Controller Bypass mode are unaffected. After a bit of the Sector Protect Register has been set, it cannot be cleared except by powering down the device.

#### **Byte Programming**

Flash Memory is enabled for byte programming after unlocking the Flash Controller and successfully enabling either Mass Erase or Page Erase. When the Flash Controller is unlocked and Mass Erase is successfully completed, all Program Memory locations are available for byte programming. In contrast, when the Flash Controller is unlocked and Page Erase is successfully completed, only the locations of the selected page are available for byte programming. An erased Flash byte contains all 1's (FFH). The programming operation can only be used to change bits from 1 to 0. To change a Flash bit (or multiple bits) from 0 to 1 requires execution of either the Page Erase or Mass Erase commands.

Byte Programming can be accomplished using the On-Chip Debugger's Write Memory command or eZ8 CPU execution of the LDC or LDCI instructions. Refer to the <u>eZ8 CPU</u> <u>Core User Manual (UM0128)</u>, available for download on <u>www.zilog.com</u>, for a description of the LDC and LDCI instructions. While the Flash Controller programs the Flash memory, the eZ8 CPU idles but the system clock and on-chip peripherals continue to operate. To exit programming mode and lock the Flash, write any value to the Flash Control Register, except the Mass Erase or Page Erase commands.

 If the PA2/RESET pin is held Low while a 32-bit key sequence is issued to the PA0/ DBG pin, the DBG feature is unlocked. After releasing PA2/RESET, it is pulled High. At this point, the PA0/DBG pin may be used to autobaud and cause the device to enter DEBUG Mode. See the <u>OCD Unlock Sequence (8-Pin Devices Only) section on</u> page 185.

#### **Exiting DEBUG Mode**

The device exits DEBUG Mode following any of these operations:

- Clearing the DBGMODE bit in the OCD Control Register to 0
- Power-On Reset
- Voltage Brown-Out reset
- Watchdog Timer reset
- Asserting the RESET pin Low to initiate a Reset
- Driving the DBG pin Low while the device is in STOP Mode initiates a System Reset

#### OCD Data Format

The OCD interface uses the asynchronous data format defined for RS-232. Each character transmitted and received by the OCD consists of 1 Start bit, 8 data bits (least-significant bit first) and 1 Stop bit as displayed in Figure 26.

	START	D0	D1	D2	D3	D4	D5	D6	D7	STOP	
--	-------	----	----	----	----	----	----	----	----	------	--

Figure 26. OCD Data Format

**Note:** When responding to a request for data, the OCD may commence transmitting immediately after receiving the stop bit of an incoming frame. Therefore, when sending the stop bit, the host must not actively drive the DBG pin High for more than 0.5 bit times. Zilog recommends that, if possible, the host drives the DBG pin using an open drain output to avoid this issue.

### **OCD Auto-Baud Detector/Generator**

To run over a range of baud rates (data bits per second) with various system clock frequencies, the On-Chip Debugger contains an Auto-Baud Detector/Generator. After a reset, the OCD is idle until it receives data. The OCD requires that the first character sent from the

# **Oscillator Control**

The Z8 Encore! XP F082A Series devices uses five possible clocking schemes, each user-selectable:

- Internal precision trimmed RC oscillator (IPO)
- On-chip oscillator using off-chip crystal or resonator
- On-chip oscillator using external RC network
- External clock drive
- On-chip low power Watchdog Timer oscillator
- Clock failure detection circuitry

In addition, Z8 Encore! XP F082A Series devices contain clock failure detection and recovery circuitry, allowing continued operation despite a failure of the system clock oscillator.

## Operation

This chapter discusses the logic used to select the system clock and handle primary oscillator failures.

## **System Clock Selection**

The oscillator control block selects from the available clocks. Table 112 details each clock source and its usage.

the Watchdog Timer failure can be detected. A very slow system clock results in very slow detection times.

**Caution:** It is possible to disable the clock failure detection circuitry and all functioning clock sources. In this case, the Z8 Encore! XP F082A Series device ceases functioning and can only be recovered by Power-On-Reset.

## **Oscillator Control Register Definitions**

The Oscillator Control Register (OSCCTL) enables/disables the various oscillator circuits, enables/disables the failure detection/recovery circuitry and selects the primary oscillator, which becomes the system clock.

The Oscillator Control Register must be unlocked before writing. Unlock the Oscillator Control Register by writing the two-step sequence E7H followed by 18H. The register is locked at successful completion of a register write to the OSCCTL.

Bit	7	6	5	4	3	2	1	0
Field	INTEN	XTLEN	WDTEN	SOFEN	WDFEN		SCKSEL	
RESET	1	0	1	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F86H							

Table 113. Oscillator Control Register (OSCCTL)

Bit	Description
[7] INTEN	Internal Precision Oscillator Enable 1 = Internal precision oscillator is enabled. 0 = Internal precision oscillator is disabled.
[6] XTLEN	Crystal Oscillator Enable; this setting overrides the GPIO register control for PA0 and PA1 1 = Crystal oscillator is enabled. 0 = Crystal oscillator is disabled.
[5] WDTEN	Watchdog Timer Oscillator Enable1 = Watchdog Timer oscillator is enabled.0 = Watchdog Timer oscillator is disabled.
[4] SOFEN	System Clock Oscillator Failure Detection Enable1 = Failure detection and recovery of system clock oscillator is enabled.0 = Failure detection and recovery of system clock oscillator is disabled.

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Figure 29. Typical RC Oscillator Frequency as a Function of the External Capacitance with a  $45k\Omega$  Resistor

**Caution:** When using the external RC oscillator mode, the oscillator can stop oscillating if the power supply drops below 2.7 V, but before the power supply drops to the Voltage Brown-Out threshold. The oscillator resumes oscillation when the supply voltage exceeds 2.7 V.

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#### Table 123. CPU Control Instructions (Continued)

Mnemonic	Operands	Instruction
RCF	_	Reset Carry Flag
SCF	—	Set Carry Flag
SRP	src	Set Register Pointer
STOP	—	STOP Mode
WDT		Watchdog Timer Refresh

#### Table 124. Load Instructions

Mnemonic	Operands	Instruction
CLR	dst	Clear
LD	dst, src	Load
LDC	dst, src	Load Constant to/from Program Memory
LDCI	dst, src	Load Constant to/from Program Memory and Auto- Increment Addresses
LDE	dst, src	Load External Data to/from Data Memory
LDEI	dst, src	Load External Data to/from Data Memory and Auto- Increment Addresses
LDWX	dst, src	Load Word using Extended Addressing
LDX	dst, src	Load using Extended Addressing
LEA	dst, X(src)	Load Effective Address
POP	dst	Рор
POPX	dst	Pop using Extended Addressing
PUSH	src	Push
PUSHX	src	Push using Extended Addressing

#### Table 125. Logical Instructions

Mnemonic	Operands	Instruction
AND	dst, src	Logical AND
ANDX	dst, src	Logical AND using Extended Addressing
COM	dst	Complement
OR	dst, src	Logical OR
ORX	dst, src	Logical OR using Extended Addressing
XOR	dst, src	Logical Exclusive OR
XORX	dst, src	Logical Exclusive OR using Extended Addressing

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