Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	64 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.173", 4.40mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f021ahj020eg

tor address. Following Stop Mode Recovery, the STOP bit in the Reset Status (RSTSTAT) Register is set to 1. Table 10 lists the Stop Mode Recovery sources and resulting actions. The text following provides more detailed information about each of the Stop Mode Recovery sources.

Table 10. Stop Mode Recovery Sources and Resulting Action

Operating Mode	Stop Mode Recovery Source	Action
STOP Mode	Watchdog Timer time-out when configured for Reset	Stop Mode Recovery
	Watchdog Timer time-out when configured for interrupt	Stop Mode Recovery followed by interrupt (if interrupts are enabled)
	Data transition on any GPIO port pin enabled as a Stop Mode Recovery source	Stop Mode Recovery
	Assertion of external $\overline{\text{RESET}}$ Pin	System Reset
	Debug Pin driven Low	System Reset

Stop Mode Recovery Using Watchdog Timer Time-Out

If the Watchdog Timer times out during STOP Mode, the device undergoes a Stop Mode Recovery sequence. In the Reset Status (RSTSTAT) Register, the WDT and STOP bits are set to 1. If the Watchdog Timer is configured to generate an interrupt upon time-out and the Z8 Encore! XP F082A Series device is configured to respond to interrupts, the eZ8 CPU services the Watchdog Timer interrupt request following the normal Stop Mode Recovery sequence.

Stop Mode Recovery Using a GPIO Port Pin Transition

Each of the GPIO port pins may be configured as a Stop Mode Recovery input source. On any GPIO pin enabled as a Stop Mode Recovery source, a change in the input pin value (from High to Low or from Low to High) initiates Stop Mode Recovery.

Note: SMR pulses shorter than specified do not trigger a recovery (see Table 135 on page 233). In this instance, the STOP bit in the Reset Status (RSTSTAT) Register is set to 1.

Caution: In STOP Mode, the GPIO Port Input Data registers (PxIN) are disabled. The Port Input Data registers record the Port transition only if the signal stays on the Port pin through the end of the Stop Mode Recovery delay. As a result, short pulses on the Port pin can initiate Stop Mode Recovery without being written to the Port Input Data Register or

Table 12. Reset and Stop Mode Recovery Bit Descriptions

Reset or Stop Mode Recovery Event	POR	STOP	WDT	EXT
Power-On Reset	1	0	0	0
Reset using $\overline{\text{RESET}}$ pin assertion	0	0	0	1
Reset using Watchdog Timer time-out	0	0	1	0
Reset using the On-Chip Debugger (OCTCTL[1] set to 1)	1	0	0	0
Reset from STOP Mode using DBG Pin driven Low	1	0	0	0
Stop Mode Recovery using GPIO pin transition	0	1	0	0
Stop Mode Recovery using Watchdog Timer time-out	0	1	1	0

Note: Asserting any power control bit disables the targeted block regardless of any enable bits contained in the target block's control registers.

Table 46. IRQ2 Enable Low Bit Register (IRQ2ENL)

Bit	7	6	5	4	3	2	1	0
Field	Reserved				C3ENL	C2ENL	C1ENL	C0ENL
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC8H							

Bit	Description
[7:4]	**Reserved** These bits are reserved and must be programmed to 0000.
[3] C3ENL	**Port C3 Interrupt Request Enable Low Bit**
[2] C2ENL	**Port C2 Interrupt Request Enable Low Bit**
[1] C1ENL	**Port C1 Interrupt Request Enable Low Bit**
[0] C0ENL	**Port C0 Interrupt Request Enable Low Bit**

Interrupt Edge Select Register

The Interrupt Edge Select (IRQES) Register, shown in Table 47, determines whether an interrupt is generated for the rising edge or falling edge on the selected GPIO Port A input pin.

Table 47. Interrupt Edge Select Register (IRQES)

Bit	7	6	5	4	3	2	1	0
Field	IES7	IES6	IES5	IES4	IES3	IES2	IES1	IES0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FCDH							

Bit	Description
[7:0] IESx	**Interrupt Edge Select *x*** 0 = An interrupt request is generated on the falling edge of the PA*x* input. 1 = An interrupt request is generated on the rising edge of the PA*x* input.

Note: x indicates the specific GPIO port pin number (0–7).

Rate Generator to function as an additional counter if the UART functionality is not employed.

UART Baud Rate Generator

The UART Baud Rate Generator creates a lower frequency baud rate clock for data transmission. The input to the Baud Rate Generator is the system clock. The UART Baud Rate High and Low Byte registers combine to create a 16-bit baud rate divisor value (BRG[15:0]) that sets the data transmission rate (baud rate) of the UART. The UART data rate is calculated using the following equation:

$$\text{UART Data Rate (bits/s)} = \frac{\text{System Clock Frequency (Hz)}}{16 \times \text{UART Baud Rate Divisor Value}}$$

When the UART is disabled, the Baud Rate Generator functions as a basic 16-bit timer with an interrupt upon time-out. Observe the following steps to configure the Baud Rate Generator as a timer with an interrupt upon time-out:

1. Disable the UART by clearing the REN and TEN bits in the UART Control 0 Register to 0.
2. Load the acceptable 16-bit count value into the UART Baud Rate High and Low Byte registers.
3. Enable the Baud Rate Generator timer function and associated interrupt by setting the BRGCTL bit in the UART Control 1 Register to 1.

When configured as a general purpose timer, the interrupt interval is calculated using the following equation:

$$\text{Interrupt Interval(s)} = \text{System Clock Period (s)} \times \text{BRG[15:0]}$$

UART Control Register Definitions

The UART Control registers support the UART and the associated Infrared Encoder/Decoders. For more information about infrared operation, see the Infrared Encoder/Decoder chapter on page 120.

UART Control 0 and Control 1 Registers

The UART Control 0 (UxCTL0) and Control 1 (UxCTL1) registers, shown in Tables 63 and 64, configure the properties of the UART's transmit and receive operations. The UART Control registers must not be written while the UART is enabled.

- Write to BUFMODE[2:0] to select SINGLE-ENDED or DIFFERENTIAL mode, plus unbuffered or buffered mode.
- Write the REFSELH bit of the pair {REFSELH, REFSELL} to select the internal voltage reference level or to disable the internal reference. The REFSELL bit is contained in the ADC Control Register 0.

3. Write to the ADC Control Register 0 to configure the ADC for continuous conversion. The bit fields in the ADC Control Register may be written simultaneously:
   - Write to the ANAIN[3:0] field to select from the available analog input sources (different input pins available depending on the device).
   - Set CONT to 1 to select continuous conversion.
   - If the internal VREF must be output to a pin, set the REFEXT bit to 1. The internal voltage reference must be enabled in this case.
   - Write the REFSELL bit of the pair {REFSELH, REFSELL} to select the internal voltage reference level or to disable the internal reference. The REFSELH bit is contained in ADC Control/Status Register 1.
   - Set CEN to 1 to start the conversions.
4. When the first conversion in continuous operation is complete (after 5129 system clock cycles, plus the 40 cycles for power-up, if necessary), the ADC control logic performs the following operations:
   - CEN resets to 0 to indicate the first conversion is complete. CEN remains 0 for all subsequent conversions in continuous operation
   - An interrupt request is sent to the Interrupt Controller to indicate the conversion is complete
5. The ADC writes a new data result every 256 system clock cycles. For each completed conversion, the ADC control logic performs the following operations:
   - Writes the 13-bit two's complement result to {ADCD_H[7:0], ADCD_L[7:3]}
   - Sends an interrupt request to the Interrupt Controller denoting conversion complete
6. To disable continuous conversion, clear the CONT bit in the ADC Control Register to 0.

Interrupts

The ADC is able to interrupt the CPU when a conversion has been completed. When the ADC is disabled, no new interrupts are asserted; however, an interrupt pending when the ADC is disabled is not cleared.

Table 75. ADC Data High Byte Register (ADCD_H)

Bit	7	6	5	4	3	2	1	0
Field	ADCDH							
RESET	X	X	X	X	X	X	X	X
R/W	R	R	R	R	R	R	R	R
Address	F72H							
X = Undefined.								

Bit	Description
[7:0] ADCDH	**ADC Data High Byte** This byte contains the upper eight bits of the ADC output. These bits are not valid during a single-shot conversion. During a continuous conversion, the most recent conversion output is held in this register. These bits are undefined after a Reset.

ADC Data Low Byte Register

The ADC Data Low Byte (ADCD_L) Register contains the lower bits of the ADC output plus an overflow status bit. The output is a 13-bit two's complement value. During a single-shot conversion, this value is invalid. Access to the ADC Data Low Byte Register is read-only. Reading the ADC Data High Byte Register latches data in the ADC Low Bits Register.

Table 76. ADC Data Low Byte Register (ADCD_L)

Bit	7	6	5	4	3	2	1	0
Field	ADCDL					Reserved		OVF
RESET	X	X	X	X	X	X	X	X
R/W	R	R	R	R	R	R	R	R
Address	F73H							
X = Undefined.								

Bit	Description
[7:3] ADCDL	**ADC Data Low Bits** These bits are the least significant five bits of the 13-bits of the ADC output. These bits are undefined after a Reset.

Bit	Description (Continued)
[2:1]	**Reserved** These bits are reserved and must be undefined.
[0] OVF	**Overflow Status** 0 = A hardware overflow did not occur in the ADC for the current sample. 1= A hardware overflow did occur in the ADC for the current sample, therefore the current sample is invalid.

Comparator

The Z8 Encore! XP F082A Series devices feature a general purpose comparator that compares two analog input signals. These analog signals may be external stimulus from a pin (CINP and/or CINN) or internally generated signals. Both a programmable voltage reference and the temperature sensor output voltage are available internally. The output is available as an interrupt source or can be routed to an external pin.

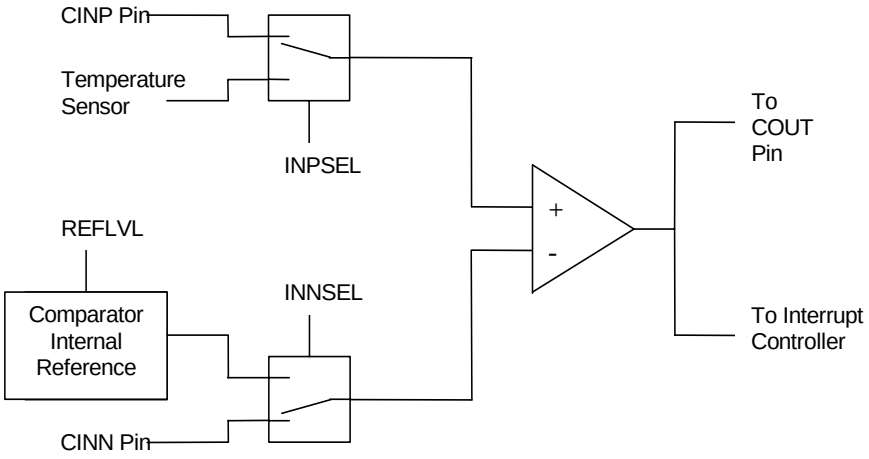

Figure 20. Comparator Block Diagram

Operation

When the positive comparator input exceeds the negative input by more than the specified hysteresis, the output is a logic High. When the negative input exceeds the positive by more than the hysteresis, the output is a logic Low. Otherwise, the comparator output retains its present value. See Table 141 on page 238 for details.

The comparator may be powered down to reduce supply current. See the Power Control Register 0 section on page 33 for details.

! Caution: Because of the propagation delay of the comparator, Zilog does not recommend enabling or reconfiguring the comparator without first disabling the interrupts and waiting for the comparator output to settle. Doing so can result in spurious interrupts.

Bit	Description (Continued)
[5:2] REFLVL	**Internal Reference Voltage Level** This reference is independent of the ADC voltage reference. **Note:** 8-pin devices contain two additional LSBs for increased resolution. For 20-/28-pin devices: 0000 = 0.0 V 0001 = 0.2 V 0010 = 0.4 V 0011 = 0.6 V 0100 = 0.8 V 0101 = 1.0 V (Default) 0110 = 1.2 V 0111 = 1.4 V 1000 = 1.6 V 1001 = 1.8 V 1010–1111 = Reserved

Operation

This section describes the interface and modes of operation of the On-Chip Debugger.

OCD Interface

The on-chip debugger uses the DBG pin for communication with an external host. This one-pin interface is a bidirectional, open-drain interface that transmits and receives data. Data transmission is half-duplex, in that transmit and receive cannot occur simultaneously. The serial data on the DBG pin is sent using the standard asynchronous data format defined in RS-232. This pin creates an interface from the Z8 Encore! XP F082A Series products to the serial port of a host PC using minimal external hardware.Two different methods for connecting the DBG pin to an RS-232 interface are displayed in Figure 24 and Figure 25. The recommended method is the buffered implementation displayed in Figure 25. The DBG pin has a internal pull-up resistor which is sufficient for some applications (for more details about the pull-up current, see the Electrical Characteristics chapter on page 226). For OCD operation at higher data rates or in noisy systems, an external pull-up resistor is recommended.

! Caution: For operation of the on-chip debugger, all power pins (V_{DD} and AV_{DD}) must be supplied with power and all ground pins (V_{SS} and AV_{SS}) must be properly grounded. The DBG pin is open-drain and may require an external pull-up resistor to ensure proper operation.

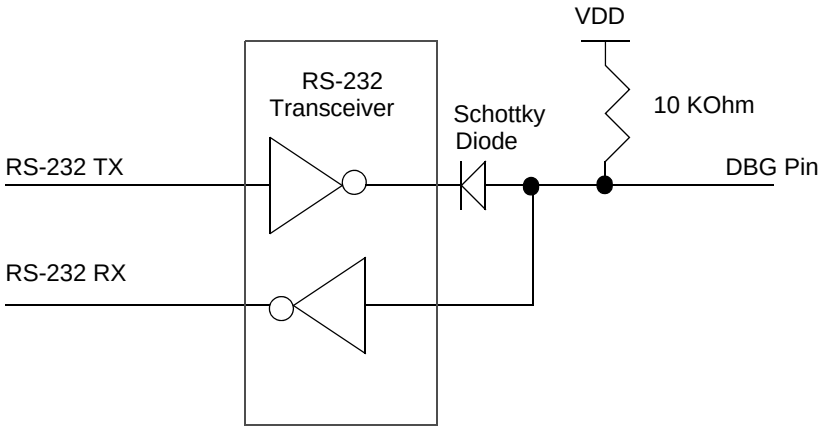

Figure 24. Interfacing the On-Chip Debugger's DBG Pin with an RS-232 Interface; #1 of 2

enabled, the OCD ignores the BRK signal and the BRK instruction operates as an NOP instruction.

Breakpoints in Flash Memory

The BRK instruction is opcode 00H, which corresponds to the fully programmed state of a byte in Flash memory. To implement a Breakpoint, write 00H to the required break address, overwriting the current instruction. To remove a Breakpoint, the corresponding page of Flash memory must be erased and reprogrammed with the original data.

Runtime Counter

The On-Chip Debugger contains a 16-bit Runtime Counter. It counts system clock cycles between Breakpoints. The counter starts counting when the On-Chip Debugger leaves DEBUG Mode and stops counting when it enters DEBUG Mode again or when it reaches the maximum count of FFFFH.

On-Chip Debugger Commands

The host communicates to the on-chip debugger by sending OCD commands using the DBG interface. During normal operation, only a subset of the OCD commands are available. In DEBUG Mode, all OCD commands become available unless the user code and control registers are protected by programming the Flash Read Protect Option bit (FRP). The Flash Read Protect Option bit prevents the code in memory from being read out of the Z8 Encore! XP F082A Series device. When this option is enabled, several of the OCD commands are disabled. See Table 109.

Table 110 on page 191 is a summary of the on-chip debugger commands. Each OCD command is described in further detail in the bulleted list following this table. Table 110 also indicates those commands that operate when the device is not in DEBUG Mode (normal operation) and those commands that are disabled by programming the Flash Read Protect Option bit.

Table 109. Debug Command Enable/Disable

Debug Command	Command Byte	Enabled when Not in DEBUG Mode?	Disabled by Flash Read Protect Option Bit
Read OCD Revision	00H	Yes	–
Reserved	01H	–	–
Read OCD Status Register	02H	Yes	–
Read Runtime Counter	03H	–	–
Write OCD Control Register	04H	Yes	Cannot clear DBGMODE bit.
Read OCD Control Register	05H	Yes	–

Table 128. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode dst	Address Mode src	Opcode(s) (Hex)	Flags C	Z	S	V	D	H	Fetch Cycles	Instr. Cycles
AND dst, src	dst ← dst AND src	r	r	52	–	*	*	0	–	–	2	3
		r	Ir	53							2	4
		R	R	54							3	3
		R	IR	55							3	4
		R	IM	56							3	3
		IR	IM	57							3	4
ANDX dst, src	dst ← dst AND src	ER	ER	58	–	*	*	0	–	–	4	3
		ER	IM	59							4	3
ATM	Block all interrupt and DMA requests during execution of the next 3 instructions			2F	–	–	–	–	–	–	1	2
BCLR bit, dst	dst[bit] ← 0	r		E2	–	–	–	–	–	–	2	2
BIT p, bit, dst	dst[bit] ← p	r		E2	–	–	–	–	–	–	2	2
BRK	Debugger Break			00	–	–	–	–	–	–	1	1
BSET bit, dst	dst[bit] ← 1	r		E2	–	–	–	–	–	–	2	2
BSWAP dst	dst[7:0] ← dst[0:7]	R		D5	X	*	*	0	–	–	2	2
BTJ p, bit, src, dst	if src[bit] = p PC ← PC + X		r	F6	–	–	–	–	–	–	3	3
			Ir	F7							3	4
BTJNZ bit, src, dst	if src[bit] = 1 PC ← PC + X		r	F6	–	–	–	–	–	–	3	3
			Ir	F7							3	4
BTJZ bit, src, dst	if src[bit] = 0 PC ← PC + X		r	F6	–	–	–	–	–	–	3	3
			Ir	F7							3	4

Note: Flags Notation:
* = Value is a function of the result of the operation.
– = Unaffected.
X = Undefined.
0 = Reset to 0.
1 = Set to 1.

Table 128. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode dst	Address Mode src	Opcode(s) (Hex)	Flags C	Z	S	V	D	H	Fetch Cycles	Instr. Cycles
LDX dst, src	dst ← src	r	ER	84	–	–	–	–	–	–	3	2
		Ir	ER	85							3	3
		R	IRR	86							3	4
		IR	IRR	87							3	5
		r	X(rr)	88							3	4
		X(rr)	r	89							3	4
		ER	r	94							3	2
		ER	Ir	95							3	3
		IRR	R	96							3	4
		IRR	IR	97							3	5
		ER	ER	E8							4	2
		ER	IM	E9							4	2
LEA dst, X(src)	dst ← src + X	r	X(r)	98	–	–	–	–	–	–	3	3
		rr	X(rr)	99							3	5
MULT dst	dst[15:0] ← dst[15:8] * dst[7:0]	RR		F4	–	–	–	–	–	–	2	8
NOP	No operation			0F	–	–	–	–	–	–	1	2
OR dst, src	dst ← dst OR src	r	r	42	–	*	*	0	–	–	2	3
		r	Ir	43							2	4
		R	R	44							3	3
		R	IR	45							3	4
		R	IM	46							3	3
		IR	IM	47							3	4

Note: Flags Notation:
* = Value is a function of the result of the operation.
– = Unaffected.
X = Undefined.
0 = Reset to 0.
1 = Set to 1.

Table 129. Opcode Map Abbreviations

Abbreviation	Description	Abbreviation	Description
b	Bit position.	IRR	Indirect register pair.
cc	Condition code.	p	Polarity (0 or 1).
X	8-bit signed index or displacement.	r	4-bit working register.
DA	Destination address.	R	8-bit register.
ER	Extended addressing register.	r1, R1, Ir1, Irr1, IR1, rr1, RR1, IRR1, ER1	Destination address.
IM	Immediate data value.	r2, R2, Ir2, Irr2, IR2, rr2, RR2, IRR2, ER2	Source address.
Ir	Indirect working register.	RA	Relative.
IR	Indirect register.	rr	Working register pair.
Irr	Indirect working register pair.	RR	Register pair.

Table 132. Power Consumption (Continued)

		V_{DD} = 2.7 V to 3.6 V				
Symbol	**Parameter**	**Typical[1]**	**Maximum Std Temp[2]**	**Maximum Ext Temp[3]**	**Units**	**Conditions**
I_{DD} ADCRef	ADC Internal Reference Supply Current	0			µA	See Note 4.
I_{DD} CMP	Comparator supply Current	150	180	190	µA	See Note 4.
I_{DD} LPO	Low-Power Operational Amplifier Supply Current	3	5	5	µA	Driving a high-impedance load.
I_{DD} TS	Temperature Sensor Supply Current	60			µA	See Note 4.
I_{DD} BG	Band Gap Supply Current	320	480	500	µA	For 20-/28-pin devices.
						For 8-pin devices.

Notes:
1. Typical conditions are defined as V_{DD} = 3.3V and +30°C.
2. Standard temperature is defined as T_A = 0°C to +70°C; these values not tested in production for worst case behavior, but are derived from product characterization and provided for design guidance only.
3. Extended temperature is defined as T_A = –40°C to +105°C; these values not tested in production for worst case behavior, but are derived from product characterization and provided for design guidance only.
4. For this block to operate, the bandgap circuit is automatically turned on and must be added to the total supply current. This bandgap current is only added once, regardless of how many peripherals are using it.

On-Chip Peripheral AC and DC Electrical Characteristics

Table 135 tabulates the electrical characteristics of the POR and VBO blocks.

Table 135. Power-On Reset and Voltage Brown-Out Electrical Characteristics and Timing

		T_A = –40°C to +105°C				
Symbol	**Parameter**	**Minimum**	**Typical[1]**	**Maximum**	**Units**	**Conditions**
V_{POR}	Power-On Reset Voltage Threshold	2.20	2.45	2.70	V	$V_{DD} = V_{POR}$
V_{VBO}	Voltage Brown-Out Reset Voltage Threshold	2.15	2.40	2.65	V	$V_{DD} = V_{VBO}$
	V_{POR} to V_{VBO} hysteresis		50	75	mV	
	Starting V_{DD} voltage to ensure valid Power-On Reset.	–	V_{SS}	–	V	
T_{ANA}	Power-On Reset Analog Delay	–	70	–	µs	$V_{DD} > V_{POR}$; T_{POR} Digital Reset delay follows T_{ANA}
T_{POR}	Power-On Reset Digital Delay		16		µs	66 Internal Precision Oscillator cycles + IPO startup time (T_{IPOST})
T_{POR}	Power-On Reset Digital Delay		1		ms	5000 Internal Precision Oscillator cycles
T_{SMR}	Stop Mode Recovery with crystal oscillator disabled		16		µs	66 Internal Precision Oscillator cycles
T_{SMR}	Stop Mode Recovery with crystal oscillator enabled		1		ms	5000 Internal Precision Oscillator cycles
T_{VBO}	Voltage Brown-Out Pulse Rejection Period	–	10	–	µs	Period of time in which $V_{DD} < V_{VBO}$ without generating a Reset.

Note: Data in the typical column is from characterization at 3.3V and 30°C. These values are provided for design guidance only and are not tested in production.

Table 137. Watchdog Timer Electrical Characteristics and Timing

		V_{DD} = 2.7 V to 3.6 V T_A = –40°C to +105°C (unless otherwise stated)				
Symbol	**Parameter**	**Minimum**	**Typical**	**Maximum**	**Units**	**Conditions**
F_{WDT}	WDT Oscillator Frequency		10		kHz	
F_{WDT}	WDT Oscillator Error			±50	%	
T_{WDTCAL}	WDT Calibrated Time-out	0.98	1	1.02	s	V_{DD} = 3.3V; T_A = 30°C
		0.70	1	1.30	s	V_{DD} = 2.7 V to 3.6 V T_A = 0°C to 70°C
		0.50	1	1.50	s	V_{DD} = 2.7 V to 3.6 V T_A = –40°C to +105°C

Table 138. Non-Volatile Data Storage

	V_{DD} = 2.7 V to 3.6 V T_A = –40°C to +105°C				
Parameter	**Minimum**	**Typical**	**Maximum**	**Units**	**Notes**
NVDS Byte Read Time	34	–	519	µs	With system clock at 20 MHz
NVDS Byte Program Time	0.171	–	39.7	ms	With system clock at 20 MHz
Data Retention	100	–	–	years	25°C
Endurance	160,000	–	–	cycles	Cumulative write cycles for entire memory

Table 148. Z8 Encore! XP F082A Series Ordering Matrix

Part Number	Flash	RAM	NVDS	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description
Z8 Encore! XP F082A Series with 4 KB Flash, 10-Bit Analog-to-Digital Converter											
Standard Temperature: 0°C to 70°C											
Z8F042APB020SG	4 KB	1KB	128 B	6	14	2	4	1	1	1	PDIP 8-pin package
Z8F042AQB020SG	4 KB	1KB	128 B	6	14	2	4	1	1	1	QFN 8-pin package
Z8F042ASB020SG	4 KB	1KB	128 B	6	14	2	4	1	1	1	SOIC 8-pin package
Z8F042ASH020SG	4 KB	1KB	128 B	17	20	2	7	1	1	1	SOIC 20-pin package
Z8F042AHH020SG	4 KB	1KB	128 B	17	20	2	7	1	1	1	SSOP 20-pin package
Z8F042APH020SG	4 KB	1KB	128 B	17	20	2	7	1	1	1	PDIP 20-pin package
Z8F042ASJ020SG	4 KB	1KB	128 B	23	20	2	8	1	1	1	SOIC 28-pin package
Z8F042AHJ020SG	4 KB	1KB	128 B	23	20	2	8	1	1	1	SSOP 28-pin package
Z8F042APJ020SG	4 KB	1KB	128 B	23	20	2	8	1	1	1	PDIP 28-pin package
Extended Temperature: –40°C to 105°C											
Z8F042APB020EG	4 KB	1KB	128 B	6	14	2	4	1	1	1	PDIP 8-pin package
Z8F042AQB020EG	4 KB	1KB	128 B	6	14	2	4	1	1	1	QFN 8-pin package
Z8F042ASB020EG	4 KB	1KB	128 B	6	14	2	4	1	1	1	SOIC 8-pin package
Z8F042ASH020EG	4 KB	1KB	128 B	17	20	2	7	1	1	1	SOIC 20-pin package
Z8F042AHH020EG	4 KB	1KB	128 B	17	20	2	7	1	1	1	SSOP 20-pin package
Z8F042APH020EG	4 KB	1KB	128 B	17	20	2	7	1	1	1	PDIP 20-pin package
Z8F042ASJ020EG	4 KB	1KB	128 B	23	20	2	8	1	1	1	SOIC 28-pin package
Z8F042AHJ020EG	4 KB	1KB	128 B	23	20	2	8	1	1	1	SSOP 28-pin package
Z8F042APJ020EG	4 KB	1KB	128 B	23	20	2	8	1	1	1	PDIP 28-pin package

Table 148. Z8 Encore! XP F082A Series Ordering Matrix

Part Number	Flash	RAM	NVDS	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description
Z8 Encore! XP F082A Series with 1KB Flash, 10-Bit Analog-to-Digital Converter											
Standard Temperature: 0°C to 70°C											
Z8F012APB020SG	1KB	256 B	16 B	6	14	2	4	1	1	1	PDIP 8-pin package
Z8F012AQB020SG	1KB	256 B	16 B	6	14	2	4	1	1	1	QFN 8-pin package
Z8F012ASB020SG	1KB	256 B	16 B	6	14	2	4	1	1	1	SOIC 8-pin package
Z8F012ASH020SG	1KB	256 B	16 B	17	20	2	7	1	1	1	SOIC 20-pin package
Z8F012AHH020SG	1KB	256 B	16 B	17	20	2	7	1	1	1	SSOP 20-pin package
Z8F012APH020SG	1KB	256 B	16 B	17	20	2	7	1	1	1	PDIP 20-pin package
Z8F012ASJ020SG	1KB	256 B	16 B	23	20	2	8	1	1	1	SOIC 28-pin package
Z8F012AHJ020SG	1KB	256 B	16 B	23	20	2	8	1	1	1	SSOP 28-pin package
Z8F012APJ020SG	1KB	256 B	16 B	23	20	2	8	1	1	1	PDIP 28-pin package
Extended Temperature: –40°C to 105°C											
Z8F012APB020EG	1KB	256 B	16 B	6	14	2	4	1	1	1	PDIP 8-pin package
Z8F012AQB020EG	1KB	256 B	16 B	6	14	2	4	1	1	1	QFN 8-pin package
Z8F012ASB020EG	1KB	256 B	16 B	6	14	2	4	1	1	1	SOIC 8-pin package
Z8F012ASH020EG	1KB	256 B	16 B	17	20	2	7	1	1	1	SOIC 20-pin package
Z8F012AHH020EG	1KB	256 B	16 B	17	20	2	7	1	1	1	SSOP 20-pin package
Z8F012APH020EG	1KB	256 B	16 B	17	20	2	7	1	1	1	PDIP 20-pin package
Z8F012ASJ020EG	1KB	256 B	16 B	23	20	2	8	1	1	1	SOIC 28-pin package
Z8F012AHJ020EG	1KB	256 B	16 B	23	20	2	8	1	1	1	SSOP 28-pin package
Z8F012APJ020EG	1KB	256 B	16 B	23	20	2	8	1	1	1	PDIP 28-pin package