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Details

Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	6
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	64 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	8-VDFN Exposed Pad
Supplier Device Package	8-QFN (5x6)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f021aqb020eg

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Z8 Encore! XP[®] F082A Series Product Specification

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	Reset Characteristics and Latency							
Reset Type	Control Registers	eZ8 CPU	Reset Latency (Delay)					
System Reset	Reset (as applicable)	Reset	66 Internal Precision Oscillator Cycles					
System Reset with Crystal Oscillator Enabled	Reset (as applicable)	Reset	5000 Internal Precision Oscillator Cycles					
Stop Mode Recovery	Unaffected, except WDT_CTL and OSC_CTL registers	Reset	66 Internal Precision Oscillator Cycles + IPO startup time					
Stop Mode Recovery with Crystal Oscillator Enabled	Unaffected, except WDT_CTL and OSC_CTL registers	Reset	5000 Internal Precision Oscillator Cycles					

Table 8. Reset and Stop Mode Recovery Characteristics and Latency

During a System Reset or Stop Mode Recovery, the Internal Precision Oscillator requires 4 μ s to start up. Then the Z8 Encore! XP F082A Series device is held in Reset for 66 cycles of the Internal Precision Oscillator. If the crystal oscillator is enabled in the Flash option bits, this reset period is increased to 5000 IPO cycles. When a reset occurs because of a low voltage condition or Power-On Reset (POR), this delay is measured from the time that the supply voltage first exceeds the POR level. If the external pin reset remains asserted at the end of the reset period, the device remains in reset until the pin is deasserted.

At the beginning of Reset, all GPIO pins are configured as inputs with pull-up resistor disabled, except PD0 (or PA2 on 8-pin devices) which is shared with the reset pin. On reset, the PD0 is configured as a bidirectional open-drain reset. The pin is internally driven low during port reset, after which the user code may reconfigure this pin as a general purpose output.

During Reset, the eZ8 CPU and on-chip peripherals are idle; however, the on-chip crystal oscillator and Watchdog Timer oscillator continue to run.

Upon Reset, control registers within the Register File that have a defined Reset value are loaded with their reset values. Other control registers (including the Stack Pointer, Register Pointer and Flags) and general-purpose RAM are undefined following Reset. The eZ8 CPU fetches the Reset vector at Program Memory addresses 0002H and 0003H and loads that value into the Program Counter. Program execution begins at the Reset vector address.

As the control registers are reinitialized by a system reset, the system clock after reset is always the IPO. The software must reconfigure the oscillator control block, such that the correct system clock source is enabled and selected.

and as long as four. A reset pulse three clock cycles in duration might trigger a reset; a pulse four cycles in duration always triggers a reset.

While the RESET input pin is asserted Low, the Z8 Encore! XP F082A Series devices remain in the Reset state. If the RESET pin is held Low beyond the System Reset timeout, the device exits the Reset state on the system clock rising edge following RESET pin deassertion. Following a System Reset initiated by the external RESET pin, the EXT status bit in the Reset Status (RSTSTAT) Register is set to 1.

External Reset Indicator

During System Reset or when enabled by the GPIO logic (see <u>Table 20 on page 46</u>), the <u>RESET</u> pin functions as an open-drain (active Low) reset mode indicator in addition to the input functionality. This reset output feature allows a Z8 Encore! XP F082A Series device to reset other components to which it is connected, even if that reset is caused by internal sources such as POR, VBO or WDT events.

After an internal reset event occurs, the internal circuitry begins driving the RESET pin Low. The RESET pin is held Low by the internal circuitry until the appropriate delay listed in Table 8 has elapsed.

On-Chip Debugger Initiated Reset

A Power-On Reset can be initiated using the On-Chip Debugger by setting the RST bit in the OCD Control Register. The On-Chip Debugger block is not reset but the rest of the chip goes through a normal system reset. The RST bit automatically clears during the system reset. Following the system reset the POR bit in the Reset Status (RSTSTAT) Register is set.

Stop Mode Recovery

STOP Mode is entered by execution of a STOP instruction by the eZ8 CPU. See the <u>Low-Power Modes</u> chapter on page 32 for detailed STOP Mode information. During Stop Mode Recovery (SMR), the CPU is held in reset for 66 IPO cycles if the crystal oscillator is disabled or 5000 cycles if it is enabled. The SMR delay (see <u>Table 135</u> on page 233) T_{SMR} , also includes the time required to start up the IPO.

Stop Mode Recovery does not affect on-chip registers other than the Watchdog Timer Control Register (WDTCTL) and the Oscillator Control Register (OSCCTL). After any Stop Mode Recovery, the IPO is enabled and selected as the system clock. If another system clock source is required, the Stop Mode Recovery code must reconfigure the oscillator control block such that the correct system clock source is enabled and selected.

The eZ8 CPU fetches the Reset vector at Program Memory addresses 0002H and 0003H and loads that value into the Program Counter. Program execution begins at the Reset vec-

HALT Mode

Executing the eZ8 CPU's HALT instruction places the device into HALT Mode, which powers down the CPU but leaves all other peripherals active. In HALT Mode, the operating characteristics are:

- Primary oscillator is enabled and continues to operate
- System clock is enabled and continues to operate
- eZ8 CPU is stopped
- Program counter (PC) stops incrementing
- Watchdog Timer's internal RC oscillator continues to operate
- If enabled, the Watchdog Timer continues to operate
- All other on-chip peripherals continue to operate, if enabled

The eZ8 CPU can be brought out of HALT Mode by any of the following operations:

- Interrupt
- Watchdog Timer time-out (interrupt or reset)
- Power-On Reset
- Voltage Brown-Out reset
- External **RESET** pin assertion

To minimize current in HALT Mode, all GPIO pins that are configured as inputs must be driven to one of the supply rails (V_{CC} or GND).

Peripheral-Level Power Control

In addition to the STOP and HALT modes, it is possible to disable each peripheral on each of the Z8 Encore! XP F082A Series devices. Disabling a given peripheral minimizes its power consumption.

Power Control Register Definitions

The following sections define the Power Control registers.

Power Control Register 0

Each bit of the following registers disables a peripheral block, either by gating its system clock input or by removing power from the block. The default state of the low-power

Architecture

Figure 8 displays the interrupt controller block diagram.



Figure 8. Interrupt Controller Block Diagram

Operation

This section describes the operational aspects of the following functions.

Master Interrupt Enable: see page 57

Interrupt Vectors and Priority: see page 58

Interrupt Assertion: see page 58

Software Interrupt Assertion: see page 59

Watchdog Timer Interrupt Assertion: see page 59

Master Interrupt Enable

The master interrupt enable bit (IRQE) in the Interrupt Control Register globally enables and disables interrupts. Interrupts are globally enabled by any of the following actions:

- Execution of an EI (Enable Interrupt) instruction
- Execution of an IRET (Return from Interrupt) instruction



Figure 11. UART Asynchronous Data Format without Parity



Figure 12. UART Asynchronous Data Format with Parity

Transmitting Data using the Polled Method

Observe the following steps to transmit data using the polled method of operation:

- 1. Write to the UART Baud Rate High and Low Byte registers to set the required baud rate.
- 2. Enable the UART pin functions by configuring the associated GPIO port pins for alternate function operation.
- 3. Write to the UART Control 1 Register, if MULTIPROCESSOR Mode is appropriate, to enable MULTIPROCESSOR (9-bit) Mode functions.
- 4. Set the Multiprocessor Mode Select (MPEN) bit to enable MULTIPROCESSOR Mode.
- 5. Write to the UART Control 0 Register to:
 - Set the transmit enable bit (TEN) to enable the UART for data transmission
 - Set the parity enable bit (PEN), if parity is appropriate and MULTIPROCESSOR Mode is not enabled and select either even or odd parity (PSEL)

ADC Control Register 0

The ADC Control Register 0 (ADCCTL0) selects the analog input channel and initiates the analog-to-digital conversion. It also selects the voltage reference configuration.

Bit	7	6	5	4	3	2	1	0				
Field	CEN	REFSELL	REFOUT	CONT		ANAI	N[3:0]					
RESET	0	0	0	0	0	0	0					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				
Address				F7	он	I		1				
Bit	Descrip	Description										
[7] CEN	Convers 0 = Conv this I 1 = Begin prog	 Conversion Enable 0 = Conversion is complete. Writing a 0 produces no effect. The ADC automatically clears this bit to 0 when a conversion is complete. 1 = Begin conversion. Writing a 1 to this bit starts a conversion. If a conversion is already in progress, the conversion restarts. This bit remains 1 until the conversion is complete. 										
[6] REFSELL	Voltage Reference Level Select Low Bit In conjunction with the High bit (REFSELH) in ADC Control/Status Register 1, this deter- mines the level of the internal voltage reference; the following details the effects of {REF- SELH, REFSELL}; note that this reference is independent of the Comparator reference. 00 = Internal Reference Disabled, reference comes from external pin. 01 = Internal Reference set to 1.0 V. 10 = Internal Reference set to 2.0 V (default).											
[5] REFOUT	Internal 0 = Refe 1 = The Caution the REF	Reference rence buffer internal ADC : When the OUT bit mus	Output Ena is disabled; reference i ADC is usec at be set to 0	ble Vref pin is a s buffered a l with an ext).	available for nd driven ou ernal referei	GPIO or ar ut to the V _{RE} nce ({REFS	alog functio _{EF} pin. ELH,REFSE	ns. ELL}=00),				
[4] CONT	Convers 0 = Singl cycle 1 = Cont 5129 long	 Conversion 0 = Single-shot conversion. ADC data is output once at completion of the 5129 system clock cycles (measurements of the internal temperature sensor take twice as long). 1 = Continuous conversion. ADC data updated every 256 system clock cycles after an initial 5129 clock conversion (measurements of the internal temperature sensor take twice as long). 										
[3:0] ANAIN[3:0]	Analog Input Select These bits select the analog input for conversion. Not all Port pins in this list are available in all packages for the Z8 Encore! XP F082A Series. For information about port pins available with each package style, see the <u>Pin Description</u> chapter on page 8. Do not enable unavail- able analog inputs. Usage of these bits changes depending on the buffer mode selected in ADC Control/Status Register 1.											

Table 73. ADC Control Register 0 (ADCCTL0)

Bit	Description (Continued)
[2:1]	Reserved
	These bits are reserved and must be undefined.
[0]	Overflow Status
OVF	0 = A hardware overflow did not occur in the ADC for the current sample.
	1= A hardware overflow did occur in the ADC for the current sample, therefore the current
	sample is invalid.

8KB Flash		4KB Flash					
Program Memor	ry	Program Memo	ry	2KB Flash			
Addresses (hex)			Addresses (hex)	Addresses (he			
Sector 7	1C00	Sector 7	0E00	Sector 3	07FF		
Sector 6	1BFF	Sector 6	0DFF	Sector 2)400		
	1800 17FF		0C00 0BFF	Sector 1)200		
Sector 5	1400	Sector 5	0A00	Sector 0)1FF		
Sector 4	13FF 1000	Sector 4	09FF 0800	(1000		
Sector 3	0FFF 0C00	Sector 3	07FF 0600	1 KB Flash Program Memory Addresse	s (hex)		
Sector 2	0BFF 0800	Sector 2	05FF 0400	Sector 1	03FF		
Sector 1	07FF 0400	Sector 1	03FF 0200	Sector 0	01FF		
Sector 0	03FF 0000	Sector 0	01FF 0000				

Figure 21. Flash Memory Arrangement

Flash Information Area

The Flash information area is separate from Program Memory and is mapped to the address range FE00H to FFFFH. This area is readable but cannot be erased or overwritten. Factory trim values for the analog peripherals are stored here. Factory calibration data for the ADC is also stored here.

Operation

The Flash Controller programs and erases Flash memory. The Flash Controller provides the proper Flash controls and timing for Byte Programming, Page Erase and Mass Erase of Flash memory.

The Flash Controller contains several protection mechanisms to prevent accidental programming or erasure. These mechanism operate on the page, sector and full-memory levels.

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Table 79. Flash Code Protection Using the Flash Option Bits

FWP	Flash Code Protection Description
0	Programming and erasing disabled for all of Flash Program Mem-
	ory. In user code programming, Page Erase and Mass Erase are all
	disabled. Mass Erase is available through the On-Chip Debugger.
1	Programming, Page Erase and Mass Erase are enabled for all of
	Flash Program Memory.

Flash Code Protection Using the Flash Controller

At Reset, the Flash Controller locks to prevent accidental program or erasure of the Flash memory. To program or erase the Flash memory, first write the Page Select Register with the target page. Unlock the Flash Controller by making two consecutive writes to the Flash Control Register with the values 73H and 8CH, sequentially. The Page Select Register must be rewritten with the target page. If the two Page Select writes do not match, the controller reverts to a locked state. If the two writes match, the selected page becomes active. See Figure 22 on page 148 for details.

After unlocking a specific page, you can enable either Page Program or Erase. Writing the value 95H causes a Page Erase only if the active page resides in a sector that is not protected. Any other value written to the Flash Control Register locks the Flash Controller. Mass Erase is not allowed in the user code but only in through the Debug Port.

After unlocking a specific page, you can also write to any byte on that page. After a byte is written, the page remains unlocked, allowing for subsequent writes to other bytes on the same page. Further writes to the Flash Control Register cause the active page to revert to a locked state.

Sector-Based Flash Protection

The final protection mechanism is implemented on a per-sector basis. The Flash memories of Z8 Encore! XP devices are divided into maximum number of 8 sectors. A sector is 1/8 of the total Flash memory size unless this value is smaller than the page size – in which case, the sector and page sizes are equal. On Z8 Encore! F082A Series devices, the sector size is varied according to the Flash memory configuration shown in <u>Table 78</u> on page 146.

The Flash Sector Protect Register can be configured to prevent sectors from being programmed or erased. After a sector is protected, it cannot be unprotected by user code. The Flash Sector Protect Register is cleared after reset, and any previously-written protection values are lost. User code must write this register in their initialization routine if they prefer to enable sector protection.

The Flash Sector Protect Register shares its Register File address with the Page Select Register. The Flash Sector Protect Register is accessed by writing the Flash Control Regis-

Option Bit Types

This section describes the five types of Flash option bits.

User Option Bits

The user option bits are contained in the first two bytes of program memory. User access to these bits has been provided because these locations contain application-specific device configurations. The information contained here is lost when page 0 of the program memory is erased.

Trim Option Bits

The trim option bits are contained in the information page of the Flash memory. These bits are factory programmed values required to optimize the operation of onboard analog circuitry and cannot be permanently altered. Program Memory may be erased without endangering these values. It is possible to alter working values of these bits by accessing the Trim Bit Address and Data registers, but these working values are lost after a power loss or any other reset event.

There are 32 bytes of trim data. To modify one of these values the user code must first write a value between 00H and 1FH into the Trim Bit Address Register. The next write to the Trim Bit Data Register changes the working value of the target trim data byte.

Reading the trim data requires the user code to write a value between 00H and 1FH into the Trim Bit Address Register. The next read from the Trim Bit Data Register returns the working value of the target trim data byte.

• Note: The trim address range is from information address 20–3F only. The remainder of the information page is not accessible through the trim bit address and data registers.

Calibration Option Bits

The calibration option bits are also contained in the information page. These bits are factory-programmed values intended for use in software correcting the device's analog performance. To read these values, the user code must employ the LDC instruction to access the information area of the address space as defined in See the <u>Flash Information Area</u> section on page 17.

Serialization Bits

As an optional feature, Zilog is able to provide factory-programmed serialization. For serialized products, the individual devices are programmed with unique serial numbers. These serial numbers are binary values, four bytes in length. The numbers increase in size with each device, but gaps in the serial sequence may exist.

Info Page Address	Memory Address	Compensation Usage	ADC Mode	Reference Type
12	FE12	Positive Gain High Byte	Differential Unbuffered	Internal 2.0 V
13	FE13	Positive Gain Low Byte	Differential Unbuffered	Internal 2.0 V
30	FE30	Negative Gain High Byte	Differential Unbuffered	Internal 2.0 V
31	FE31	Negative Gain Low Byte	Differential Unbuffered	Internal 2.0 V
72	FE72	Offset	Differential Unbuffered	Internal 1.0 V
14	FE14	Positive Gain High Byte	Differential Unbuffered	Internal 1.0 V
15	FE15	Positive Gain Low Byte	Differential Unbuffered	Internal 1.0 V
32	FE32	Negative Gain High Byte	Differential Unbuffered	Internal 1.0 V
33	FE33	Negative Gain Low Byte	Differential Unbuffered	Internal 1.0 V
75	FE75	Offset	Differential Unbuffered	External 2.0 V
16	FE16	Positive Gain High Byte	Differential Unbuffered	External 2.0 V
17	FE17	Positive Gain Low Byte	Differential Unbuffered	External 2.0 V
34	FE34	Negative Gain High Byte	Differential Unbuffered	External 2.0 V
35	FE35	Negative Gain Low Byte	Differential Unbuffered	External 2.0 V
78	FE78	Offset	Differential 1x Buffered	Internal 2.0 V
18	FE18	Positive Gain High Byte	Differential 1x Buffered	Internal 2.0 V
19	FE19	Positive Gain Low Byte	Differential 1x Buffered	Internal 2.0 V
36	FE36	Negative Gain High Byte	Differential 1x Buffered	Internal 2.0 V
37	FE37	Negative Gain Low Byte	Differential 1x Buffered	Internal 2.0 V
7B	FE7B	Offset	Differential 1x Buffered	External 2.0 V
1A	FE1A	Positive Gain High Byte	Differential 1x Buffered	External 2.0 V
1B	FE1B	Positive Gain Low Byte	Differential 1x Buffered	External 2.0 V
38	FE38	Negative Gain High Byte	Differential 1x Buffered	External 2.0 V
39	FE39	Negative Gain Low Byte	Differential 1x Buffered	External 2.0 V

Table 97. ADC Calibration Data Location (Continued)

Register file size varies depending on the device type. See the device-specific Z8 Encore! XP Product Specification to determine the exact register file range available.

eZ8 CPU Instruction Notation

In the eZ8 CPU Instruction Summary and Description sections, the operands, condition codes, status flags and address modes are represented by a notational shorthand that is described in Table 118.

Notation	Description	Operand	Range
b	Bit	b	b represents a value from 0 to 7 (000B to 111B).
CC	Condition code	—	Refer to the Condition Codes section in the <u>eZ8</u> <u>CPU Core User Manual (UM0128)</u> .
DA	Direct address	Addrs	Represents a number in the range 0000H to FFFFH.
ER	Extended addressing register	Reg	Reg. represents a number in the range of 000H to FFFH.
IM	Immediate data	#Data	Data is a number between 00H to FFH.
lr	Indirect working register	@Rn	n = 0–15.
IR	Indirect register	@Reg	Reg. represents a number in the range of 00H to FFH.
Irr	Indirect working register pair	@RRp	p = 0, 2, 4, 6, 8, 10, 12, or 14.
IRR	Indirect register pair	@Reg	Reg. represents an even number in the range 00H to FEH.
р	Polarity	р	Polarity is a single bit binary value of either 0B or 1B.
r	Working register	Rn	n = 0 - 15.
R	Register	Reg	Reg. represents a number in the range of 00H to FFH.
RA	Relative address	Х	X represents an index in the range of +127 to – 128 which is an offset relative to the address of the next instruction.
rr	Working register pair	RRp	p = 0, 2, 4, 6, 8, 10, 12, or 14.
RR	Register pair	Reg	Reg. represents an even number in the range of 00H to FEH.

Table 118. Notational Shorthand

Assembly		Add Mo	lress ode	Oncode(s)			Fla	ags			Fetch	Instr.
Mnemonic	Symbolic Operation	dst	src	(Hex)	С	Ζ	S	۷	D	Н	S	S
JR dst	$PC \gets PC + X$	DA		8B	_	-	-	-	-	_	2	2
JR cc, dst	if cc is true PC \leftarrow PC + X	DA		0B-FB	_	_	_	_	_	_	2	2
LD dst, rc	dst \leftarrow src	r	IM	0C-FC	_	_	_	_	_	_	2	2
		r	X(r)	C7	-						3	3
		X(r)	r	D7	-						3	4
		r	lr	E3	-						2	3
		R	R	E4	-						3	2
		R	IR	E5	_						3	4
		R	IM	E6	-						3	2
		IR	IM	E7	_						3	3
		Ir	r	F3	_						2	3
		IR	R	F5	_						3	3
LDC dst, src	dst \leftarrow src	r	Irr	C2	_	_	_	_	_	_	2	5
		Ir	Irr	C5	_						2	9
		Irr	r	D2	_						2	5
LDCI dst, src	dst \leftarrow src	Ir	Irr	C3	_	_	_	_	_	_	2	9
	r ← r + 1 rr ← rr + 1	Irr	lr	D3	-						2	9
LDE dst, src	dst \leftarrow src	r	Irr	82	_	_	_	_	_	_	2	5
		Irr	r	92	-						2	5
LDEI dst, src	dst \leftarrow src	lr	Irr	83	_	_	_	_	_	_	2	9
	r ← r + 1 rr ← rr + 1	Irr	lr	93	-						2	9
I DWX dst_src	dst ← src	FR	FR	1FF8	_	_	_	_	_	_	5	4

Table 128. eZ8 CPU Instruction Summary (Continued)

Note: Flags Notation:

* = Value is a function of the result of the operation.

- = Unaffected.

X = Undefined.

0 = Reset to 0.

1 =Set to 1.

				-	•			-				
Assembly	_	Add Mo	lress ode	_ Opcode(s)			Fla	ags			Fetch Cycle	Instr. Cvcle
Mnemonic	Symbolic Operation	dst	src	(Hex)	С	Ζ	S	۷	D	Н	s	s
RRC dst	「	R		C0	*	*	*	*	-	-	2	2
	► <u>D7D6D5D4D3D2D1D0</u> ►_C dst	IR		C1	-						2	3
SBC dst, src	$dst \leftarrow dst - src - C$	r	r	32	*	*	*	*	1	*	2	3
	-	r	lr	33							2	4
	-	R	R	34							3	3
	-	R	IR	35	-						3	4
	-	R	IM	36	-						3	3
	-	IR	IM	37							3	4
SBCX dst, src	$dst \leftarrow dst - src - C$	ER	ER	38	*	*	*	*	1	*	4	3
	-	ER	IM	39	-						4	3
SCF	C ← 1			DF	1	-	-	-	-	-	1	2
SRA dst		R		D0	*	*	*	0	-	-	2	2
	D7D6D5D4D3D2D1D0	IR		D1	-						2	3
SRL dst	0 - ► D7 D6 D5 D4 D3 D2 D1 D0 ► C	R		1F C0	*	*	0	*	_	_	3	2
	dst	IR		1F C1							3	3
SRP src	$RP \leftarrow src$		IM	01	_	_	_	_	_	_	2	2
STOP	STOP Mode			6F	_	-	_	_	_	-	1	2
Note: Flags Nota * = Value is a fund - = Unaffected.	ation: ction of the result of the oper	ation.										

Table 128. eZ8 CPU Instruction Summary (Continued)

X = Undefined.

0 = Reset to 0.

1 = Set to 1.

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Opcode Maps

A description of the opcode map data and the abbreviations are provided in Figure 30. Figures 31 and 32 display the eZ8 CPU instructions. Table 129 lists Opcode Map abbreviations.



Figure 30. Opcode Map Cell Description

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AC Characteristics

The section provides information about the AC characteristics and timing. All AC timing information assumes a standard load of 50pF on all outputs.

		V _{DD} = 2.7 T _A = -40°C (unless c sta	℃ to 3.6V to +105°C otherwise ted)		
Symbol	Parameter	Minimum	Maximum	Units	Conditions
F _{SYSCLK}	System Clock Frequency	-	20.0	MHz	Read-only from Flash mem- ory
		0.032768	20.0	MHz	Program or erasure of the Flash memory
F _{XTAL}	Crystal Oscillator Frequency	-	20.0	MHz	System clock frequencies below the crystal oscillator minimum require an exter- nal clock driver
T _{XIN}	System Clock Period	50	-	ns	T _{CLK} = 1/F _{sysclk}
T _{XINH}	System Clock High Time	20	30	ns	T _{CLK} = 50 ns
T _{XINL}	System Clock Low Time	20	30	ns	T _{CLK} = 50 ns
T _{XINR}	System Clock Rise Time	-	3	ns	T _{CLK} = 50 ns
T _{XINF}	System Clock Fall Time	_	3	ns	T _{CLK} = 50 ns

|--|

Table 134. Internal Precision Oscillator Electrical Characteristics

		V _{DD} T _A = - (unless	= 2.7V to 3 -40°C to +7 otherwise			
Symbol	Parameter	Minimum	Typical	Maximum	Units	Conditions
F _{IPO}	Internal Precision Oscillator Fre- quency (High Speed)		5.53		MHz	V _{DD} = 3.3V T _A = 30°C
F _{IPO}	Internal Precision Oscillator Fre- quency (Low Speed)		32.7		kHz	V _{DD} = 3.3V T _A = 30°C
F _{IPO}	Internal Precision Oscillator Error		<u>+</u> 1	<u>+</u> 4	%	
T _{IPOST}	Internal Precision Oscillator Startup Time		3		μs	

On-Chip Peripheral AC and DC Electrical Characteristics

Table 135 tabulates the electrical characteristics of the POR and VBO blocks.

Table 135. Power-On Reset and Voltage Brown-Out Electrical Characteristics and Timing

		T _A =				
Symbol	Parameter	Minimum	Typical ¹	Maximum	Units	Conditions
V _{POR}	Power-On Reset Voltage Thresh- old	2.20	2.45	2.70	V	$V_{DD} = V_{POR}$
V_{VBO}	Voltage Brown-Out Reset Voltage Threshold	2.15	2.40	2.65	V	$V_{DD} = V_{VBO}$
	V _{POR} to V _{VBO} hysteresis		50	75	mV	
	Starting V _{DD} voltage to ensure valid Power-On Reset.	-	V _{SS}	_	V	
T _{ANA}	Power-On Reset Analog Delay	-	70	-	μs	V _{DD} > V _{POR} ; T _{POR} Digital Reset delay follows T _{ANA}
T _{POR}	Power-On Reset Digital Delay		16		μs	66 Internal Precision Oscillator cycles + IPO startup time (T _{IPOST})
T _{POR}	Power-On Reset Digital Delay		1		ms	5000 Internal Precision Oscillator cycles
T _{SMR}	Stop Mode Recovery with crystal oscillator disabled		16		μs	66 Internal Precision Oscillator cycles
T _{SMR}	Stop Mode Recovery with crystal oscillator enabled		1		ms	5000 Internal Precision Oscillator cycles
T _{VBO}	Voltage Brown-Out Pulse Rejec- tion Period	_	10	_	μs	Period of time in which $V_{DD} < V_{VBO}$ without generating a Reset.

Note: Data in the typical column is from characterization at 3.3 V and 30°C. These values are provided for design guidance only and are not tested in production.

		V _{DD} T _A : (unless	= 3.0 V to = 0°C to +7 otherwise	3.6 V 70°C e stated)			
Symbol	Parameter	Minimum	Typical	Maximum	Units	Conditions	
	Resolution	10		_	bits		
	Differential Nonlinearity (DNL)	-1.0	_	1.0	LSB ³	External V _{REF} = 2.0 V; R _S \leftarrow 3.0 k Ω	
	Integral Nonlinearity (INL)	-3.0	-	3.0	LSB ³	External V _{REF} = 2.0 V; R _S \leftarrow 3.0 k Ω	
	Offset Error with Calibra- tion		<u>+</u> 1		LSB ³		
	Absolute Accuracy with Calibration		<u>+</u> 3		LSB ³		
V _{REF}	Internal Reference Volt- age	1.0 2.0	1.1 2.2	1.2 2.4	V	REFSEL=01 REFSEL=10	
V _{REF}	Internal Reference Varia- tion with Temperature		<u>+</u> 1.0		%	Temperature variation with $V_{DD} = 3.0$	
V _{REF}	Internal Reference Volt- age Variation with V _{DD}		<u>+</u> 0.5		%	Supply voltage varia- tion with $T_A = 30^{\circ}C$	
R _{RE-} FOUT	Reference Buffer Output Impedance		850		W	When the internal ref- erence is buffered and driven out to the VREF pin (REFOUT = 1)	
	Single-Shot Conversion Time	-	5129	_	Sys- tem clock cycles	All measurements but temperature sensor	
			10258			Temperature sensor measurement	

Table 139. Analog-to-Digital Converter Electrical Characteristics and Timing

Notes:

1. Analog source impedance affects the ADC offset voltage (because of pin leakage) and input settling time.

2. Devices are factory calibrated at V_{DD} = 3.3V and T_A = +30°C, so the ADC is maximally accurate under these conditions.

3. LSBs are defined assuming 10-bit resolution.

4. This is the maximum recommended resistance seen by the ADC input pin.

5. The input impedance is inversely proportional to the system clock frequency.

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General Purpose I/O Port Input Data Sample Timing

Figure 34 displays timing of the GPIO Port input sampling. The input value on a GPIO port pin is sampled on the rising edge of the system clock. The Port value is available to the eZ8 CPU on the second rising clock edge following the change of the Port value.



Figure 34. Port Input Sample Timing

Table 143. GPIO Port Input Timing

		Delay (ns)	
Parameter	Abbreviation	Minimum	Maximum
T _{S_PORT}	Port Input Transition to X _{IN} Rise Setup Time (not pictured)	5	-
T _{H_PORT}	X _{IN} Rise to Port Input Transition Hold Time (not pictured)	0	-
T _{SMR}	GPIO Port Pin Pulse Width to ensure Stop Mode Recovery (for GPIO port pins enabled as SMR sources)	1 μs	