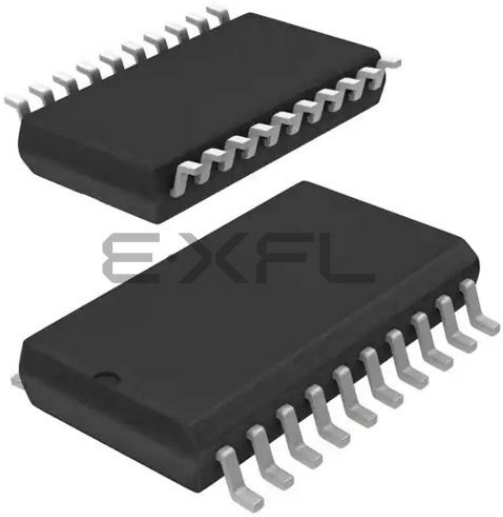
# Zilog - Z8F021ASH020EG Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | eZ8 |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | IrDA, UART/USART |
| Peripherals | Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT |
| Number of I/O | 17 |
| Program Memory Size | 2KB (2K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 64 x 8 |
| RAM Size | 512 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-SOIC (0.295", 7.50mm Width) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z8f021ash020eg |

**Table 2. Signal Descriptions (Continued)**

| Signal Mnemonic | I/O | Description |
|---|---|---|
| **Reset** | | |
| $\overline{\text{RESET}}$ | I/O | RESET. Generates a Reset when asserted (driven Low). Also serves as a reset indicator; the Z8 Encore! XP forces this pin low when in reset. This pin is open-drain and features an enabled internal pull-up resistor. |
| **Power Supply** | | |
| $V_{DD}$ | I | Digital Power Supply. |
| $AV_{DD}$ | I | Analog Power Supply. |
| $V_{SS}$ | I | Digital Ground. |
| $AV_{SS}$ | I | Analog Ground. |

Notes:
1. PB6 and PB7 are only available in 28-pin packages without ADC. In 28-pin packages with ADC, they are replaced by $AV_{DD}$ and $AV_{SS}$.
2. The $AV_{DD}$ and $AV_{SS}$ signals are available only in 28-pin packages with ADC. They are replaced by PB6 and PB7 on 28-pin packages without ADC.

# Pin Characteristics

Table 3 describes the characteristics for each pin available on the Z8 Encore! XP F082A Series 20- and 28-pin devices. Data in Table 3 is sorted alphabetically by the pin symbol mnemonic.

Table 4 on page 14 provides detailed information about the characteristics for each pin available on the Z8 Encore! XP F082A Series 8-pin devices.

**Note:** All six I/O pins on the 8-pin packages are 5 V-tolerant (unless the pull-up devices are enabled). The column in Table 3 below describes 5 V-tolerance for the 20- and 28-pin packages only.

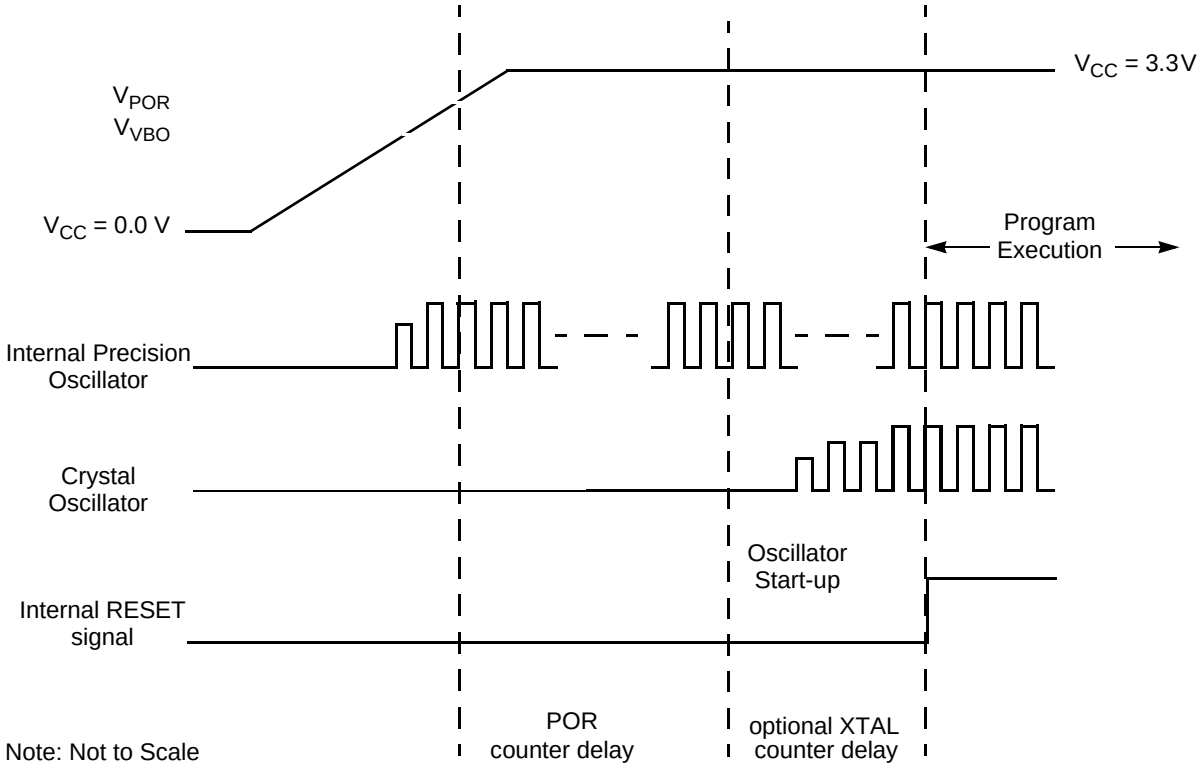


**Figure 5. Power-On Reset Operation**

## Voltage Brown-Out Reset

The devices in the Z8 Encore! XP F082A Series provide low Voltage Brown-Out (VBO) protection. The VBO circuit senses when the supply voltage drops to an unsafe level (below the VBO threshold voltage) and forces the device into the Reset state. While the supply voltage remains below the Power-On Reset voltage threshold ($V_{POR}$), the VBO block holds the device in the Reset.

After the supply voltage again exceeds the Power-On Reset voltage threshold, the device progresses through a full System Reset sequence, as described in the Power-On Reset section. Following Power-On Reset, the POR status bit in the Reset Status (RSTSTAT) Register is set to 1. Figure 6 displays Voltage Brown-Out operation. See the Electrical Characteristics chapter on page 226 for the VBO and POR threshold voltages ($V_{VBO}$ and $V_{POR}$).

The Voltage Brown-Out circuit can be either enabled or disabled during STOP Mode. Operation during STOP Mode is set by the VBO_AO Flash option bit. See the Flash Option Bits chapter on page 159 for information about configuring VBO_AO.

## Port A–D Control Registers

The Port A–D Control registers set the GPIO port operation. The value in the corresponding Port A–D Address Register determines which subregister is read from or written to by a Port A–D Control Register transaction; see Table 20.

**Table 20. Port A–D Control Registers (PxCTL)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | PCTL | | | | | | | |
| RESET | 00H | | | | | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FD1H, FD5H, FD9H, FDDH | | | | | | | |

| Bit | Description |
|---|---|
| [7:0]<br>PCTLx | **Port Control**<br>The Port Control Register provides access to all subregisters that configure the GPIO port operation. |

Note: x indicates the specific GPIO port pin number (7–0).

## Port A–D Data Direction Subregisters

The Port A–D Data Direction subregister is accessed through the Port A–D Control Register by writing 01H to the Port A–D Address Register; see Table 21.

**Table 21. Port A–D Data Direction Subregisters (PxDD)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | DD7 | DD6 | DD5 | DD4 | DD3 | DD2 | DD1 | DD0 |
| RESET | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | If 01H in Port A–D Address Register, accessible through the Port A–D Control Register | | | | | | | |

| Bit | Description |
|---|---|
| [7:0]<br>DDx | **Data Direction**<br>These bits control the direction of the associated port pin. Port Alternate Function operation overrides the Data Direction Register setting.<br>0 = Output. Data in the Port A–D Output Data Register is driven onto the port pin.<br>1 = Input. The port pin is sampled and the value written into the Port A–D Input Data Register. The output driver is tristated. |

Note: x indicates the specific GPIO port pin number (7–0).

## Port A–C Input Data Registers

Reading from the Port A–C Input Data registers, shown in Table 29, return the sampled values from the corresponding port pins. The Port A–C Input Data registers are read-only. The value returned for any unused ports is 0. Unused ports include those missing on the 8- and 28-pin packages, as well as those missing on the ADC-enabled 28-pin packages.

**Table 29. Port A–C Input Data Registers (PxIN)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | PIN7 | PIN6 | PIN5 | PIN4 | PIN3 | PIN2 | PIN1 | PIN0 |
| RESET | X | X | X | X | X | X | X | X |
| R/W | R | R | R | R | R | R | R | R |
| Address | FD2H, FD6H, FDAH | | | | | | | |

X = Undefined.

| Bit | Description |
|---|---|
| [7:0] PxIN | **Port Input Data**<br>Sampled data from the corresponding port pin input.<br>0 = Input data is logical 0 (Low).<br>1 = Input data is logical 1 (High). |

Note: x indicates the specific GPIO port pin number (7–0).

## Port A–D Output Data Register

The Port A–D Output Data Register, shown in Table 30, controls the output data to the pins.

**Table 30. Port A–D Output Data Register (P*x*OUT)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | POUT7 | POUT6 | POUT5 | POUT4 | POUT3 | POUT2 | POUT1 | POUT0 |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FD3H, FD7H, FDBH, FDFH | | | | | | | |

| Bit | Description |
|---|---|
| [7:0] PxOUT | **Port Output Data**<br>These bits contain the data to be driven to the port pins. The values are only driven if the corresponding pin is configured as an output and the pin is not configured for alternate function operation.<br>0 = Drive a logical 0 (Low).<br>1 = Drive a logical 1 (High). High value is not driven if the drain has been disabled by setting the corresponding Port Output Control Register bit to 1. |

Note: x indicates the specific GPIO port pin number (7–0).

## Interrupt Request 2 Register

The Interrupt Request 2 (IRQ2) Register, shown in Table 37, stores interrupt requests for both vectored and polled interrupts. When a request is presented to the interrupt controller, the corresponding bit in the IRQ2 Register becomes 1. If interrupts are globally enabled (vectored interrupts), the interrupt controller passes an interrupt request to the eZ8 CPU. If interrupts are globally disabled (polled interrupts), the eZ8 CPU can read the Interrupt Request 2 Register to determine if any interrupt requests are pending.

**Table 37. Interrupt Request 2 Register (IRQ2)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | Reserved | | | | PC3I | PC2I | PC1I | PC0I |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FC6H | | | | | | | |

| Bit | Description |
|---|---|
| [7:4] | **Reserved**<br>These bits are reserved and must be programmed to 0000. |
| [3:0]<br>PCxI | **Port C Pin *x* Interrupt Request**<br>0 = No interrupt request is pending for GPIO Port C pin *x*.<br>1 = An interrupt request from GPIO Port C pin *x* is awaiting service. |

Note: x indicates the specific GPIO Port C pin number (0–3).

## IRQ0 Enable High and Low Bit Registers

Table 38 describes the priority control for IRQ0. The IRQ0 Enable High and Low Bit registers, shown in Tables 39 and 40, form a priority-encoded enabling for interrupts in the Interrupt Request 0 Register.

**Table 38. IRQ0 Enable and Priority Encoding**

| IRQ0ENH[*x*] | IRQ0ENL[*x*] | Priority | Description |
|---|---|---|---|
| 0 | 0 | Disabled | Disabled |
| 0 | 1 | Level 1 | Low |
| 1 | 0 | Level 2 | Medium |
| 1 | 1 | Level 3 | High |

Note: x indicates register bits 0–7.

## Interrupt Control Register

The Interrupt Control (IRQCTL) Register, shown in Table 49, contains the master enable bit for all interrupts.

**Table 49. Interrupt Control Register (IRQCTL)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | IRQE | Reserved | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R | R | R | R | R | R | R |
| Address | FCFH | | | | | | | |

| Bit | Description |
|---|---|
| [7]<br>IRQE | **Interrupt Request Enable**<br>This bit is set to 1 by executing an EI (Enable Interrupts) or IRET (Interrupt Return) instruction, or by a direct register write of a 1 to this bit. It is reset to 0 by executing a DI instruction, eZ8 CPU acknowledgement of an interrupt request, Reset or by a direct register write of a 0 to this bit.<br>0 = Interrupts are disabled.<br>1 = Interrupts are enabled. |
| [6:0] | **Reserved**<br>These bits are reserved and must be programmed to 0000000. |

delay ensures a time gap between the deassertion of one PWM output to the assertion of its complement.

Observe the following steps for configuring a timer for PWM DUAL OUTPUT Mode and initiating the PWM operation:

1. Write to the Timer Control Register to:
   - Disable the timer
   - Configure the timer for PWM DUAL OUTPUT Mode by writing the TMODE bits in the TxCTL1 Register and the TMODEHI bit in TxCTL0 Register
   - Set the prescale value
   - Set the initial logic level (High or Low) and PWM High/Low transition for the Timer Output alternate function
2. Write to the Timer High and Low Byte registers to set the starting count value (typically `0001H`). This only affects the first pass in PWM mode. After the first timer reset in PWM mode, counting always begins at the reset value of `0001H`.
3. Write to the PWM High and Low Byte registers to set the PWM value.
4. Write to the PWM Control Register to set the PWM dead band delay value. The dead-band delay must be less than the duration of the positive phase of the PWM signal (as defined by the PWM high and low byte registers). It must also be less than the duration of the negative phase of the PWM signal (as defined by the difference between the PWM registers and the Timer Reload registers).
5. Write to the Timer Reload High and Low Byte registers to set the reload value (PWM period). The reload value must be greater than the PWM value.
6. If appropriate, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
7. Configure the associated GPIO port pin for the Timer Output and Timer Output Complement alternate functions. The Timer Output Complement function is shared with the Timer Input function for both timers. Setting the timer mode to Dual PWM automatically switches the function from Timer In to Timer Out Complement.
8. Write to the Timer Control Register to enable the timer and initiate counting.

The PWM period is represented by the following equation:

$$\text{PWM Period (s)} = \frac{\text{Reload Value} \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

If an initial starting value other than `0001H` is loaded into the Timer High and Low Byte registers, the ONE-SHOT Mode equation determines the first PWM time-out period.

# Watchdog Timer

The Watchdog Timer (WDT) protects against corrupt or unreliable software, power faults and other system-level problems which may place the Z8 Encore! XP F082A Series devices into unsuitable operating states. The features of Watchdog Timer include:

- On-chip RC oscillator
- A selectable time-out response: reset or interrupt
- 24-bit programmable time-out value

## Operation

The Watchdog Timer is a one-shot timer that resets or interrupts the Z8 Encore! XP F082A Series devices when the WDT reaches its terminal count. The Watchdog Timer uses a dedicated on-chip RC oscillator as its clock source. The Watchdog Timer operates in only two modes: ON and OFF. Once enabled, it always counts and must be refreshed to prevent a time-out. Perform an enable by executing the WDT instruction or by setting the WDT_AO Flash option bit. The WDT_AO bit forces the Watchdog Timer to operate immediately upon reset, even if a WDT instruction has not been executed.

The Watchdog Timer is a 24-bit reloadable downcounter that uses three 8-bit registers in the eZ8 CPU register space to set the reload value. The nominal WDT time-out period is described by the following equation:

$$\text{WDT Time-out Period (ms)} = \frac{\text{WDT Reload Value}}{10}$$

where the WDT reload value is the decimal value of the 24-bit value given by {WDTU[7:0], WDTH[7:0], WDTL[7:0]} and the typical Watchdog Timer RC oscillator frequency is 10kHz. The Watchdog Timer cannot be refreshed after it reaches 000002H. The WDT reload value must not be set to values below 000004H. Table 58 provides information about approximate time-out delays for the minimum and maximum WDT reload values.

**Table 58. Watchdog Timer Approximate Time-Out Delays**

| WDT Reload Value (Hex) | WDT Reload Value (Decimal) | Approximate Time-Out Delay (with 10kHz typical WDT oscillator frequency) | |
|---|---|---|---|
| | | Typical | Description |
| 000004 | 4 | 400 µs | Minimum time-out delay |
| FFFFFF | 16,777,215 | 28 minutes | Maximum time-out delay |

**Table 62. Watchdog Timer Reload Low Byte Register (WDTL)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | WDTL | | | | | | | |
| RESET | 00H | | | | | | | |
| R/W | R/W* | | | | | | | |
| Address | FF3H | | | | | | | |
| Note: A read returns the current WDT count value; a write sets the appropriate reload value. | | | | | | | | |

| Bit | Description |
|---|---|
| [7:0] WDTL | **WDT Reload Low**<br>Least significant byte (LSB), Bits[7:0], of the 24-bit WDT reload value. |

| Bit | Description (Continued) |
|---|---|
| [2]<br>TDRE | **TDRE—Transmitter Data Register Empty**<br>This bit indicates that the UART Transmit Data Register is empty and ready for additional data. Writing to the UART Transmit Data Register resets this bit.<br>0 = Do not write to the UART Transmit Data Register.<br>1 = The UART Transmit Data Register is ready to receive an additional byte to be transmitted. |
| [1]<br>TXE | **Transmitter Empty**<br>This bit indicates that the Transmit Shift Register is empty and character transmission is finished.<br>0 = Data is currently transmitting.<br>1 = Transmission is complete. |
| [0]<br>CTS | **$\overline{\text{CTS}}$ Signal**<br>When this bit is read it returns the level of the $\overline{\text{CTS}}$ signal. This signal is active Low. |

## UART Status 1 Register

This register contains multiprocessor control and status bits.

**Table 66. UART Status 1 Register (U0STAT1)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | Reserved | | | | | | NEWFRM | MPRX |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R | R | R | R | R/W | R/W | R | R |
| Address | F44H | | | | | | | |

| Bit | Description |
|---|---|
| [7:2] | **Reserved**<br>These bits are reserved and must be programmed to 000000. |
| [1]<br>NEWFRM | **New Frame**<br>A status bit denoting the start of a new frame. Reading the UART Receive Data Register resets this bit to 0.<br>0 = The current byte is not the first data byte of a new frame.<br>1 = The current byte is the first data byte of a new frame. |
| [0]<br>MPRX | **Multiprocessor Receive**<br>Returns the value of the most recent multiprocessor bit received. Reading from the UART Receive Data Register resets this bit to 0. |

## UART Transmit Data Register

Data bytes written to the UART Transmit Data (UxTXD) Register, shown in Table 67, are shifted out on the TXDx pin. The Write-only UART Transmit Data Register shares a Register File address with the read-only UART Receive Data Register.

Figure 22 displays a basic Flash Controller flow. The following subsections provide details about the various operations displayed in Figure 22.

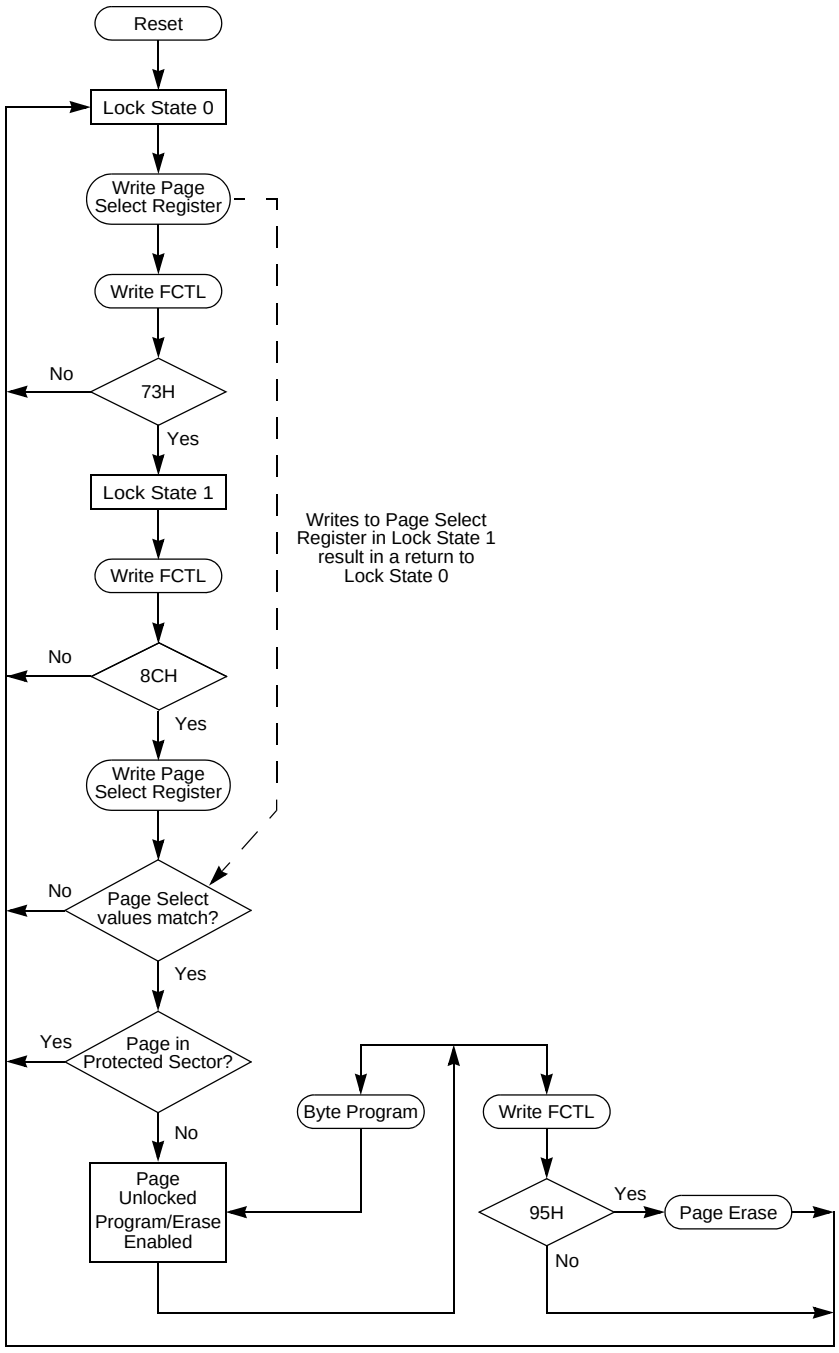


**Figure 22. Flash Controller Operation Flow Chart**

**!** **Caution:** The Flash Frequency High and Low Byte registers must be loaded with the correct value to ensure proper operation of the device. Also, Flash programming and erasure is not supported for system clock frequencies below 20 kHz or above 20 MHz.

**Table 84. Flash Frequency High Byte Register (FFREQH)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | FFREQH | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FFAH | | | | | | | |

| Bit | Description |
|---|---|
| [7:0] FFREQH | **Flash Frequency High Byte**<br>High byte of the 16-bit Flash Frequency value. |

**Table 85. Flash Frequency Low Byte Register (FFREQL)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | FFREQL | | | | | | | |
| RESET | 0 | | | | | | | |
| R/W | R/W | | | | | | | |
| Address | FFBH | | | | | | | |

| Bit | Description |
|---|---|
| [7:0] FFREQL | **Flash Frequency Low Byte**<br>Low byte of the 16-bit Flash Frequency value. |

## Trim Bit Address 0002H

**Table 92. Trim Option Bits at 0002H (TIPO)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | IPO_TRIM | | | | | | | |
| RESET | U | | | | | | | |
| R/W | R/W | | | | | | | |
| Address | Information Page Memory 0022H | | | | | | | |

Note: U = Unchanged by Reset. R/W = Read/Write.

| Bit | Description |
|---|---|
| [7:0] IPO_TRIM | **Internal Precision Oscillator Trim Byte**<br>Contains trimming bits for the Internal Precision Oscillator. |

## Trim Bit Address 0003H

**Note:** The LVD is available on 8-pin devices only.

**Table 93. Trim Option Bits at Address 0003H (TLVD)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | Reserved | | | LVD_TRIM | | | | |
| RESET | U | U | U | U | U | U | U | U |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | Information Page Memory 0023H | | | | | | | |

Note: U = Unchanged by Reset. R/W = Read/Write.

| Bit | Description |
|---|---|
| [7:5] | **Reserved**<br>These bits are reserved and must be programmed to 111. |
| [4:0] LVD_TRIM | **Low Voltage Detect Trimm**<br>This trimming affects the low voltage detection threshold. Each LSB represents a 50mV change in the threshold level. Alternatively, the low voltage threshold may be computed from the options bit value by the following equation:<br>$LVD\_LVL = 3.6\ V - LVD\_TRIM \times 0.05\ V$<br>These values are tabulated in Table 94. |

## Temperature Sensor Calibration Data

**Table 98. Temperature Sensor Calibration High Byte at 003A (TSCALH)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | TSCALH | | | | | | | |
| RESET | U | U | U | U | U | U | U | U |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | Information Page Memory 003A | | | | | | | |

Note: U = Unchanged by Reset. R/W = Read/Write.

| Bit | Description |
|---|---|
| [7:0] TSCALH | **Temperature Sensor Calibration High Byte**<br>The TSCALH and TSCALL bytes combine to form the 12-bit temperature sensor offset calibration value. For more details, see Temperature Sensor Operation on page 139. |

**Table 99. Temperature Sensor Calibration Low Byte at 003B (TSCALL)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | TSCALL | | | | | | | |
| RESET | U | U | U | U | U | U | U | U |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | Information Page Memory 003B | | | | | | | |

Note: U = Unchanged by Reset. R/W = Read/Write.

| Bit | Description |
|---|---|
| [7:0] TSCALL | **Temperature Sensor Calibration Low Byte**<br>The TSCALH and TSCALL bytes combine to form the 12-bit temperature sensor offset calibration value. For usage details, see the Temperature Sensor Operation section on page 144. |

# eZ8 CPU Instruction Summary

Table 128 summarizes the eZ8 CPU instructions. The table identifies the addressing modes employed by the instruction, the effect upon the Flags Register, the number of CPU clock cycles required for the instruction fetch and the number of CPU clock cycles required for the instruction execution.

**Table 128. eZ8 CPU Instruction Summary**

| Assembly Mnemonic | Symbolic Operation | Address Mode dst | Address Mode src | Opcode(s) (Hex) | Flags C | Z | S | V | D | H | Fetch Cycles | Instr. Cycles |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADC dst, src | dst ← dst + src + C | r | r | 12 | * | * | * | * | 0 | * | 2 | 3 |
| | | r | Ir | 13 | | | | | | | 2 | 4 |
| | | R | R | 14 | | | | | | | 3 | 3 |
| | | R | IR | 15 | | | | | | | 3 | 4 |
| | | R | IM | 16 | | | | | | | 3 | 3 |
| | | IR | IM | 17 | | | | | | | 3 | 4 |
| ADCX dst, src | dst ← dst + src + C | ER | ER | 18 | * | * | * | * | 0 | * | 4 | 3 |
| | | ER | IM | 19 | | | | | | | 4 | 3 |
| ADD dst, src | dst ← dst + src | r | r | 02 | * | * | * | * | 0 | * | 2 | 3 |
| | | r | Ir | 03 | | | | | | | 2 | 4 |
| | | R | R | 04 | | | | | | | 3 | 3 |
| | | R | IR | 05 | | | | | | | 3 | 4 |
| | | R | IM | 06 | | | | | | | 3 | 3 |
| | | IR | IM | 07 | | | | | | | 3 | 4 |
| ADDX dst, src | dst ← dst + src | ER | ER | 08 | * | * | * | * | 0 | * | 4 | 3 |
| | | ER | IM | 09 | | | | | | | 4 | 3 |

Note: Flags Notation:
* = Value is a function of the result of the operation.
– = Unaffected.
X = Undefined.
0 = Reset to 0.
1 = Set to 1.

Figure 33 displays the typical current consumption while operating with all peripherals disabled, at 30 ºC, versus the system clock frequency.

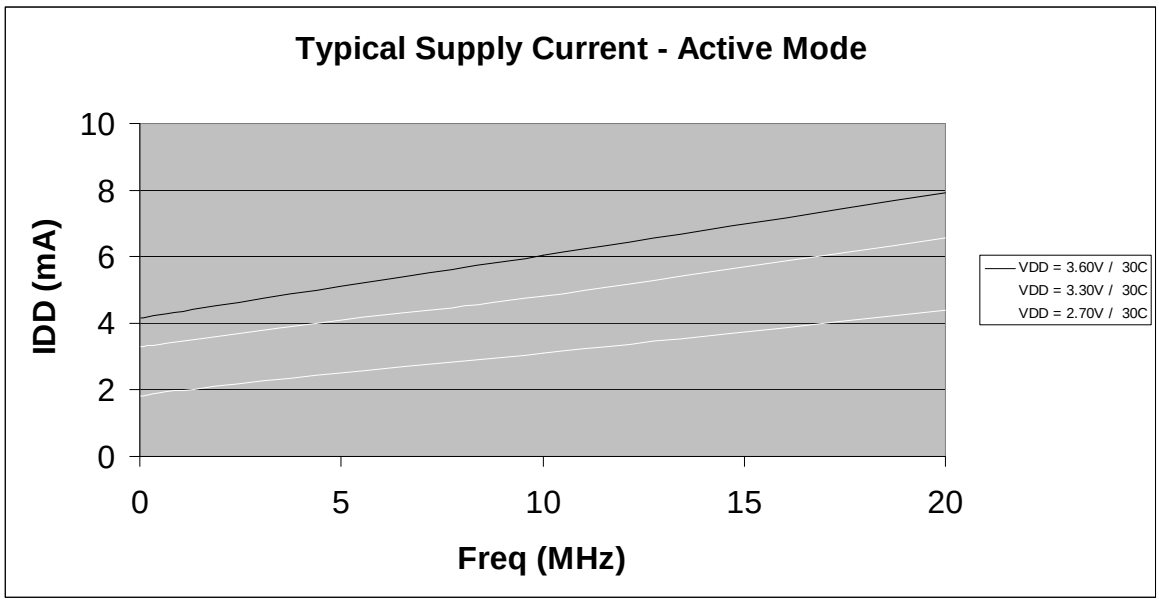


**Figure 33. Typical Active Mode $I_{DD}$ Versus System Clock Frequency**

# AC Characteristics

The section provides information about the AC characteristics and timing. All AC timing information assumes a standard load of 50pF on all outputs.

**Table 133. AC Characteristics**

| | | $V_{DD}$ = 2.7V to 3.6V<br>$T_A$ = –40°C to +105°C<br>(unless otherwise stated) | | | |
|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Minimum** | **Maximum** | **Units** | **Conditions** |
| $F_{SYSCLK}$ | System Clock Frequency | – | 20.0 | MHz | Read-only from Flash memory |
| | | 0.032768 | 20.0 | MHz | Program or erasure of the Flash memory |
| $F_{XTAL}$ | Crystal Oscillator Frequency | – | 20.0 | MHz | System clock frequencies below the crystal oscillator minimum require an external clock driver |
| $T_{XIN}$ | System Clock Period | 50 | – | ns | $T_{CLK} = 1/F_{sysclk}$ |
| $T_{XINH}$ | System Clock High Time | 20 | 30 | ns | $T_{CLK}$ = 50 ns |
| $T_{XINL}$ | System Clock Low Time | 20 | 30 | ns | $T_{CLK}$ = 50 ns |
| $T_{XINR}$ | System Clock Rise Time | – | 3 | ns | $T_{CLK}$ = 50 ns |
| $T_{XINF}$ | System Clock Fall Time | – | 3 | ns | $T_{CLK}$ = 50 ns |

**Table 134. Internal Precision Oscillator Electrical Characteristics**

| | | $V_{DD}$ = 2.7V to 3.6V<br>$T_A$ = –40°C to +105°C<br>(unless otherwise stated) | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Minimum** | **Typical** | **Maximum** | **Units** | **Conditions** |
| $F_{IPO}$ | Internal Precision Oscillator Frequency (High Speed) | | 5.53 | | MHz | $V_{DD}$ = 3.3V<br>$T_A$ = 30°C |
| $F_{IPO}$ | Internal Precision Oscillator Frequency (Low Speed) | | 32.7 | | kHz | $V_{DD}$ = 3.3V<br>$T_A$ = 30°C |
| $F_{IPO}$ | Internal Precision Oscillator Error | | $\pm$1 | $\pm$4 | % | |
| $T_{IPOST}$ | Internal Precision Oscillator Startup Time | | 3 | | µs | |

Figure 38 and Table 147 provide timing information for UART pins for the case where CTS is not used for flow control. DE asserts after the Transmit Data Register has been written. DE remains asserted for multiple characters as long as the Transmit Data Register is written with the next character before the current character has completed.

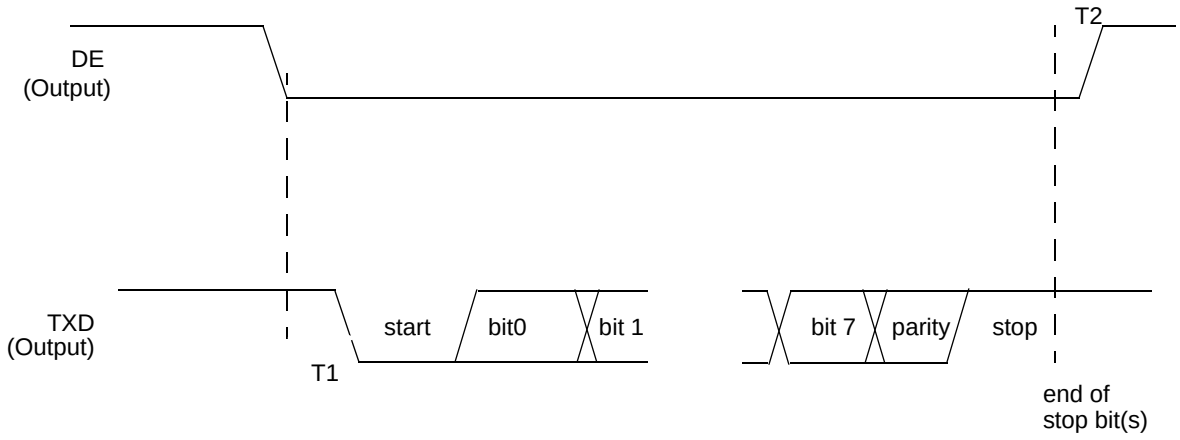


**Figure 38. UART Timing Without CTS**

**Table 147. UART Timing Without CTS**

| | | Delay (ns) | |
|---|---|---|---|
| **Parameter** | **Abbreviation** | **Minimum** | **Maximum** |
| **UART** | | | |
| $T_1$ | DE assertion to TXD falling edge (start bit) delay | 1 * $X_{IN}$ period | 1 bit time |
| $T_2$ | End of Stop Bit(s) to DE deassertion delay (Tx Data Register is empty) | ± 5 | |

**Table 148. Z8 Encore! XP F082A Series Ordering Matrix**

| Part Number | Flash | RAM | NVDS | I/O Lines | Interrupts | 16-Bit Timers w/PWM | 10-Bit A/D Channels | UART with IrDA | Comparator | Temperature Sensor | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Z8 Encore! XP F082A Series with 2 KB Flash** | | | | | | | | | | | |
| **Standard Temperature: 0°C to 70°C** | | | | | | | | | | | |
| Z8F021APB020SG | 2 KB | 512 B | 64 B | 6 | 13 | 2 | 0 | 1 | 1 | 0 | PDIP 8-pin package |
| Z8F021AQB020SG | 2 KB | 512 B | 64 B | 6 | 13 | 2 | 0 | 1 | 1 | 0 | QFN 8-pin package |
| Z8F021ASB020SG | 2 KB | 512 B | 64 B | 6 | 13 | 2 | 0 | 1 | 1 | 0 | SOIC 8-pin package |
| Z8F021ASH020SG | 2 KB | 512 B | 64 B | 17 | 19 | 2 | 0 | 1 | 1 | 0 | SOIC 20-pin package |
| Z8F021AHH020SG | 2 KB | 512 B | 64 B | 17 | 19 | 2 | 0 | 1 | 1 | 0 | SSOP 20-pin package |
| Z8F021APH020SG | 2 KB | 512 B | 64 B | 17 | 19 | 2 | 0 | 1 | 1 | 0 | PDIP 20-pin package |
| Z8F021ASJ020SG | 2 KB | 512 B | 64 B | 25 | 19 | 2 | 0 | 1 | 1 | 0 | SOIC 28-pin package |
| Z8F021AHJ020SG | 2 KB | 512 B | 64 B | 25 | 19 | 2 | 0 | 1 | 1 | 0 | SSOP 28-pin package |
| Z8F021APJ020SG | 2 KB | 512 B | 64 B | 25 | 19 | 2 | 0 | 1 | 1 | 0 | PDIP 28-pin package |
| **Extended Temperature: –40°C to 105°C** | | | | | | | | | | | |
| Z8F021APB020EG | 2 KB | 512 B | 64 B | 6 | 13 | 2 | 0 | 1 | 1 | 0 | PDIP 8-pin package |
| Z8F021AQB020EG | 2 KB | 512 B | 64 B | 6 | 13 | 2 | 0 | 1 | 1 | 0 | QFN 8-pin package |
| Z8F021ASB020EG | 2 KB | 512 B | 64 B | 6 | 13 | 2 | 0 | 1 | 1 | 0 | SOIC 8-pin package |
| Z8F021ASH020EG | 2 KB | 512 B | 64 B | 17 | 19 | 2 | 0 | 1 | 1 | 0 | SOIC 20-pin package |
| Z8F021AHH020EG | 2 KB | 512 B | 64 B | 17 | 19 | 2 | 0 | 1 | 1 | 0 | SSOP 20-pin package |
| Z8F021APH020EG | 2 KB | 512 B | 64 B | 17 | 19 | 2 | 0 | 1 | 1 | 0 | PDIP 20-pin package |
| Z8F021ASJ020EG | 2 KB | 512 B | 64 B | 25 | 19 | 2 | 0 | 1 | 1 | 0 | SOIC 28-pin package |
| Z8F021AHJ020EG | 2 KB | 512 B | 64 B | 25 | 19 | 2 | 0 | 1 | 1 | 0 | SSOP 28-pin package |
| Z8F021APJ020EG | 2 KB | 512 B | 64 B | 25 | 19 | 2 | 0 | 1 | 1 | 0 | PDIP 28-pin package |

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