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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	64 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f021asj020eg

Table 2. Signal Descriptions (Continued)

Signal Mnemonic	I/O	Description
Analog		
ANA[7:0]	I	Analog Port. These signals are used as inputs to the analog-to-digital converter (ADC).
VREF	I/O	Analog-to-digital converter reference voltage input, or buffered output for internal reference.
Low-Power Operational Amplifier (LPO)		
AMPINP/AMPINN	I	LPO inputs. If enabled, these pins drive the positive and negative amplifier inputs respectively.
AMPOUT	O	LPO output. If enabled, this pin is driven by the on-chip LPO.
Oscillators		
XIN	I	External Crystal Input. This is the input pin to the crystal oscillator. A crystal can be connected between it and the X_{OUT} pin to form the oscillator. In addition, this pin is used with external RC networks or external clock drivers to provide the system clock.
X_{OUT}	O	External Crystal Output. This pin is the output of the crystal oscillator. A crystal can be connected between it and the **XIN** pin to form the oscillator.
Clock Input		
CLKIN	I	Clock Input Signal. This pin may be used to input a TTL-level signal to be used as the system clock.
LED Drivers		
LED	O	Direct LED drive capability. All port C pins have the capability to drive an LED without any other external components. These pins have programmable drive strengths set by the GPIO block.
On-Chip Debugger		
DBG	I/O	Debug. This signal is the control and data input and output to and from the On-Chip Debugger. **Caution:** The DBG pin is open-drain and requires a pull-up resistor to ensure proper operation.

Notes:
1. PB6 and PB7 are only available in 28-pin packages without ADC. In 28-pin packages with ADC, they are replaced by AV_{DD} and AV_{SS}.
2. The AV_{DD} and AV_{SS} signals are available only in 28-pin packages with ADC. They are replaced by PB6 and PB7 on 28-pin packages without ADC.

and as long as four. A reset pulse three clock cycles in duration might trigger a reset; a pulse four cycles in duration always triggers a reset.

While the $\overline{\text{RESET}}$ input pin is asserted Low, the Z8 Encore! XP F082A Series devices remain in the Reset state. If the $\overline{\text{RESET}}$ pin is held Low beyond the System Reset time-out, the device exits the Reset state on the system clock rising edge following the $\overline{\text{RESET}}$ deassertion. Following a System Reset initiated by the external $\overline{\text{RESET}}$ pin, the EXT status bit in the Reset Status (RSTSTAT) Register is set to 1.

External Reset Indicator

During System Reset or when enabled by the GPIO logic (see Table 20 on page 46), the $\overline{\text{RESET}}$ pin functions as an open-drain (active Low) reset mode indicator in addition to the input functionality. This reset output feature allows a Z8 Encore! XP F082A Series device to reset other components to which it is connected, even if that reset is caused by internal sources such as POR, VBO or WDT events.

After an internal reset event occurs, the internal circuitry begins driving the $\overline{\text{RESET}}$ pin Low. The $\overline{\text{RESET}}$ pin is held Low by the internal circuitry until the appropriate delay listed in Table 8 has elapsed.

On-Chip Debugger Initiated Reset

A Power-On Reset can be initiated using the On-Chip Debugger by setting the RST bit in the OCD Control Register. The On-Chip Debugger block is not reset but the rest of the chip goes through a normal system reset. The RST bit automatically clears during the system reset. Following the system reset the POR bit in the Reset Status (RSTSTAT) Register is set.

Stop Mode Recovery

STOP Mode is entered by execution of a STOP instruction by the eZ8 CPU. See the Low-Power Modes chapter on page 32 for detailed STOP Mode information. During Stop Mode Recovery (SMR), the CPU is held in reset for 66 IPO cycles if the crystal oscillator is disabled or 5000 cycles if it is enabled. The SMR delay (Table 135 on page 233) T_{SMR}, also includes the time required to start up the IPO.

Stop Mode Recovery does not affect any other registers than the Watchdog Timer Control Register (WDTCTL) and the Oscillator Control Register (OSCCTL). After any Stop Mode Recovery, the IPO is enabled and selected as the system clock. If another system clock source is required, the Stop Mode Recovery code must reconfigure the oscillator control block such that the correct system clock source is enabled and selected.

The eZ8 CPU fetches the Reset vector at Program Memory addresses 0002H and 0003H and loads that value into the Program Counter. Program execution begins at the Reset vec-

Table 15. Port Alternate Function Mapping (Non 8-Pin Parts) (Continued)

Port	Pin	Mnemonic	Alternate Function Description	Alternate Function Set Register AFS1
Port C [5]	PC0	Reserved		AFS1[0]: 0
		ANA4/CINP	ADC or Comparator Input	AFS1[0]: 1
	PC1	Reserved		AFS1[1]: 0
		ANA5/CINN	ADC or Comparator Input	AFS1[1]: 1
	PC2	Reserved		AFS1[2]: 0
		ANA6/V_{REF} [4]	ADC Analog Input or ADC Voltage Reference	AFS1[2]: 1
	PC3	COUT	Comparator Output	AFS1[3]: 0
		Reserved		AFS1[3]: 1
	PC4	Reserved		AFS1[4]: 0
				AFS1[4]: 1
	PC5	Reserved		AFS1[5]: 0
				AFS1[5]: 1
	PC6	Reserved		AFS1[6]: 0
				AFS1[6]: 1
	PC7	Reserved		AFS1[7]: 0
				AFS1[7]: 1
Port D [6]	PD0	$\overline{\text{RESET}}$	External Reset	N/A

Notes:
1. Because there is only a single alternate function for each Port A pin, the Alternate Function Set registers are not implemented for Port A. Enabling alternate function selections automatically enables the associated alternate function. See the Port A D Alternate Function Subregisters (PxAF) section on page 47 for details.
2. Whether PA0/PA6 takes on the timer input or timer output complement function depends on the timer configuration. See the Timer Pin Signal Operation section on page 84 for details.
3. Because there are at most two choices of alternate function for any pin of Port B, the Alternate Function Set Register AFS2 is not used to select the function. Alternate function selection must also be enabled. See the Port A D Alternate Function Subregisters (PxAF) section on page 47 for details.
4. V_{REF} is available on PB5 in 28-pin products and on PC2 in 20-pin parts.
5. Because there are at most two choices of alternate function for any pin of Port C, the Alternate Function Set Register AFS2 is not used to select the function. Alternate function selection must also be enabled. See the Port A D Alternate Function Subregisters (PxAF) section on page 47 for details.
6. Because there is only a single alternate function for the Port PD0 pin, the Alternate Function Set registers are not implemented for Port D. Enabling alternate function selections automatically enables the associated alternate function. See the Port A D Alternate Func tion Subregisters (PxAF) section on page 47 for details.

Table 44. IRQ2 Enable and Priority Encoding

IRQ2ENH[x]	IRQ2ENL[x]	Priority	Description
0	0	Disabled	Disabled
0	1	Level 1	Low
1	0	Level 2	Medium
1	1	Level 3	High

Note: *x* indicates register bits 0 7.

Table 45. IRQ2 Enable Hi gh Bit Register (IRQ2ENH)

Bit	7	6	5	4	3	2	1	0
Field	Reserved				C3ENH	C2ENH	C1ENH	C0ENH
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC7H							

Bit	Description
[7:4]	Reserved These bits are reserved and must be programmed to 0000.
[3] C3ENH	Port C3 Interrupt Requ est Enable High Bit
[2] C2ENH	Port C2 Interrupt Requ est Enable High Bit
[1] C1ENH	Port C1 Interrupt Requ est Enable High Bit
[0] C0ENH	Port C0 Interrupt Requ est Enable High Bit

Shared Interrupt Select Register

The Shared Interrupt Select (IRQSS) Register, shown in Table 48, determines the source of the PADxS interrupts. The Shared Interrupt Select Register selects between Port A and alternate sources for the individual interrupts.

Because these shared interrupts are edge-triggered, it is possible to generate an interrupt just by switching from one shared source to another. For this reason, an interrupt must be disabled before switching between sources.

Table 48. Shared Interrupt Select Register (IRQSS)

Bit	7	6	5	4	3	2	1	0
Field	PA7VS	PA6CS	Reserved					
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FCEH							

Bit	Description
[7] PA7VS	PA7/LVD Selection 0 = PA7 is used for the interrupt for PA7VS interrupt request. 1 = The LVD is used for the interrupt for PA7VS interrupt request.
[6] PA6CS	PA6/Comparator Selection 0 = PA6 is used for the interrupt for PA6CS interrupt request. 1 = The Comparator is used for the interrupt for PA6CS interrupt request.
[5:0]	Reserved These bits are reserved and must be programmed to 000000.

Set or clear CTSE to enable or disable control from the remote receiver using the $\overline{CTS}$ pin

8. Execute an EI instruction to enable interrupts.

The UART is now configured for interrupt-driven data transmission. Because the UART Transmit Data Register is empty, an interrupt is generated immediately. When the UART Transmit interrupt is detected, the associated interrupt service routine (ISR) performs the following:

1. Write the UART Control 1 Register to select the multiprocessor bit for the byte to be transmitted:
2. Set the Multiprocessor Bit Transmitter (MPBT) if sending an address byte, clear it if sending a data byte.
3. Write the data byte to the UART Transmit Data Register. The transmitter automatically transfers the data to the Transmit Shift Register and transmits the data.
4. Clear the UART Transmit interrupt bit in the applicable Interrupt Request Register.
5. Execute the IRET instruction to return from the interrupt service routine and wait for the Transmit Data Register to again become empty.

Receiving Data using the Polled Method

Observe the following steps to configure the UART for polled data reception:

1. Write to the UART Baud Rate High and Low Byte registers to set an acceptable baud rate for the incoming data stream.
2. Enable the UART pin functions by configuring the associated GPIO port pins for alternate function operation.
3. Write to the UART Control 1 Register to enable MULTIPROCESSOR Mode functions, if appropriate.
4. Write to the UART Control 0 Register to:

   Set the receive enable bit (REN) to enable the UART for data reception

   Enable parity, if appropriate and if Multiprocessor mode is not enabled and select either even or odd parity.
5. Check the RDA bit in the UART Status 0 Register to determine if the Receive Data Register contains a valid data byte (indicated by a 1). If RDA is set to 1 to indicate available data, continue to Step 5. If the Receive Data Register is empty (indicated by a 0), continue to monitor the RDA bit awaiting reception of the valid data.

6. Read data from the UART Receive Data Register. If operating in MULTIPROCESSOR (9-bit) Mode, further actions may be required depending on the MULTIPROCESSOR Mode bits MPMD[1:0].
7. Return to Step 4 to receive additional data.

Receiving Data using the Interrupt-Driven Method

The UART Receiver interrupt indicates the availability of new data (and error conditions). Observe the following steps to configure the UART receiver for interrupt-driven operation:

1. Write to the UART Baud Rate High and Low Byte registers to set the acceptable baud rate.
2. Enable the UART pin functions by configuring the associated GPIO port pins for alternate function operation.
3. Execute a DI instruction to disable interrupts.
4. Write to the Interrupt control registers to enable the UART Receiver interrupt and set the acceptable priority.
5. Clear the UART Receiver interrupt in the applicable Interrupt Request Register.
6. Write to the UART Control 1 Register to enable Multiprocessor (9-bit) mode functions, if appropriate.

   Set the Multiprocessor Mode Select (MPEN) to Enable MULTIPROCESSOR Mode.

   Set the Multiprocessor Mode Bits, MPMD[1:0], to select the acceptable address matching scheme.

   Configure the UART to interrupt on received data and errors or errors only (interrupt on errors only is likely to be useful for Z8 Encore! devices without a DMA block)

7. Write the device address to the Address Compare Register (automatic MULTIPROCESSOR Modes only).
8. Write to the UART Control 0 Register to:

   Set the receive enable bit (REN) to enable the UART for data reception

   Enable parity, if appropriate and if multiprocessor mode is not enabled and select either even or odd parity

9. Execute an EI instruction to enable interrupts.

Rate Generator to function as an additional counter if the UART functionality is not employed.

UART Baud Rate Generator

The UART Baud Rate Generator creates a lower frequency baud rate clock for data transmission. The input to the Baud Rate Generator is the system clock. The UART Baud Rate High and Low Byte registers combine to create a 16-bit baud rate divisor value (BRG[15:0]) that sets the data transmission rate (baud rate) of the UART. The UART data rate is calculated using the following equation:

$$\text{UART Data Rate (bits/s)} = \frac{\text{System Clock Frequency (Hz)}}{16 \times \text{UART Baud Rate Divisor Value}}$$

When the UART is disabled, the Baud Rate Generator functions as a basic 16-bit timer with an interrupt upon time-out. Observe the following steps to configure the Baud Rate Generator as a timer with an interrupt upon time-out:

1. Disable the UART by clearing the REN and TEN bits in the UART Control 0 Register to 0.
2. Load the acceptable 16-bit count value into the UART Baud Rate High and Low Byte registers.
3. Enable the Baud Rate Generator timer function and associated interrupt by setting the BRGCTL bit in the UART Control 1 Register to 1.

When configured as a general purpose timer, the interrupt interval is calculated using the following equation:

Interrupt Interval (s) = System Clock Period (s) × BRG [15:0] @

UART Control Register Definitions

The UART Control registers support the UART and the associated Infrared Encoder/Decoders. For more information about infrared operation, see the Infrared Encoder/Decoder chapter on page 120.

UART Control 0 and Control 1 Registers

The UART Control 0 (UxCTL0) and Control 1 (UxCTL1) registers, shown in Tables 63 and 64, configure the properties of the UART's transmit and receive operations. The UART Control registers must not be written while the UART is enabled.

Output Data

The output format of the corrected ADC value is shown below.

MSB								LSB							
s	v	b	a	9	8	7	6	5	4	3	2	1	0	–	–

The overflow bit in the corrected output indicates that the computed value was greater than the maximum logical value (+1023) or less than the minimum logical value (1024). Unlike the hardware overflow bit, this is not a simple binary flag. For a normal (nonoverflow) sample, the sign and the overflow bit match. If the sign bit and overflow bit do not match, a computational overflow has occurred.

Input Buffer Stage

Many applications require the measurement of an input voltage source with a high output impedance. This ADC provides a buffered input for such situations. The drawback of the buffered input is a limitation of the input range. When using unity gain buffered mode, the input signal must be prevented from coming too close to either V_{SS} or V_{DD}. See Table 139 on page 236 for details.

This condition applies only to the input voltage level (with respect to ground) of each differential input signal. The actual differential input voltage magnitude may be less than 300 mV.

The input range of the unbuffered ADC swings from V_{SS} to V_{DD}. Input signals smaller than 300 mV must use the unbuffered input mode. If these signals do not contain low output impedances, they might require off-chip buffering.

Signals outside the allowable input range can be used without instability or device damage. Any ADC readings made outside the input range are subject to greater inaccuracy than specified.

ADC Control Register Definitions

This section defines the features of the following ADC Control registers.

ADC Control Register 0 (ADCCTL0) see page 134

ADC Control/Status Register 1 (ADCCTL1) see page 136

ADC Data High Byte Register (ADCD_H) see page 137

ADC Data Low Byte Register (ADCD_L) see page 137

ADC Control Register 0

The ADC Control Register 0 (ADCCTL0) selects the analog input channel and initiates the analog-to-digital conversion. It also selects the voltage reference configuration.

Table 73. ADC Control Register 0 (ADCCTL0)

Bit	7	6	5	4	3	2	1	0
Field	CEN	REFSELL	REFOUT	CONT	ANAIN[3:0]			
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F70H							

Bit	Description
[7] CEN	Conversion Enable 0 = Conversion is complete. Writing a 0 produces no effect. The ADC automatically clears this bit to 0 when a conversion is complete. 1 = Begin conversion. Writing a 1 to this bit starts a conversion. If a conversion is already in progress, the conversion restarts. This bit remains 1 until the conversion is complete.
[6] REFSELL	Voltage Reference Level Select Low Bit In conjunction with the High bit (REFSELH) in ADC Control/Status Register 1, this determines the level of the internal voltage reference; the following details the effects of {REFSELH, REFSELL}; note that this reference is independent of the Comparator reference. 00 = Internal Reference Disabled, reference comes from external pin. 01 = Internal Reference set to 1.0 V. 10 = Internal Reference set to 2.0 V (default). 11 = Reserved.
[5] REFOUT	Internal Reference Output Enable 0 = Reference buffer is disabled; Vref pin is available for GPIO or analog functions. 1 = The internal ADC reference is buffered and driven out to the V_{REF} pin. Caution: When the ADC is used with an external reference ({REFSELH,REFSELL}=00), the REFOUT bit must be set to 0.
[4] CONT	Conversion 0 = Single-shot conversion. ADC data is output once at completion of the 5129 system clock cycles (measurements of the internal temperature sensor take twice as long). 1 = Continuous conversion. ADC data updated every 256 system clock cycles after an initial 5129 clock conversion (measurements of the internal temperature sensor take twice as long).
[3:0] ANAIN[3:0]	Analog Input Select These bits select the analog input for conversion. Not all Port pins in this list are available in all packages for the Z8 Encore! XP F082A Series. For information about port pins available with each package style, see the Pin Description chapter on page 8. Do not enable unavailable analog inputs. Usage of these bits changes depending on the buffer mode selected in ADC Control/Status Register 1.

Low Power Operational Amplifier

The LPO is a general-purpose low power operational amplifier. Each of the three ports of the amplifier is accessible from the package pins. The LPO contains only one pin configuration: ANA0 is the output/feedback node, ANA1 is the inverting input and ANA2 is the noninverting input.

Operation

To use the LPO, it must be enabled in the Power Control Register 0 (PWRCTL0). The default state of the LPO is OFF. To use the LPO, the LPO bit must be cleared by turning it ON (for details, see the Power Control Register 0 section on page 33). When making normal ADC measurements on ANA0 (i.e., measurements not involving the LPO output), the LPO bit must be turned OFF. Turning the LPO ON interferes with normal ADC measurements.

! Caution: The LPO bit enables the amplifier even in STOP Mode. If the amplifier is not required in STOP Mode, disable it. Failing to perform this results in STOP Mode currents higher than necessary.

As with other ADC measurements, any pins used for analog purposes must be configured as such in the GPIO registers. See the Port A D Alternate Function Subregisters section on page 47 for details.

LPO output measurements are made on ANA0, as selected by the ANAIN[3:0] bits of ADC Control Register 0. It is also possible to make single-ended measurements on ANA1 and ANA2 while the amplifier is enabled, which is often useful for determining offset conditions. Differential measurements between ANA0 and ANA2 may be useful for noise cancellation purposes.

If the LPO output is routed to the ADC, then the BUFFMODE[2:0] bits of ADC Control/Status Register 1 must also be configured for unity-gain buffered operation. Sampling the LPO in an unbuffered mode is not recommended.

When either input is overdriven, the amplifier output saturates at the positive or negative supply voltage. No instability results.

Temperature Sensor Calibration Data

Table 98. Temperature Sensor Calibration High Byte at 003A (TSCALH)

Bit	7	6	5	4	3	2	1	0
Field	TSCALH							
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Information Page Memory 003A							

Note: U = Unchanged by Reset. R/W = Read/Write.

Bit	Description
[7:0] TSCALH	Temperature Sensor Calibration High Byte The TSCALH and TSCALL bytes combine to form the 12-bit temperature sensor offset calibration value. For more details, see Temperature Sensor Operation on page 139.

Table 99. Temperature Sensor Calibration Low Byte at 003B (TSCALL)

Bit	7	6	5	4	3	2	1	0
Field	TSCALL							
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Information Page Memory 003B							

Note: U = Unchanged by Reset. R/W = Read/Write.

Bit	Description
[7:0] TSCALL	Temperature Sensor Calibration Low Byte The TSCALH and TSCALL bytes combine to form the 12-bit temperature sensor offset calibration value. For usage details, see the Temperature Sensor Operation section on page 144.

Randomized Lot Identifier

Table 104. Lot Id entification Number (RAND_LOT)

Bit	7	6	5	4	3	2	1	0
Field	RAND_LOT							
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Interspersed throughout Information Page Memory							

Note: U = Unchanged by Reset. R/W = Read/Write.

Bit	Description
[7] RAND_LOT	Randomized Lot ID The randomized lot ID is a 32-byte binary value that changes for each production lot. See Table 105.

Table 105. Randomized Lot ID Locations

Info Page Address	Memory Address	Usage
3C	FE3C	Randomized Lot ID Byte 31 (most significant).
3D	FE3D	Randomized Lot ID Byte 30.
3E	FE3E	Randomized Lot ID Byte 29.
3F	FE3F	Randomized Lot ID Byte 28.
58	FE58	Randomized Lot ID Byte 27.
59	FE59	Randomized Lot ID Byte 26.
5A	FE5A	Randomized Lot ID Byte 25.
5B	FE5B	Randomized Lot ID Byte 24.
5C	FE5C	Randomized Lot ID Byte 23.
5D	FE5D	Randomized Lot ID Byte 22.
5E	FE5E	Randomized Lot ID Byte 21.
5F	FE5F	Randomized Lot ID Byte 20.
61	FE61	Randomized Lot ID Byte 19.
62	FE62	Randomized Lot ID Byte 18.
64	FE64	Randomized Lot ID Byte 17.
65	FE65	Randomized Lot ID Byte 16.
67	FE67	Randomized Lot ID Byte 15.
68	FE68	Randomized Lot ID Byte 14.

Byte Read

To read a byte from the NVDS array, user code must first push the address onto the stack. User code issues a CALL instruction to the address of the byte-read routine (0x1000). At the return from the sub-routine, the read byte resides in working register R0 and the read status byte resides in working register R1. The contents of the status byte are undefined for read operations to illegal addresses. Also, the user code must pop the address byte off the stack.

The read routine uses 9 bytes of stack space in addition to the one byte of address pushed by the user. Sufficient memory must be available for this stack usage.

Because of the Flash memory architecture, NVDS reads exhibit a nonuniform execution time. A read operation takes between 54 and 489 µs (assuming a 20 MHz system clock). Slower system clock speeds result in proportionally higher execution times.

NVDS byte reads from invalid addresses (those exceeding the NVDS array size) return 0xff. Illegal read operations have a 2 µs execution time.

The status byte returned by the NVDS read routine is zero for successful read, as determined by a CRC check. If the status byte is non-zero, there was a corrupted value in the NVDS array at the location being read. In this case, the value returned in R0 is the byte most recently written to the array that does not have a CRC error.

Power Failure Protection

The NVDS routines employ error checking mechanisms to ensure a power failure endangers only the most recently written byte. Bytes previously written to the array are not perturbed.

A system reset (such as a pin reset or Watchdog Timer reset) that occurs during a write operation also perturbs the byte currently being written. All other bytes in the array are unperturbed.

Optimizing NVDS Memory Usage for Execution Speed

NVDS read time can vary drastically. This discrepancy is a trade-off for minimizing the frequency of writes that require post-write page erases, as indicated in Table 107. The NVDS read time of address N is a function of the number of writes to addresses other than N since the most recent write to address N, or the number of writes since the most recent page erase. Neglecting effects caused by page erases and results caused by the initial condition in which the NVDS is blank, a rule of thumb is that every write since the most recent page erase causes read times of unwritten addresses to increase by 1 µs, up to a maximum of (511-NVDS_SIZE) µs.

eZ8 CPU Instruction Summary

Table 128 summarizes the eZ8 CPU instructions. The table identifies the addressing modes employed by the instruction, the effect on the Flags Register, the number of CPU clock cycles required for the instruction fetch and the number of CPU clock cycles required for the instruction execution.

Table 128. eZ8 CPU Instruction Summary

Assembly Mnemonic	Symbolic Operation	Address Mode dst	Address Mode src	Opcode(s) (Hex)	Flags C	Z	S	V	D	H	Fetch Cycles	Instr. Cycles
ADC dst, src	dst ← dst + src + C	r	r	12	*	*	*	*	0	*	2	3
		r	Ir	13							2	4
		R	R	14							3	3
		R	IR	15							3	4
		R	IM	16							3	3
		IR	IM	17							3	4
ADCX dst, src	dst ← dst + src + C	ER	ER	18	*	*	*	*	0	*	4	3
		ER	IM	19							4	3
ADD dst, src	dst ← dst + src	r	r	02	*	*	*	*	0	*	2	3
		r	Ir	03							2	4
		R	R	04							3	3
		R	IR	05							3	4
		R	IM	06							3	3
		IR	IM	07							3	4
ADDX dst, src	dst ← dst + src	ER	ER	08	*	*	*	*	0	*	4	3
		ER	IM	09							4	3

Note: Flags Notation:
* = Value is a function of the result of the operation.
– = Unaffected.
X = Undefined.
0 = Reset to 0.
1 = Set to 1.

Table 128. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode dst	Address Mode src	Opcode(s) (Hex)	Flags C	Z	S	V	D	H	Fetch Cycles	Instr. Cycles
DA dst	dst m DA(dst)	R		40	*	*	*	X			2	2
		IR		41							2	3
DEC dst	dst m dst - 1	R		30		*	*	*			2	2
		IR		31							2	3
DECW dst	dst m dst - 1	RR		80		*	*	*			2	5
		IRR		81							2	6
DI	IRQCTL[7] m 0			8F							1	2
DJNZ dst, RA	dst m dst 1 if dst z0 PC m PC + X	r		0A-FA							2	3
EI	IRQCTL[7] m 1			9F							1	2
HALT	Halt Mode			7F							1	2
INC dst	dst m dst + 1	R		20		*	*				2	2
		IR		21							2	3
		r		0E-FE							1	2
INCW dst	dst m dst + 1	RR		A0		*	*	*			2	5
		IRR		A1							2	6
IRET	FLAGS m @SP SP m SP + 1 PC m @SP SP m SP + 2 IRQCTL[7] m 1			BF	*	*	*	*	*	*	1	5
JP dst	PC m dst	DA		8D							3	2
		IRR		C4							2	3
JP cc, dst	if cc is true PC m dst	DA		0D-FD							3	2

Note: Flags Notation:
* = Value is a function of the result of the operation.
= Unaffected.
X = Undefined.
0 = Reset to 0.
1 = Set to 1.

UART Timing

Figure 37 and Table 146 provide timing information for UART pins for the case where CTS is used for flow control. The CTS to DE assertion delay (T1) assumes the Transmit Data Register has been loaded with data prior to CTS assertion.

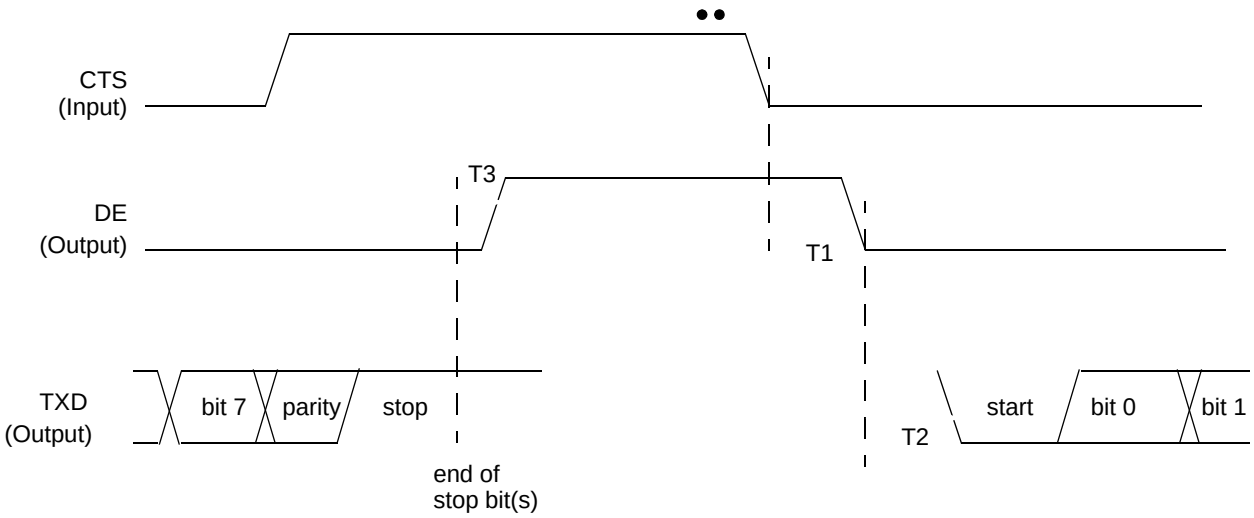

Figure 37. UART Timing With CTS

Table 146. UART Timing With CTS

		Delay (ns)	
Parameter	Abbreviation	Minimum	Maximum
UART			
T_1	CTS Fall to DE output delay	2 * X_{IN} period	2 * X_{IN} period + 1 bit time
T_2	DE assertion to TXD falling edge (start bit) delay	– 5	
T_3	End of Stop Bit(s) to DE deassertion delay	– 5	

Table 148. Z8 Encore! XP F082A Series Ordering Matrix

Part Number	Flash	RAM	NVDS	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description
Z8 Encore! XP F082A Series with 1KB Flash											
Standard Temperature: 0°C to 70°C											
Z8F011APB020SG	1KB	256 B	16 B	6	13	2	0	1	1	0	PDIP 8-pin package
Z8F011AQB020SG	1KB	256 B	16 B	6	13	2	0	1	1	0	QFN 8-pin package
Z8F011ASB020SG	1KB	256 B	16 B	6	13	2	0	1	1	0	SOIC 8-pin package
Z8F011ASH020SG	1KB	256 B	16 B	17	19	2	0	1	1	0	SOIC 20-pin package
Z8F011AHH020SG	1KB	256 B	16 B	17	19	2	0	1	1	0	SSOP 20-pin package
Z8F011APH020SG	1KB	256 B	16 B	17	19	2	0	1	1	0	PDIP 20-pin package
Z8F011ASJ020SG	1KB	256 B	16 B	25	19	2	0	1	1	0	SOIC 28-pin package
Z8F011AHJ020SG	1KB	256 B	16 B	25	19	2	0	1	1	0	SSOP 28-pin package
Z8F011APJ020SG	1KB	256 B	16 B	25	19	2	0	1	1	0	PDIP 28-pin package
Extended Temperature: 40°C to 105°C											
Z8F011APB020EG	1KB	256 B	16 B	6	13	2	0	1	1	0	PDIP 8-pin package
Z8F011AQB020EG	1KB	256 B	16 B	6	13	2	0	1	1	0	QFN 8-pin package
Z8F011ASB020EG	1KB	256 B	16 B	6	13	2	0	1	1	0	SOIC 8-pin package
Z8F011ASH020EG	1KB	256 B	16 B	17	19	2	0	1	1	0	SOIC 20-pin package
Z8F011AHH020EG	1KB	256 B	16 B	17	19	2	0	1	1	0	SSOP 20-pin package
Z8F011APH020EG	1KB	256 B	16 B	17	19	2	0	1	1	0	PDIP 20-pin package
Z8F011ASJ020EG	1KB	256 B	16 B	25	19	2	0	1	1	0	SOIC 28-pin package
Z8F011AHJ020EG	1KB	256 B	16 B	25	19	2	0	1	1	0	SSOP 28-pin package
Z8F011APJ020EG	1KB	256 B	16 B	25	19	2	0	1	1	0	PDIP 28-pin package

Table 148. Z8 Encore! XP F082A Series Ordering Matrix

Part Number	Flash	RAM	NVDS	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description
Z8 Encore! XP F082A Series Development Kit											
Z8F08A28100KITG	Z8 Encore! XP F082A Series 28-Pin Development Kit										
Z8F04A28100KITG	Z8 Encore! XP F042A Series 28-Pin Development Kit										
Z8F04A08100KITG	Z8 Encore! XP F042A Series 8-Pin Development Kit										
ZUSBSC00100ZACG	USB Smart Cable Accessory Kit										
ZUSBOPTSC01ZACG	USB Opto-Isolated Smart Cable Accessory Kit										
ZENETSC0100ZACG	Ethernet Smart Cable Accessory Kit										