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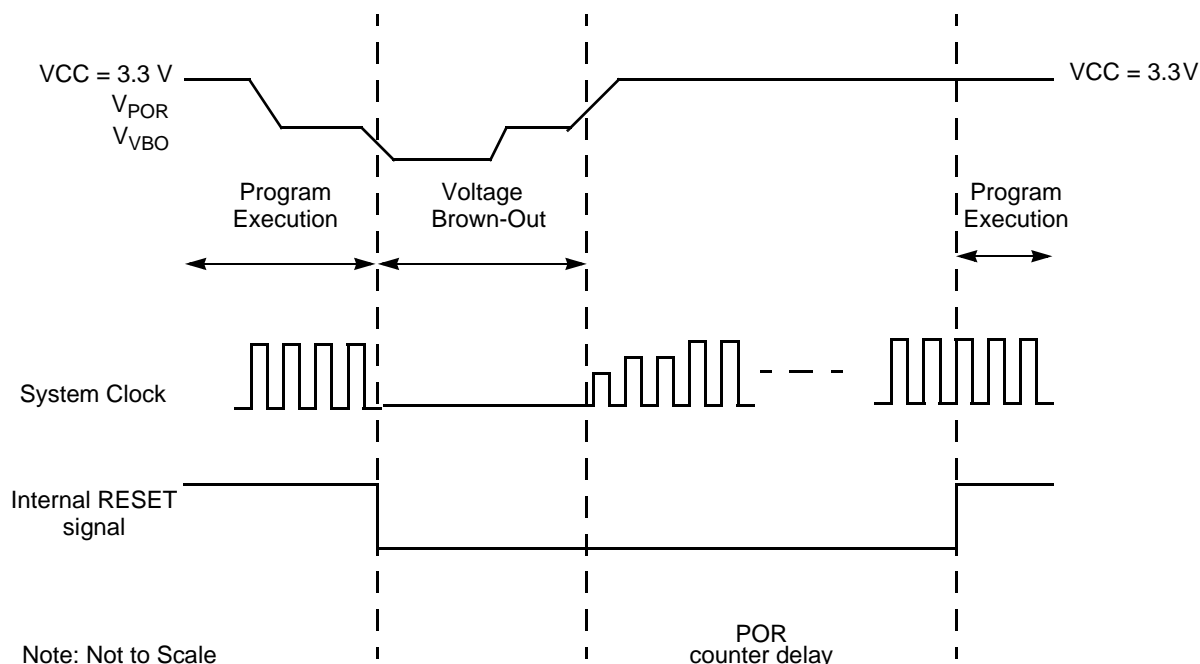
#### Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, Temp Sensor, WDT
Number of I/O	23
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	64 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.173", 4.40mm Width)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/z8f022ahj020eg">https://www.e-xfl.com/product-detail/zilog/z8f022ahj020eg</a>

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**Figure 6. Voltage Brown-Out Reset Operation**

The POR level is greater than the VBO level by the specified hysteresis value. This ensures that the device undergoes a Power-On Reset after recovering from a VBO condition.

## Watchdog Timer Reset

If the device is operating in NORMAL or HALT Mode, the Watchdog Timer can initiate a System Reset at time-out if the WDT\_RES Flash option bit is programmed to 1, i.e., the unprogrammed state of the WDT\_RES Flash option bit. If the bit is programmed to 0, it configures the Watchdog Timer to cause an interrupt, not a System Reset, at time-out.

The WDT bit in the Reset Status (RSTSTAT) Register is set to signify that the reset was initiated by the Watchdog Timer.

## External Reset Input

The  $\overline{\text{RESET}}$  pin has a Schmitt-Triggered input and an internal pull-up resistor. Once the  $\overline{\text{RESET}}$  pin is asserted for a minimum of four system clock cycles, the device progresses through the System Reset sequence. Because of the possible asynchronicity of the system clock and reset signals, the required reset duration may be as short as three clock periods

Table 15. Port Alternate Function Mapping (Non 8-Pin Parts) (Continued)

Port	Pin	Mnemonic	Alternate Function Description	Alternate Function Set Register AFS1
Port C <sup>5</sup>	PC0	Reserved		AFS1[0]: 0
		ANA4/CINP	ADC or Comparator Input	AFS1[0]: 1
	PC1	Reserved		AFS1[1]: 0
		ANA5/CINN	ADC or Comparator Input	AFS1[1]: 1
	PC2	Reserved		AFS1[2]: 0
		ANA6/V <sub>REF</sub> <sup>4</sup>	ADC Analog Input or ADC Voltage Reference	AFS1[2]: 1
	PC3	COUT	Comparator Output	AFS1[3]: 0
		Reserved		AFS1[3]: 1
	PC4	Reserved		AFS1[4]: 0
				AFS1[4]: 1
	PC5	Reserved		AFS1[5]: 0
				AFS1[5]: 1
	PC6	Reserved		AFS1[6]: 0
				AFS1[6]: 1
	PC7	Reserved		AFS1[7]: 0
				AFS1[7]: 1
Port D <sup>6</sup>	PD0	RESET	External Reset	N/A

## Notes:

1. Because there is only a single alternate function for each Port A pin, the Alternate Function Set registers are not implemented for Port A. Enabling alternate function selections automatically enables the associated alternate function. See the [Port A–D Alternate Function Subregisters \(PxAF\)](#) section on page 47 for details.
2. Whether PA0/PA6 takes on the timer input or timer output complement function depends on the timer configuration. See the [Timer Pin Signal Operation](#) section on page 84 for details.
3. Because there are at most two choices of alternate function for any pin of Port B, the Alternate Function Set Register AFS2 is not used to select the function. Alternate function selection must also be enabled. See the [Port A–D Alternate Function Subregisters \(PxAF\)](#) section on page 47 for details.
4. V<sub>REF</sub> is available on PB5 in 28-pin products and on PC2 in 20-pin parts.
5. Because there are at most two choices of alternate function for any pin of Port C, the Alternate Function Set Register AFS2 is not used to select the function. Alternate function selection must also be enabled. See the [Port A–D Alternate Function Subregisters \(PxAF\)](#) section on page 47 for details.
6. Because there is only a single alternate function for the Port PD0 pin, the Alternate Function Set registers are not implemented for Port D. Enabling alternate function selections automatically enables the associated alternate function. See the [Port A–D Alternate Function Subregisters \(PxAF\)](#) section on page 47 for details.

## GPIO Interrupts

Many of the GPIO port pins can be used as interrupt sources. Some port pins can be configured to generate an interrupt request on either the rising edge or falling edge of the pin input signal. Other port pin interrupt sources generate an interrupt when any edge occurs (both rising and falling). See the [GPIO Mode Interrupt Controller](#) chapter on page 55 for more information about interrupts using the GPIO pins.

## GPIO Control Register Definitions

Four registers for each port provide access to GPIO control, input data and output data. Table 17 lists these port registers. Use the Port A–D Address and Control registers together to provide access to subregisters for port configuration and control.

**Table 17. GPIO Port Registers and Subregisters**

<b>Port Register Mnemonic</b>	<b>Port Register Name</b>
PxADDR	Port A–D Address Register; selects subregisters.
PxCTL	Port A–D Control Register; provides access to subregisters.
PxIN	Port A–D Input Data Register.
PxOUT	Port A–D Output Data Register.
<b>Port Subregister Mnemonic</b>	<b>Port Register Name</b>
PxDD	Data Direction.
PxAF	Alternate Function.
PxOC	Output Control (Open-Drain).
PxHDE	High Drive Enable.
PxSMRE	Stop Mode Recovery Source Enable.
PxPUE	Pull-up Enable.
PxAFS1	Alternate Function Set 1.
PxAFS2	Alternate Function Set 2.

## Port A–D Control Registers

The Port A–D Control registers set the GPIO port operation. The value in the corresponding Port A–D Address Register determines which subregister is read from or written to by a Port A–D Control Register transaction; see Table 20.

**Table 20. Port A–D Control Registers (PxCTL)**

Bit	7	6	5	4	3	2	1	0
Field	PCTL							
RESET	00H							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FD1H, FD5H, FD9H, FDDH							

Bit	Description
[7:0]	<b>Port Control</b>
PCTLx	The Port Control Register provides access to all subregisters that configure the GPIO port operation.

Note: x indicates the specific GPIO port pin number (7–0).

## Port A–D Data Direction Subregisters

The Port A–D Data Direction subregister is accessed through the Port A–D Control Register by writing 01H to the Port A–D Address Register; see Table 21.

**Table 21. Port A–D Data Direction Subregisters (PxDD)**

Bit	7	6	5	4	3	2	1	0
Field	DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	If 01H in Port A–D Address Register, accessible through the Port A–D Control Register							

Bit	Description
[7:0]	<b>Data Direction</b>
DDx	These bits control the direction of the associated port pin. Port Alternate Function operation overrides the Data Direction Register setting. 0 = Output. Data in the Port A–D Output Data Register is driven onto the port pin. 1 = Input. The port pin is sampled and the value written into the Port A–D Input Data Register. The output driver is tristated.

Note: x indicates the specific GPIO port pin number (7–0).

The window remains open until the count again reaches 8 (that is, 24 baud clock periods since the previous pulse was detected), giving the Endec a sampling window of minus four baud rate clocks to plus eight baud rate clocks around the expected time of an incoming pulse. If an incoming pulse is detected inside this window this process is repeated. If the incoming data is a logical 1 (no pulse), the Endec returns to the initial state and waits for the next falling edge. As each falling edge is detected, the Endec clock counter is reset, resynchronizing the Endec to the incoming signal, allowing the Endec to tolerate jitter and baud rate errors in the incoming datastream. Resynchronizing the Endec does not alter the operation of the UART, which ultimately receives the data. The UART is only synchronized to the incoming data stream when a Start bit is received.

## Infrared Encoder/Decoder Control Register Definitions

All infrared endec configuration and status information is set by the UART Control registers as defined in the Universal Asynchronous Receiver/Transmitter section on page 99.

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**!** **Caution:** To prevent spurious signals during IrDA data transmission, set the IREN bit in the UART Control 1 Register to 1 to enable the Infrared Encoder/Decoder before enabling the GPIO Port alternate function for the corresponding pin.

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## Flash Operation Timing Using the Flash Frequency Registers

Before performing either a program or erase operation on Flash memory, you must first configure the Flash Frequency High and Low Byte registers. The Flash Frequency registers allow programming and erasing of the Flash with system clock frequencies ranging from 32 kHz (32768 Hz) through 20 MHz.

The Flash Frequency High and Low Byte registers combine to form a 16-bit value, FFREQ, to control timing for Flash program and erase operations. The 16-bit binary Flash Frequency value must contain the system clock frequency (in kHz). This value is calculated using the following equation:

$$\text{FFREQ}[15:0] = \frac{\text{System Clock Frequency (Hz)}}{1000}$$

---

**! Caution:** Flash programming and erasure are not supported for system clock frequencies below 32 kHz (32768 Hz) or above 20 MHz. The Flash Frequency High and Low Byte registers must be loaded with the correct value to ensure operation of the Z8 Encore! XP F082A Series devices.

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## Flash Code Protection Against External Access

The user code contained within the Flash memory can be protected against external access by the on-chip debugger. Programming the FRP Flash option bit prevents reading of the user code with the On-Chip Debugger. See the [Flash Option Bits](#) chapter on page 159 and the [On-Chip Debugger](#) chapter on page 180 for more information.

## Flash Code Protection Against Accidental Program and Erasure

The Z8 Encore! XP F082A Series provides several levels of protection against accidental program and erasure of the Flash memory contents. This protection is provided by a combination of the Flash option bits, the register locking mechanism, the page select redundancy and the sector level protection control of the Flash Controller.

### Flash Code Protection Using the Flash Option Bits

The FRP and FWP Flash option bits combine to provide three levels of Flash Program Memory protection, as shown in Table 79. See the [Flash Option Bits](#) chapter on page 159 for more information.

Bit	Description (Continued)
[5:4] OSC_SEL[1:0]	<b>Oscillator Mode Selection</b> 00 = On-chip oscillator configured for use with external RC networks (<4MHz). 01 = Minimum power for use with very low frequency crystals (32kHz to 1.0MHz). 10 = Medium power for use with medium frequency crystals or ceramic resonators (0.5MHz to 5.0MHz). 11 = Maximum power for use with high frequency crystals (5.0MHz to 20.0MHz). This setting is the default for unprogrammed (erased) Flash.
[3] VBO_AO	<b>Voltage Brown-Out Protection Always On</b> 0 = Voltage Brown-Out Protection can be disabled in STOP Mode to reduce total power consumption. For the block to be disabled, the power control register bit must also be written (see the <a href="#">Power Control Register Definitions</a> section on page 33). 1 = Voltage Brown-Out Protection is always enabled including during STOP Mode. This setting is the default for unprogrammed (erased) Flash.
[2] FRP	<b>Flash Read Protect</b> 0 = User program code is inaccessible. Limited control features are available through the On-Chip Debugger. 1 = User program code is accessible. All On-Chip Debugger commands are enabled. This setting is the default for unprogrammed (erased) Flash.
[1]	<b>Reserved</b> This bit is reserved and must be programmed to 1.
[0] FWP	<b>Flash Write Protect</b> This Option Bit provides Flash Program Memory protection: 0 = Programming and erasure disabled for all of Flash Program Memory. Programming, Page Erase and Mass Erase through User Code is disabled. Mass Erase is available using the On-Chip Debugger. 1 = Programming, Page Erase and Mass Erase are enabled for all of Flash program memory.

## Flash Program Memory Address 0001H

Table 89. Flash Options Bits at Program Memory Address 0001H

Bit	7	6	5	4	3	2	1	0
Field	Reserved			XTLDIS	Reserved			
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Program Memory 0001H							
Note: U = Unchanged by Reset. R/W = Read/Write.								

Bit	Description
[7:5]	<b>Reserved</b> These bits are reserved and must be programmed to 111.
[4] XTLDIS	<b>State of the Crystal Oscillator at Reset</b> This bit only enables the crystal oscillator. Its selection as a system clock must be performed manually. 0 = Crystal oscillator is enabled during reset, resulting in longer reset timing. 1 = Crystal oscillator is disabled during reset, resulting in shorter reset timing.  <b>Caution:</b> Programming the XTLDIS bit to zero on 8-pin versions of this device prevents any further communication via the debug pin due to the fact that the XIN and DBG functions are shared on pin 2 of this package. Do not program this bit to zero on 8-pin devices unless further debugging or Flash programming is not required.
[3:0]	<b>Reserved</b> These bits are reserved and must be programmed to 1111.

## Trim Bit Address Space

All available Trim bit addresses and their functions are listed in Table 90 through Table 95.

### Trim Bit Address 0000H

Table 90. Trim Options Bits at Address 0000H

Bit	7	6	5	4	3	2	1	0
Field	Reserved							
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Information Page Memory 0020H							
Note: U = Unchanged by Reset. R/W = Read/Write.								

Bit	Description
[7:0]	<b>Reserved</b> These bits are reserved; altering this register may result in incorrect device operation.

### Trim Bit Address 0001H

Table 91. Trim Option Bits at 0001H

Bit	7	6	5	4	3	2	1	0
Field	Reserved							
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Information Page Memory 0021H							
Note: U = Unchanged by Reset. R/W = Read/Write.								

Bit	Description
[7:0]	<b>Reserved</b> These bits are reserved; altering this register may result in incorrect device operation.

## Trim Bit Address 0004H

Table 95. Trim Option Bits at 0004H

Bit	7	6	5	4	3	2	1	0
Field	Reserved							
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Information Page Memory 0024H							
Note: U = Unchanged by Reset. R/W = Read/Write.								

Bit	Description
[7:0]	<b>Reserved</b> These bits are reserved; altering this register may result in incorrect device operation.

## Zilog Calibration Data

This section briefly describes the features of the following Flash option bit calibration registers.

ADC Calibration Data: see page 169

Temperature Sensor Calibration Data: see page 171

Watchdog Timer Calibration Data: see page 172

Serialization Data: see page 173

Randomized Lot Identifier: see page 174

Table 109. Debug Command Enable/Disable (Continued)

Debug Command	Command Byte	Enabled when Not in DEBUG Mode?	Disabled by Flash Read Protect Option Bit
Write Program Counter	06H	–	Disabled.
Read Program Counter	07H	–	Disabled.
Write Register	08H	–	Only writes of the Flash Memory Control registers are allowed. Additionally, only the Mass Erase command is allowed to be written to the Flash Control Register.
Read Register	09H	–	Disabled.
Write Program Memory	0AH	–	Disabled.
Read Program Memory	0BH	–	Disabled.
Write Data Memory	0CH	–	Yes.
Read Data Memory	0DH	–	–
Read Program Memory CRC	0EH	–	–
Reserved	0FH	–	–
Step Instruction	10H	–	Disabled.
Stuff Instruction	11H	–	Disabled.
Execute Instruction	12H	–	Disabled.
Reserved	13H–FFH	–	–

In the list of OCD commands that follows, data and commands sent from the host to the On-Chip Debugger are identified by  $\text{DBG} \leftarrow \text{Command/Data}$ . Data sent from the On-Chip Debugger back to the host is identified by  $\text{DBG} \rightarrow \text{Data}$ .

**Read OCD Revision (00H).** The Read OCD Revision command determines the version of the On-Chip Debugger. If OCD commands are added, removed, or changed, this revision number changes.

$\text{DBG} \leftarrow 00\text{H}$

$\text{DBG} \rightarrow \text{OCDRev}[15:8]$  (Major revision number)

$\text{DBG} \rightarrow \text{OCDRev}[7:0]$  (Minor revision number)

**Read OCD Status Register (02H).** The Read OCD Status Register command reads the OCDSTAT Register.

$\text{DBG} \leftarrow 02\text{H}$

$\text{DBG} \rightarrow \text{OCDSTAT}[7:0]$

**Read Runtime Counter (03H).** The Runtime Counter counts system clock cycles in between Breakpoints. The 16-bit Runtime Counter counts up from 0000H and stops at the maximum count of FFFFH. The Runtime Counter is overwritten during the Write Memory,

Bit	Description (Continued)
[5] DBGACK	<b>Debug Acknowledge</b> This bit enables the debug acknowledge feature. If this bit is set to 1, the OCD sends a Debug Acknowledge character (FFH) to the host when a Breakpoint occurs. 0 = Debug Acknowledge is disabled. 1 = Debug Acknowledge is enabled.
[4:1]	<b>Reserved</b> These bits are reserved and must be programmed to 0000.
[0] RST	<b>Reset</b> Setting this bit to 1 resets the Z8F04xA family device. The device goes through a normal Power-On Reset sequence with the exception that the On-Chip Debugger is not reset. This bit is automatically cleared to 0 at the end of reset. 0 = No effect. 1 = Reset the Flash Read Protect Option Bit device.

## OCD Status Register

The OCD Status Register reports status information about the current state of the debugger and the system.

**Table 111. OCD Status Register (OCDSTAT)**

Bit	7	6	5	4	3	2	1	0
Field	DBG	HALT	FRPENB	Reserved				
RESET	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R

Bit	Description
[7] DBG	<b>Debug Status</b> 0 = NORMAL Mode. 1 = DEBUG Mode.
[6] HALT	<b>HALT Mode</b> 0 = Not in HALT Mode. 1 = In HALT Mode.
[5] FRPENB	<b>Flash Read Protect Option Bit Enable</b> 0 = FRP bit enabled, that allows disabling of many OCD commands. 1 = FRP bit has no effect.
[4:0]	<b>Reserved</b> These bits are reserved and must be programmed to 00000.

# Oscillator Control

The Z8 Encore! XP F082A Series devices uses five possible clocking schemes, each user-selectable:

- Internal precision trimmed RC oscillator (IPO)
- On-chip oscillator using off-chip crystal or resonator
- On-chip oscillator using external RC network
- External clock drive
- On-chip low power Watchdog Timer oscillator
- Clock failure detection circuitry

In addition, Z8 Encore! XP F082A Series devices contain clock failure detection and recovery circuitry, allowing continued operation despite a failure of the system clock oscillator.

## Operation

This chapter discusses the logic used to select the system clock and handle primary oscillator failures.

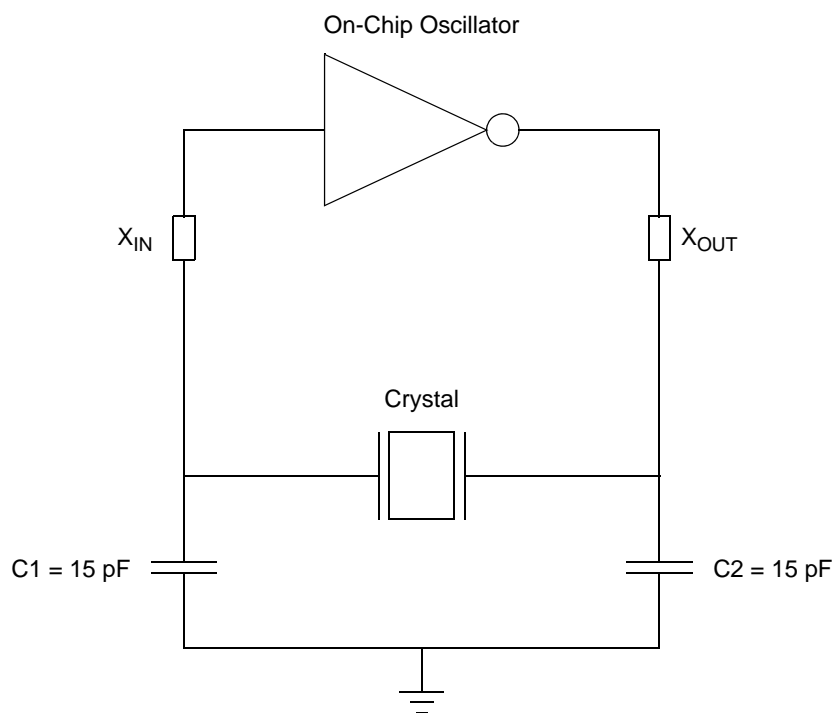
### System Clock Selection

The oscillator control block selects from the available clocks. Table 112 details each clock source and its usage.



► **Note:** The stabilization time varies depending on the crystal, resonator or feedback network used. See Table 115 for transconductance values to compute oscillator stabilization times.

Figure 27 displays a recommended configuration for connection with an external fundamental-mode, parallel-resonant crystal operating at 20MHz. Recommended 20MHz crystal specifications are provided in Table 114. Printed circuit board layouts must add no more than 4pF of stray capacitance to either the  $X_{IN}$  or  $X_{OUT}$  pins. If oscillation does not occur, reduce the values of capacitors C1 and C2 to decrease loading.



**Figure 27. Recommended 20MHz Crystal Oscillator Configuration**

## Internal Precision Oscillator

The internal precision oscillator (IPO) is designed for use without external components. You can either manually trim the oscillator for a nonstandard frequency or use the automatic factory-trimmed version to achieve a 5.53MHz frequency. IPO features include:

- On-chip RC oscillator that does not require external components
- Output frequency of either 5.53MHz or 32.8kHz (contains both a fast and a slow mode)
- Trimmed through Flash option bits with user override
- Elimination of crystals or ceramic resonators in applications where very high timing accuracy is not required

### Operation

An 8-bit trimming register, incorporated into the design, compensates for absolute variation of oscillator frequency. Once trimmed the oscillator frequency is stable and does not require subsequent calibration. Trimming is performed during manufacturing and is not necessary for you to repeat unless a frequency other than 5.53MHz (fast mode) or 32.8kHz (slow mode) is required. This trimming is done at +30°C and a supply voltage of 3.3V, so accuracy of this operating point is optimal.

If not used, the IPO can be disabled by the Oscillator Control Register (see the [Oscillator Control Register Definitions](#) section on page 196).

By default, the oscillator frequency is set by the factory trim value stored in the write-protected Flash information page. However, the user code can override these trim values as described in the [Trim Bit Address Space](#) section on page 165.

Select one of two frequencies for the oscillator (5.53MHz and 32.8kHz) using the OSC-SEL bits in the the [Oscillator Control](#) chapter on page 193.

Table 126. Program Control Instructions

Mnemonic	Operands	Instruction
BRK	—	On-Chip Debugger Break
BTJ	p, bit, src, DA	Bit Test and Jump
BTJNZ	bit, src, DA	Bit Test and Jump if Non-Zero
BTJZ	bit, src, DA	Bit Test and Jump if Zero
CALL	dst	Call Procedure
DJNZ	dst, src, RA	Decrement and Jump Non-Zero
IRET	—	Interrupt Return
JP	dst	Jump
JP cc	dst	Jump Conditional
JR	DA	Jump Relative
JR cc	DA	Jump Relative Conditional
RET	—	Return
TRAP	vector	Software Trap

Table 127. Rotate and Shift Instructions

Mnemonic	Operands	Instruction
BSWAP	dst	Bit Swap
RL	dst	Rotate Left
RLC	dst	Rotate Left through Carry
RR	dst	Rotate Right
RRC	dst	Rotate Right through Carry
SRA	dst	Shift Right Arithmetic
SRL	dst	Shift Right Logical
SWAP	dst	Swap Nibbles

Table 128. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode		Opcode(s) (Hex)	Flags						Fetch Cycle s	Instr. Cycle s
		dst	src		C	Z	S	V	D	H		
TMX dst, src	dst AND src	ER	ER	78	–	*	*	0	–	–	4	3
		ER	IM	79							4	3
TRAP Vector	SP ← SP – 2 @SP ← PC SP ← SP – 1 @SP ← FLAGS PC ← @Vector		Vector	F2	–	–	–	–	–	–	2	6
WDT				5F	–	–	–	–	–	–	1	2
XOR dst, src	dst ← dst XOR src	r	r	B2	–	*	*	0	–	–	2	3
		r	lr	B3							2	4
		R	R	B4							3	3
		R	IR	B5							3	4
		R	IM	B6							3	3
		IR	IM	B7							3	4
XORX dst, src	dst ← dst XOR src	ER	ER	B8	–	*	*	0	–	–	4	3
		ER	IM	B9							4	3

Note: Flags Notation:

\* = Value is a function of the result of the operation.

– = Unaffected.

X = Undefined.

0 = Reset to 0.

1 = Set to 1.

UART Timing

Figure 37 and Table 146 provide timing information for UART pins for the case where CTS is used for flow control. The CTS to DE assertion delay (T1) assumes the Transmit Data Register has been loaded with data prior to CTS assertion.

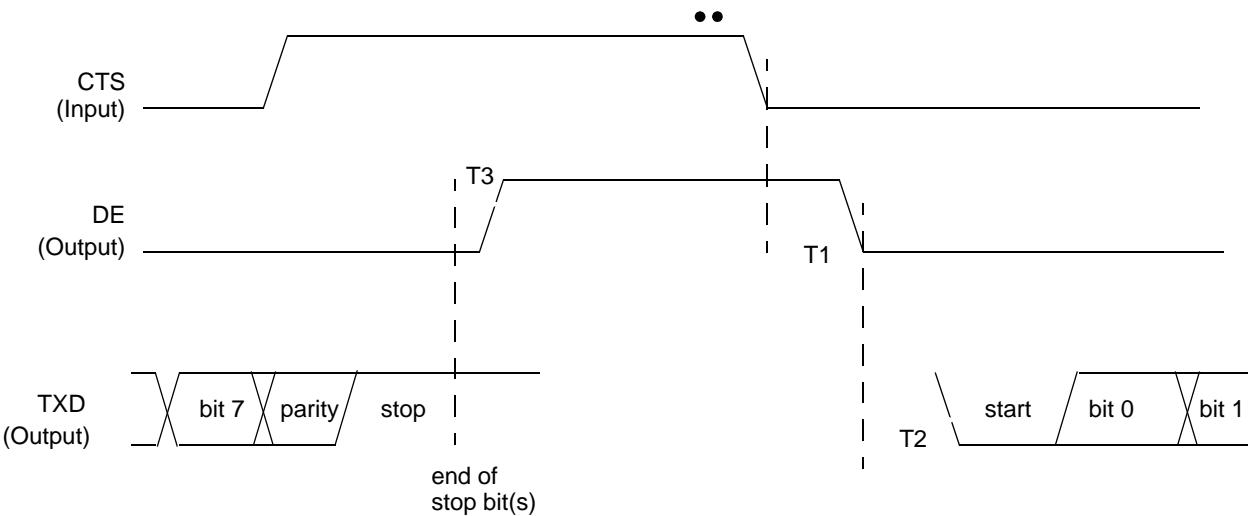


Figure 37. UART Timing With CTS

Table 146. UART Timing With CTS

Parameter	Abbreviation	Delay (ns)	
		Minimum	Maximum
UART			
T <sub>1</sub>	CTS Fall to DE output delay	2 * X <sub>IN</sub> period	2 * X <sub>IN</sub> period + 1 bit time
T <sub>2</sub>	DE assertion to TXD falling edge (start bit) delay	± 5	
T <sub>3</sub>	End of Stop Bit(s) to DE deassertion delay	± 5	