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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f041aph020sg

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Z8 Encore! XP[®] F082A Series Product Specification

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Signal Descriptions

Table 2 describes the Z8 Encore! XP F082A Series signals. See the <u>Pin Configurations</u> section on page 8 to determine the signals available for the specific package styles.

Signal Mnemonic	I/O	Description
General-Purpose I/C) Ports	A–D
PA[7:0]	I/O	Port A. These pins are used for general-purpose I/O.
PB[7:0]	I/O	Port B. These pins are used for general-purpose I/O. PB6 and PB7 are available only in those devices without an ADC.
PC[7:0]	I/O	Port C. These pins are used for general-purpose I/O.
PD[0]	I/O	Port D. This pin is used for general-purpose output only.
UART Controllers		
TXD0	0	Transmit Data. This signal is the transmit output from the UART and IrDA.
RXD0	I	Receive Data. This signal is the receive input for the UART and IrDA.
CTS0	Ι	Clear To Send. This signal is the flow control input for the UART.
DE	0	Driver Enable. This signal allows automatic control of external RS-485 drivers. This signal is approximately the inverse of the TXE (Transmit Empty) bit in the UART Status 0 Register. The DE signal may be used to ensure the external RS-485 driver is enabled when data is transmitted by the UART.
Timers		
T0OUT/T1OUT	0	Timer Output 0–1. These signals are outputs from the timers.
T0OUT/T1OUT	0	Timer Complement Output 0–1. These signals are output from the timers in PWM Dual Output mode.
T0IN/T1IN	I	Timer Input 0–1. These signals are used as the capture, gating and counter inputs.
Comparator		
CINP/CINN	Ι	Comparator Inputs. These signals are the positive and negative inputs to the comparator.
COUT	0	Comparator Output.
Notes:		

Table 2. Signal Descriptions

1. PB6 and PB7 are only available in 28-pin packages without ADC. In 28-pin packages with ADC, they are replaced by AV_{DD} and AV_{SS} .

2. The AV_{DD} and AV_{SS} signals are available only in 28-pin packages with ADC. They are replaced by PB6 and PB7 on 28-pin packages without ADC.

Reset, Stop Mode Recovery and Low Voltage Detection

The Reset Controller within the Z8 Encore! XP F082A Series controls Reset and Stop Mode Recovery operation and provides indication of low supply voltage conditions. In typical operation, the following events cause a Reset:

- Power-On Reset (POR)
- Voltage Brown-Out (VBO)
- Watchdog Timer time-out (when configured by the WDT_RES Flash option bit to initiate a reset)
- External **RESET** pin assertion (when the alternate **RESET** function is enabled by the GPIO Register)
- On-chip debugger initiated Reset (OCDCTL[0] set to 1)

When the device is in STOP Mode, a Stop Mode Recovery is initiated by either of the following occurrences:

- Watchdog Timer time-out
- GPIO Port input pin transition on an enabled Stop Mode Recovery source

The low voltage detection circuitry on the device (available on the 8-pin product versions only) performs the following functions:

- Generates the VBO reset when the supply voltage drops below a minimum safe level.
- Generates an interrupt when the supply voltage drops below a user-defined level (8-pin devices only).

Reset Types

The Z8 Encore! XP F082A Series provides several different types of Reset operation. Stop Mode Recovery is considered as a form of Reset. Table 8 lists the types of Reset and their operating characteristics. The System Reset is longer if the external crystal oscillator is enabled by the Flash option bits, allowing additional time for oscillator start-up.

Reset Sources

Table 9 lists the possible sources of a system reset.

	Table 9. Reset Source	ces and Resulting Reset Type
_		

Operating Mode	Reset Source	Special Conditions	
NORMAL or HALT modes	Power-On Reset/Voltage Brown- Out	Reset delay begins after supply voltage exceeds POR level.	
	Watchdog Timer time-out when configured for Reset	None.	
	RESET pin assertion	All reset pulses less than three system clocks in width are ignored.	
	On-Chip Debugger initiated Reset (OCDCTL[0] set to 1)	System Reset, except the On-Chip Debugger is unaffected by the reset.	
STOP Mode	Power-On Reset/Voltage Brown- Out	Reset delay begins after supply voltage exceeds POR level.	
	RESET pin assertion	All reset pulses less than the specified analog delay are ignored. See Table 131 on page 229.	
	DBG pin driven Low	None.	

Power-On Reset

Z8 Encore! XP F082A Series devices contain an internal Power-On Reset circuit. The POR circuit monitors the supply voltage and holds the device in the Reset state until the supply voltage reaches a safe operating level. After the supply voltage exceeds the POR voltage threshold (VPOR), the device is held in the Reset state until the POR Counter has timed out. If the crystal oscillator is enabled by the option bits, this time-out is longer.

After the Z8 Encore! XP F082A Series device exits the Power-On Reset state, the eZ8 CPU fetches the Reset vector. Following Power-On Reset, the POR status bit in the Reset Status (RSTSTAT) Register is set to 1.

Figure 5 displays Power-On Reset operation. See Electrical Characteristics on page 221 for the POR threshold voltage (V_{POR}).

Bit	7	6	5	4	3	2	1	0
Field	POC7	POC6	POC5	POC4	POC3	POC2	POC1	POC0
RESET		00H (Ports A-C); 01H (Port D)						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	If 03H in Port A–D Address Register, accessible through the Port A–D Control Register							

Table 23. Port A–D Output Control Subregisters (PxOC)

Bit	Description
[7:0]	Port Output Control
POC	K These bits function independently of the alternate function bit and always disable the drains if set to 1.
	0 = The source current is enabled for any output mode unless overridden by the alternate func- tion (push-pull output).
	1 = The source current for the associated pin is disabled (open-drain mode).
Note:	x indicates the specific GPIO port pin number (7–0).

Port A–D High Drive Enable Subregisters

The Port A–D High Drive Enable Subregister, shown in Table 24, is accessed through the port A–D Control Register by writing 04H to the Port A–D Address Register. Setting the bits in the Port A–D High Drive Enable subregisters to 1 configures the specified port pins for high current output drive operation. The Port A–D High Drive Enable subregister affects the pins directly and, as a result, alternate functions are also affected.

Bit	7	6	5	4	3	2	1	0
Field	PHDE7	PHDE6	PHDE5	PHDE4	PHDE3	PHDE2	PHDE1	PHDE0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	lf 04H ir	n Port A–D A	Address Reg	gister, acces	sible throug	h the Port A	–D Control F	Register

Table 24. Port A–D High Drive Enable Subregisters (PxHDE)

Bit	Description
[7:0] PHDEx	Port High Drive Enabled 0 = The port pin is configured for standard output current drive.
	1 = The port pin is configured for high output current drive.
Note: x inc	dicates the specific GPIO port pin number (7–0).

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Port A–D Stop Mode Recovery Source Enable Subregisters

The Port A–D Stop Mode Recovery Source Enable Subregister, shown in Table 25, is accessed through the Port A–D Control Register by writing 05H to the Port A–D Address Register. Setting the bits in the Port A–D Stop Mode Recovery Source Enable subregisters to 1 configures the specified port pins as a Stop Mode Recovery source. During STOP Mode, any logic transition on a port pin enabled as a Stop Mode Recovery source initiates Stop Mode Recovery.

Table 25. Port A–D Stop Mode Recovery Source Enable Subregisters (PxSMRE)

Bit	7	6	5	4	3	2	1	0
Field	PSMRE7	PSMRE6	PSMRE5	PSMRE4	PSMRE3	PSMRE2	PSMRE1	PSMRE0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	If 05H i	n Port A–D A	Address Reg	jister, acces	sible throug	h the Port A	–D Control I	Register

Bit Description

[7:0] **Port Stop Mode Recovery Source Enabled**

PSMREx 0 = The port pin is not configured as a Stop Mode Recovery source. Transitions on this pin during STOP Mode do not initiate Stop Mode Recovery.

1 = The port pin is configured as a Stop Mode Recovery source. Any logic transition on this pin during STOP Mode initiates Stop Mode Recovery.

Note: x indicates the specific GPIO port pin number (7-0).

- 5. Enable the timer interrupt, if appropriate and set the timer interrupt priority by writing to the relevant interrupt registers. By default, the timer interrupt is generated for both input capture and reload events. If appropriate, configure the timer interrupt to be generated only at the input capture event or the reload event by setting TICONFIG field of the TxCTL0 Register.
- 6. Configure the associated GPIO port pin for the Timer Input alternate function.
- 7. Write to the Timer Control Register to enable the timer and initiate counting.

In CAPTURE Mode, the elapsed time from timer start to Capture event can be calculated using the following equation:

Capture Elapsed Time (s) = $\frac{(Capture Value - Start Value) \times Prescale}{System Clock Frequency (Hz)}$

CAPTURE RESTART Mode

In CAPTURE RESTART Mode, the current timer count value is recorded when the acceptable external Timer Input transition occurs. The Capture count value is written to the Timer PWM High and Low Byte registers. The timer input is the system clock. The TPOL bit in the Timer Control Register determines if the Capture occurs on a rising edge or a falling edge of the Timer Input signal. When the Capture event occurs, an interrupt is generated and the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. The INPCAP bit in TxCTL0 Register is set to indicate the timer interrupt is because of an input capture event.

If no Capture event occurs, the timer counts up to the 16-bit Compare value stored in the Timer Reload High and Low Byte registers. Upon reaching the reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. The INPCAP bit in TxCTL0 Register is cleared to indicate the timer interrupt is not caused by an input capture event.

Observe the following steps for configuring a timer for CAPTURE RESTART Mode and initiating the count:

- 1. Write to the Timer Control Register to:
 - Disable the timer
 - Configure the timer for CAPTURE RESTART Mode by writing the TMODE bits in the TxCTL1 Register and the TMODEHI bit in TxCTL0 Register
 - Set the prescale value
 - Set the Capture edge (rising or falling) for the Timer Input
- 2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H).

- Set the Capture edge (rising or falling) for the Timer Input
- 2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H).
- 3. Write to the Timer Reload High and Low Byte registers to set the Compare value.
- 4. Enable the timer interrupt, if appropriate and set the timer interrupt priority by writing to the relevant interrupt registers.By default, the timer interrupt are generated for both input capture and reload events. If appropriate, configure the timer interrupt to be generated only at the input capture event or the reload event by setting TICONFIG field of the TxCTL0 Register.
- 5. Configure the associated GPIO port pin for the Timer Input alternate function.
- 6. Write to the Timer Control Register to enable the timer.
- 7. Counting begins on the first appropriate transition of the Timer Input signal. No interrupt is generated by this first edge.

In CAPTURE/COMPARE Mode, the elapsed time from timer start to Capture event can be calculated using the following equation:

Capture Elapsed Time (s) = $\frac{(Capture Value - Start Value) \times Prescale}{System Clock Frequency (Hz)}$

Reading the Timer Count Values

The current count value in the timers can be read while counting (enabled). This capability has no effect on timer operation. When the timer is enabled and the Timer High Byte Register is read, the contents of the Timer Low Byte Register are placed in a holding register. A subsequent read from the Timer Low Byte Register returns the value in the holding register. This operation allows accurate reads of the full 16-bit timer count value while enabled. When the timers are not enabled, a read from the Timer Low Byte Register returns the actual value in the counter.

Timer Pin Signal Operation

The timer output function is a GPIO port pin alternate function. The Timer Output is toggled every time the counter is reloaded.

Bit Description (Continued)

[6] **GATED Mode**

- TPOL (cont'd)
- 0 = Timer counts when the Timer Input signal is High (1) and interrupts are generated on the falling edge of the Timer Input.
 - 1 = Timer counts when the Timer Input signal is Low (0) and interrupts are generated on the rising edge of the Timer Input.

CAPTURE/COMPARE Mode

- 0 = Counting is started on the first rising edge of the Timer Input signal. The current count is captured on subsequent rising edges of the Timer Input signal.
- 1 = Counting is started on the first falling edge of the Timer Input signal. The current count is captured on subsequent falling edges of the Timer Input signal.

PWM DUAL OUTPUT Mode

- 0 = Timer Output is forced Low (0) and Timer Output Complement is forced High (1) when the timer is disabled. When enabled, the Timer Output is forced High (1) upon PWM count match and forced Low (0) upon reload. When enabled, the Timer Output Complement is forced Low (0) upon PWM count match and forced High (1) upon reload. The PWMD field in TxCTL0 Register is a programmable delay to control the number of cycles time delay before the Timer Output and the Timer Output Complement is forced to High (1).
- 1 = Timer Output is forced High (1) and Timer Output Complement is forced Low (0) when the timer is disabled. When enabled, the Timer Output is forced Low (0) upon PWM count match and forced High (1) upon reload. When enabled, the Timer Output Complement is forced High (1) upon PWM count match and forced Low (0) upon reload. The PWMD field in TxCTL0 Register is a programmable delay to control the number of cycles time delay before the Timer Output and the Timer Output Complement is forced to Low (0).

CAPTURE RESTART Mode

- 0 = Count is captured on the rising edge of the Timer Input signal.
- 1 = Count is captured on the falling edge of the Timer Input signal.

COMPARATOR COUNTER Mode

When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer Reload. Also:

0 =Count is captured on the rising edge of the comparator output.

1 = Count is captured on the falling edge of the comparator output.

Caution: When the Timer Output alternate function TxOUT on a GPIO port pin is enabled, TxOUT changes to whatever state the TPOL bit is in. The timer does not need to be enabled for that to happen. Also, the Port Data Direction Subregister is not required to be set to output on TxOUT. Changing the TPOL bit with the timer enabled and running does not immediately change the TxOUT.

Bit	7	6	5	4	3	2	1	0
Field	MPMD[1]	MPEN		MPBT	DEPOL	BRGCTL	RDAIRQ	IREN
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address				F4	3H			
Bit	Descript	tion						
 MOLTIPROCESSOR Mode MPMD[1,0] If MULTIPROCESSOR (9-bit) Mode is enabled: 00 = The UART generates an interrupt request on all received bytes (data and address). 01 = The UART generates an interrupt request only on received address bytes. 10 = The UART generates an interrupt request when a received address byte matches the value stored in the Address Compare Register and on all successive data bytes until an address mismatch occurs. 11 = The UART generates an interrupt request on all received data bytes for which the most recent address byte matched the value in the Address Compare Register. [6] MULTIPROCESSOR (9-bit) Enable MPEN This bit is used to enable MULTIPROCESSOR (9-bit) Mode. 0 = Disable MULTIPROCESSOR (9-bit) Mode. 							ddress). atches the bytes until th the most	
[4] MPBT	Multipro This bit is used by tion. 0 = Senc 1 = Senc	cessor Bit s applicable the receiving a 0 in the r a 1 in the r	Transmit only when M g device to c nultiprocess nultiprocess	MULTIPROC determine if or bit locatic or bit locatic	EESSOR (9- the data byte on of the data	bit) Mode is e contains a a stream (da a stream (ac	enabled. Th ddress or da ata byte). ddress byte).	ne 9th bit is ata informa-
DEPOL	0 = DE s 1 = DE s	ignal is Acti	ve High. ve Low.					

Table 64. UART Control 1 Register (U0CTL1)

- If the internal voltage reference must be output to a pin, set the REFEXT bit to 1. The internal voltage reference must be enabled in this case.
- Write the REFSELL bit of the pair {REFSELH, REFSELL} to select the internal voltage reference level or to disable the internal reference. The REFSELH bit is contained in the ADC Control/Status Register 1.
- Set CEN to 1 to start the conversion.
- 4. CEN remains 1 while the conversion is in progress. A single-shot conversion requires 5129 system clock cycles to complete. If a single-shot conversion is requested from an ADC powered down state, the ADC uses 40 additional clock cycles to power up before beginning the 5129 cycle conversion.
- 5. When the conversion is complete, the ADC control logic performs the following operations:
 - 13-bit two's-complement result written to {ADCD_H[7:0], ADCD_L[7:3]}
 - Sends an interrupt request to the Interrupt Controller denoting conversion complete
 - CEN resets to 0 to indicate the conversion is complete
- 6. If the ADC remains idle for 160 consecutive system clock cycles, it is automatically powered down.

Continuous Conversion

When configured for continuous conversion, the ADC continuously performs an analogto-digital conversion on the selected analog input. Each new data value overwrites the previous value stored in the ADC Data registers. An interrupt is generated after each conversion.

Caution: In CONTINUOUS Mode, ADC updates are limited by the input signal bandwidth of the ADC and the latency of the ADC and its digital filter. Step changes at the input are not immediately detected at the next output from the ADC. The response of the ADC (in all modes) is limited by the input signal bandwidth and the latency.

Observe the following steps for setting up the ADC and initiating continuous conversion:

- 1. Enable the appropriate analog input by configuring the general-purpose I/O pins for alternate function. This action disables the digital input and output driver.
- 2. Write the ADC Control/Status Register 1 to configure the ADC.

8KB Flash		4KB Flash			
Program Memor	ry	Program Memo	ry	2KB Flash	
	Addresses (hex)		Addresses (hex)	Addresses	s (hex)
Sector 7	1C00	Sector 7	0E00	Sector 3	07FF
Sector 6	1BFF	Sector 6	0DFF	Sector 2)400
	1800 17FF		0C00 0BFF	Sector 1)200
Sector 5	1400	Sector 5	0A00	Sector 0)1FF
Sector 4	13FF 1000	Sector 4	09FF 0800	(1000
Sector 3	0FFF 0C00	Sector 3	07FF 0600	1 KB Flash Program Memory Addresse	s (hex)
Sector 2	0BFF 0800	Sector 2	05FF 0400	Sector 1	03FF
Sector 1	07FF 0400	Sector 1	03FF 0200	Sector 0	01FF
Sector 0	03FF 0000	Sector 0	01FF 0000		

Figure 21. Flash Memory Arrangement

Flash Information Area

The Flash information area is separate from Program Memory and is mapped to the address range FE00H to FFFFH. This area is readable but cannot be erased or overwritten. Factory trim values for the analog peripherals are stored here. Factory calibration data for the ADC is also stored here.

Operation

The Flash Controller programs and erases Flash memory. The Flash Controller provides the proper Flash controls and timing for Byte Programming, Page Erase and Mass Erase of Flash memory.

The Flash Controller contains several protection mechanisms to prevent accidental programming or erasure. These mechanism operate on the page, sector and full-memory levels.

Flash Controller Behavior in DEBUG Mode

The following changes in behavior of the Flash Controller occur when the Flash Controller is accessed using the On-Chip Debugger:

- The Flash Write Protect option bit is ignored.
- The Flash Sector Protect Register is ignored for programming and erase operations.
- Programming operations are not limited to the page selected in the Page Select Register.
- Bits in the Flash Sector Protect Register can be written to one or zero.
- The second write of the Page Select Register to unlock the Flash Controller is not necessary.
- The Page Select Register can be written when the Flash Controller is unlocked.
- The Mass Erase command is enabled through the Flash Control Register.

Caution: For security reasons, the Flash controller allows only a single page to be opened for write/ erase. When writing multiple Flash pages, the flash controller must go through the unlock sequence again to select another page.

Flash Control Register Definitions

This section defines the features of the following Flash Control registers.

Flash Control Register: see page 153

Flash Status Register: see page 155

Flash Page Select Register: see page 156

Flash Sector Protect Register: see page 157

Flash Frequency High and Low Byte Registers: see page 157

Flash Control Register

The Flash Controller must be unlocked using the Flash Control (FCTL) Register before programming or erasing the Flash memory. Writing the sequence 73H 8CH, sequentially, to the Flash Control Register unlocks the Flash Controller. When the Flash Controller is unlocked, the Flash memory can be enabled for Mass Erase or Page Erase by writing the appropriate enable command to the FCTL. Page Erase applies only to the active page selected in Flash Page Select Register. Mass Erase is enabled only through the On-Chip

Flash Program Memory Address 0001H

Table 89. Flash Options Bits at Program Memory Address 0001H

Bit	7	6	5	4	3	2	1	0		
Field	Reserved			XTLDIS	Reserved					
RESET	U	U	U	U	U	U U		U		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Address	Program Memory 0001H									

Note: U = Unchanged by Reset. R/W = Read/Write.

Bit	Description								
[7:5]	Reserved								
	These bits are reserved and must be programmed to 111.								
[4]	State of the Crystal Oscillator at Reset								
XTLDIS	This bit only enables the crystal oscillator. Its selection as a system clock must be performed manually.								
	0 = Crystal oscillator is enabled during reset, resulting in longer reset timing.								
	1 = Crystal oscillator is disabled during reset, resulting in shorter reset timing.								
	Caution: Programming the XTLDIS bit to zero on 8-pin versions of this device prevents any further communication via the debug pin due to the fact that the XIN and DBG functions are shared on pin 2 of this package. Do not program this bit to zero on 8-pin devices unless further debugging or Flash programming is not required.								
[3:0]	Reserved These bits are reserved and must be programmed to 1111								

Table 123. CPU Control Instructions (Continued)

Mnemonic	Operands	Instruction
RCF	_	Reset Carry Flag
SCF	—	Set Carry Flag
SRP	src	Set Register Pointer
STOP	—	STOP Mode
WDT		Watchdog Timer Refresh

Table 124. Load Instructions

Mnemonic	Operands	Instruction
CLR	dst	Clear
LD	dst, src	Load
LDC	dst, src	Load Constant to/from Program Memory
LDCI	dst, src	Load Constant to/from Program Memory and Auto- Increment Addresses
LDE	dst, src	Load External Data to/from Data Memory
LDEI	dst, src	Load External Data to/from Data Memory and Auto- Increment Addresses
LDWX	dst, src	Load Word using Extended Addressing
LDX	dst, src	Load using Extended Addressing
LEA	dst, X(src)	Load Effective Address
POP	dst	Рор
POPX	dst	Pop using Extended Addressing
PUSH	src	Push
PUSHX	src	Push using Extended Addressing

Table 125. Logical Instructions

Mnemonic	Operands	Instruction
AND	dst, src	Logical AND
ANDX	dst, src	Logical AND using Extended Addressing
COM	dst	Complement
OR	dst, src	Logical OR
ORX	dst, src	Logical OR using Extended Addressing
XOR	dst, src	Logical Exclusive OR
XORX	dst, src	Logical Exclusive OR using Extended Addressing

General Purpose I/O Port Output Timing

Figure 35 and Table 144 provide timing information for GPIO port pins.



Figure 3	5. GPIO	Port Ou	tput Timing
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		Delay (ns)			
Parameter	Abbreviation	Minimum	Maximum		
GPIO port pi	ns				
T ₁	X _{IN} Rise to Port Output Valid Delay	-	15		
T ₂	X _{IN} Rise to Port Output Hold Time	2	-		

Table 144. GPIO Port Output Timing

Jart Number	Elash	MAM Mitth 3	SOVN	// V Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description
Standard Tomporatu			ND FIAS	ы, то		Anan	Jy-lu	-Digi		JIIVe	
	2 KB	512 B	64 B	6	14	2	Δ	1	1	1	PDIP 8-nin nackade
Z8F022A0B020SG	2 KB	512 B	64 B	6	14	2	4	1	1	1	OFN 8-pin package
Z8F022ASB020SG	2 KB	512 B	64 B	6	14	2	4	1	1	1	SOIC 8-pin package
Z8F022ASH020SG	2 KB	512 B	64 B	17	20	2	7	1	1	1	SOIC 20-pin package
Z8F022AHH020SG	2 KB	512 B	64 B	17	20	2	7	1	1	1	SSOP 20-pin package
Z8F022APH020SG	2 KB	512 B	64 B	17	20	2	7	1	1	1	PDIP 20-pin package
Z8F022ASJ020SG	2 KB	512 B	64 B	23	20	2	8	1	1	1	SOIC 28-pin package
Z8F022AHJ020SG	2 KB	512 B	64 B	23	20	2	8	1	1	1	SSOP 28-pin package
Z8F022APJ020SG	2 KB	512 B	64 B	23	20	2	8	1	1	1	PDIP 28-pin package
Extended Temperatu	re: –40°	°C to 10	5°C								
Z8F022APB020EG	2 KB	512 B	64 B	6	14	2	4	1	1	1	PDIP 8-pin package
Z8F022AQB020EG	2 KB	512 B	64 B	6	14	2	4	1	1	1	QFN 8-pin package
Z8F022ASB020EG	2 KB	512 B	64 B	6	14	2	4	1	1	1	SOIC 8-pin package
Z8F022ASH020EG	2 KB	512 B	64 B	17	20	2	7	1	1	1	SOIC 20-pin package
Z8F022AHH020EG	2 KB	512 B	64 B	17	20	2	7	1	1	1	SSOP 20-pin package
Z8F022APH020EG	2 KB	512 B	64 B	17	20	2	7	1	1	1	PDIP 20-pin package
Z8F022ASJ020EG	2 KB	512 B	64 B	23	20	2	8	1	1	1	SOIC 28-pin package
Z8F022AHJ020EG	2 KB	512 B	64 B	23	20	2	8	1	1	1	SSOP 28-pin package
Z8F022APJ020EG	2 KB	512 B	64 B	23	20	2	8	1	1	1	PDIP 28-pin package

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