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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, Temp Sensor, WDT
Number of I/O	6
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	8-VDFN Exposed Pad
Supplier Device Package	8-QFN (5x6)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f042aqb020eg

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Signal Mnemonic	I/O	Description
Reset		
RESET	I/O	RESET. Generates a Reset when asserted (driven Low). Also serves as a reset indicator; the Z8 Encore! XP forces this pin low when in reset. This pin is open-drain and features an enabled internal pull-up resistor.
Power Supply		
V _{DD}	Ι	Digital Power Supply.
AV _{DD}	I	Analog Power Supply.
V _{SS}	I	Digital Ground.
AV _{SS}	I	Analog Ground.
Notes:		

Table 2. Signal Descriptions (Continued)

inotes

1. PB6 and PB7 are only available in 28-pin packages without ADC. In 28-pin packages with ADC, they are replaced by AV_DD and $\mathsf{AV}_\mathsf{SS}.$

2. The AV_{DD} and AV_{SS} signals are available only in 28-pin packages with ADC. They are replaced by PB6 and PB7 on 28-pin packages without ADC.

Pin Characteristics

Table 3 describes the characteristics for each pin available on the Z8 Encore! XP F082A Series 20- and 28-pin devices. Data in Table 3 is sorted alphabetically by the pin symbol mnemonic.

Table 4 on page 14 provides detailed information about the characteristics for each pin available on the Z8 Encore! XP F082A Series 8-pin devices.

Note: All six I/O pins on the 8-pin packages are 5 V-tolerant (unless the pull-up devices are enabled). The column in Table 3 below describes 5 V-tolerance for the 20- and 28-pin packages only.

Register Map

Table 7 provides the address map for the Register File of the Z8 Encore! XP F082A Series devices. Not all devices and package styles in the Z8 Encore! XP F082A Series support the ADC, or all of the GPIO Ports. Consider registers for unimplemented peripherals as Reserved.

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page
General-Purpos	e RAM			
Z8F082A/Z8F08	1A Devices			
000–3FF	General-Purpose Register File RAM	—	XX	
400–EFF	Reserved	—	XX	
Z8F042A/Z8F04	1A Devices			
000–3FF	General-Purpose Register File RAM	—	XX	
400–EFF	Reserved	—	XX	
Z8F022A/Z8F02	1A Devices			
000–1FF	General-Purpose Register File RAM	—	XX	
200–EFF	Reserved	—	XX	
Z8F012A/Z8F01	1A Devices			
000–0FF	General-Purpose Register File RAM	_	XX	
100–EFF	Reserved	—	XX	
Timer 0				
F00	Timer 0 High Byte	T0H	00	<u>90</u>
F01	Timer 0 Low Byte	TOL	01	<u>90</u>
F02	Timer 0 Reload High Byte	TORH	FF	<u>91</u>
F03	Timer 0 Reload Low Byte	TORL	FF	<u>91</u>
F04	Timer 0 PWM High Byte	TOPWMH	00	<u>92</u>
F05	Timer 0 PWM Low Byte	TOPWML	00	<u>92</u>
F06	Timer 0 Control 0	T0CTL0	00	<u>85</u>
F07	Timer 0 Control 1	T0CTL1	00	<u>86</u>
Notoo:				

Table 7. Register File Address Map

Notes: 1. XX = Undefined.

2. Refer to the <u>eZ8</u> CPU <u>Core User Manual (UM0128)</u>.

	-			
Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page
FD9	Port C Control	PCCTL	00	<u>46</u>
FDA	Port C Input Data	PCIN	XX	<u>46</u>
FDB	Port C Output Data	PCOUT	00	<u>46</u>
GPIO Port D				
FDC	Port D Address	PDADDR	00	<u>44</u>
FDD	Port D Control	PDCTL	00	<u>46</u>
FDE	Reserved	—	XX	
FDF	Port D Output Data	PDOUT	00	<u>46</u>
FE0–FEF	Reserved	—	XX	
Watchdog Time	r (WDT)			
FF0	Reset Status (Read-only)	RSTSTAT	X0	<u>29</u>
	Watchdog Timer Control (Write-only)	WDTCTL	N/A	<u>96</u>
FF1	Watchdog Timer Reload Upper Byte	WDTU	00	<u>97</u>
FF2	Watchdog Timer Reload High Byte	WDTH	04	<u>97</u>
FF3	Watchdog Timer Reload Low Byte	WDTL	00	<u>98</u>
FF4–FF5	Reserved	—	XX	
Trim Bit Control				
FF6	Trim Bit Address	TRMADR	00	<u>161</u>
FF7	Trim Bit Data	TRMDR	00	<u>162</u>
Flash Memory C	Controller			
FF8	Flash Control	FCTL	00	<u>155</u>
FF8	Flash Status	FSTAT	00	<u>155</u>
FF9	Flash Page Select	FPS	00	<u>156</u>
	Flash Sector Protect	FPROT	00	<u>157</u>
FFA	Flash Programming Frequency High Byte	FFREQH	00	<u>158</u>
FFB	Flash Programming Frequency Low Byte	FFREQL	00	<u>158</u>
eZ8 CPU				
FFC	Flags	_	XX	See
FFD	Register Pointer	RP	XX	foot-
FFE	Stack Pointer High Byte	SPH	XX	-note 2.
FFF	Stack Pointer Low Byte	SPL	XX	
Notes:				

Table 7. Register File Address Map (Continued)

1. XX = Undefined.

2. Refer to the <u>eZ8</u> CPU Core User Manual (UM0128).

Low-Power Modes

The Z8 Encore! XP F082A Series products contain power-saving features. The highest level of power reduction is provided by the STOP Mode, in which nearly all device functions are powered down. The next lower level of power reduction is provided by the HALT Mode, in which the CPU is powered down.

Further power savings can be implemented by disabling individual peripheral blocks while in Active mode (defined as being in neither STOP nor HALT Mode).

STOP Mode

Executing the eZ8 CPU's STOP instruction places the device into STOP Mode, powering down all peripherals except the Voltage Brown-Out detector, the Low-power Operational Amplifier and the Watchdog Timer. These three blocks may also be disabled for additional power savings. Specifically, the operating characteristics are:

- Primary crystal oscillator and internal precision oscillator are stopped; X_{IN} and X_{OUT} (if previously enabled) are disabled and PA0/PA1 revert to the states programmed by the GPIO registers
- System clock is stopped
- eZ8 CPU is stopped
- Program counter (PC) stops incrementing
- Watchdog Timer's internal RC oscillator continues to operate if enabled by the Oscillator Control Register
- If enabled, the Watchdog Timer logic continues to operate
- If enabled for operation in STOP Mode by the associated Flash option bit, the Voltage Brown-Out protection circuit continues to operate
- Low-power operational amplifier continues to operate if enabled by the Power Control Register
- All other on-chip peripherals are idle

To minimize current in STOP Mode, all GPIO pins that are configured as digital inputs must be driven to one of the supply rails (V_{CC} or GND). Additionally, any GPIOs configured as outputs must also be driven to one of the supply rails. The device can be brought out of STOP Mode using Stop Mode Recovery. For more information about Stop Mode Recovery, see the <u>Reset, Stop Mode Recovery and Low Voltage Detection</u> chapter on page 22.

General-Purpose Input/Output

The Z8 Encore! XP F082A Series products support a maximum of 25 port pins (Ports A–D) for general-purpose input/output (GPIO) operations. Each port contains control and data registers. The GPIO control registers determine data direction, open-drain, output drive current, programmable pull-ups, Stop Mode Recovery functionality and alternate pin functions. Each port pin is individually programmable. In addition, the Port C pins are capable of direct LED drive at programmable drive strengths.

GPIO Port Availability By Device

Table 14 lists the port pins available with each device and package type.

Devices	Package	ADC	Port A	Port B	Port C	Port D	Total I/O
Z8F082ASB, Z8F082APB, Z8F082AQB Z8F042ASB, Z8F042APB, Z8F042AQB Z8F022ASB, Z8F022APB, Z8F022AQB Z8F012ASB, Z8F012APB, Z8F012AQB	8-pin	Yes	[5:0]	No	No	No	6
Z8F081ASB, Z8F081APB, Z8F081AQB Z8F041ASB, Z8F041APB, Z8F041AQB Z8F021ASB, Z8F021APB, Z8F021AQB Z8F011ASB, Z8F011APB, Z8F011AQB	8-pin	No	[5:0]	No	No	No	6
Z8F082APH, Z8F082AHH, Z8F082ASH Z8F042APH, Z8F042AHH, Z8F042ASH Z8F022APH, Z8F022AHH, Z8F022ASH Z8F012APH, Z8F012AHH, Z8F012ASH	20-pin	Yes	[7:0]	[3:0]	[3:0]	[0]	17
Z8F081APH, Z8F081AHH, Z8F081ASH Z8F041APH, Z8F041AHH, Z8F041ASH Z8F021APH, Z8F021AHH, Z8F021ASH Z8F011APH, Z8F011AHH, Z8F011ASH	20-pin	No	[7:0]	[3:0]	[3:0]	[0]	17
Z8F082APJ, Z8F082ASJ, Z8F082AHJ Z8F042APJ, Z8F042ASJ, Z8F042AHJ Z8F022APJ, Z8F022ASJ, Z8F022AHJ Z8F012APJ, Z8F012ASJ, Z8F012AHJ	28-pin	Yes	[7:0]	[5:0]	[7:0]	[0]	23
Z8F081APJ, Z8F081ASJ, Z8F081AHJ Z8F041APJ, Z8F041ASJ, Z8F041AHJ Z8F021APJ, Z8F021ASJ, Z8F021AHJ Z8F011APJ, Z8F011ASJ, Z8F011AHJ	28-pin	No	[7:0]	[7:0]	[7:0]	[0]	25

Table 14. Port Availability by Device and Package Type

Example 1. A poor coding style that can result in lost interrupt requests:

LDX r0, IRQ0 AND r0, MASK LDX IRQ0, r0

To avoid missing interrupts, use the coding style in Example 2 to clear bits in the Interrupt Request 0 Register:

Example 2. A good coding style that avoids lost interrupt requests:

ANDX IRQ0, MASK

Software Interrupt Assertion

Program code can generate interrupts directly. Writing a 1 to the correct bit in the Interrupt Request Register triggers an interrupt (assuming that interrupt is enabled). When the interrupt request is acknowledged by the eZ8 CPU, the bit in the Interrupt Request Register is automatically cleared to 0.

Caution: Zilog recommends not using a coding style to generate software interrupts by setting bits in the Interrupt Request registers. All incoming interrupts received between execution of the first LDX command and the final LDX command are lost. See Example 3, which follows.

Example 3. A poor coding style that can result in lost interrupt requests:

```
LDX r0, IRQ0
OR r0, MASK
LDX IRQ0, r0
```

To avoid missing interrupts, use the coding style in Example 4 to set bits in the Interrupt Request registers:

Example 4. A good coding style that avoids lost interrupt requests:

ORX IRQ0, MASK

Watchdog Timer Interrupt Assertion

The Watchdog Timer interrupt behavior is different from interrupts generated by other sources. The Watchdog Timer continues to assert an interrupt as long as the time-out condition continues. As it operates on a different (and usually slower) clock domain than the rest of the device, the Watchdog Timer continues to assert this interrupt for many system clocks until the counter rolls over.

Table 42. IRQ1	Enable	High Bit	Register	(IRQ1ENH)
----------------	--------	-----------------	----------	-----------

Bit	7	6	5	4	3	2	1	0
Field	PA7VENH	PA6CENH	PA5ENH	PA4ENH	PA3ENH	PA2ENH	PA1ENH	PA0ENH
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address				FC	4H			

Bit	Description
[7] PA7VENH	Port A Bit[7] or LVD Interrupt Request Enable High Bit
[6] PA6CENH	Port A Bit[7] or Comparator Interrupt Request Enable High Bit
[5:0] PAxENH	Port A Bit[x] Interrupt Request Enable High Bit

See the <u>Shared Interrupt Select Register (IRQSS) Register</u> on page 68 for selection of either the LVD or the comparator as the interrupt source.

Table 43.	IRQ1 E	Enable L	ow Bit	Register	(IRQ1ENL)
					·····

Bit	7	6	5	4	3	2	1	0
Field	PA7VENL	PA6CENL	PA5ENL	PA4ENL	PA3ENL	PA2ENL	PA1ENL	PA0ENL
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address				FC	5H			

Bit	Description
[7] PA7VENL	Port A Bit[7] or LVD Interrupt Request Enable Low Bit
[6] PA6CENL	Port A Bit[6] or Comparator Interrupt Request Enable Low Bit
[5:0] PAxENL	Port A Bit[x] Interrupt Request Enable Low Bit

IRQ2 Enable High and Low Bit Registers

Table 44 describes the priority control for IRQ2. The IRQ2 Enable High and Low Bit registers, shown in Tables 44 and 45, form a priority-encoded enabling for interrupts in the Interrupt Request 2 Register.



Operation

The timers are 16-bit up-counters. Minimum time-out delay is set by loading the value 0001H into the Timer Reload High and Low Byte registers and setting the prescale value to 1. Maximum time-out delay is set by loading the value 0000H into the Timer Reload High and Low Byte registers and setting the prescale value to 128. If the Timer reaches FFFFH, the timer rolls over to 0000H and continues counting.

Timer Operating Modes

The timers can be configured to operate in the following modes:

ONE-SHOT Mode

In ONE-SHOT Mode, the timer counts up to the 16-bit reload value stored in the Timer Reload High and Low byte registers. The timer input is the system clock. Upon reaching the reload value, the timer generates an interrupt and the count value in the Timer High and Low Byte registers is reset to 0001H. The timer is automatically disabled and stops counting.

Also, if the Timer Output alternate function is enabled, the Timer Output pin changes state for one system clock cycle (from Low to High or from High to Low) upon timer Reload. If

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Bit Description (Continued)

[6] Timer Input/Output Polarity

TPOL Operation of this bit is a function of the current operating mode of the timer.

ONE-SHOT Mode

When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer Reload.

CONTINUOUS Mode

When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer Reload.

COUNTER Mode

If the timer is enabled the Timer Output signal is complemented after timer reload.

- 0 = Count occurs on the rising edge of the Timer Input signal.
- 1 = Count occurs on the falling edge of the Timer Input signal.

PWM SINGLE OUTPUT Mode

- 0 = Timer Output is forced Low (0) when the timer is disabled. When enabled, the Timer Output is forced High (1) upon PWM count match and forced Low (0) upon reload.
- 1 = Timer Output is forced High (1) when the timer is disabled. When enabled, the Timer Output is forced Low (0) upon PWM count match and forced High (1) upon reload.

CAPTURE Mode

0 = Count is captured on the rising edge of the Timer Input signal.

1 = Count is captured on the falling edge of the Timer Input signal.

COMPARE Mode

When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer Reload.

Bit	Description (Continued)
[2] TDRE	 TDRE—Transmitter Data Register Empty This bit indicates that the UART Transmit Data Register is empty and ready for additional data. Writing to the UART Transmit Data Register resets this bit. 0 = Do not write to the UART Transmit Data Register. 1 = The UART Transmit Data Register is ready to receive an additional byte to be transmitted.
[1] TXE	Transmitter Empty This bit indicates that the Transmit Shift Register is empty and character transmission is finished. 0 = Data is currently transmitting. 1 = Transmission is complete.
[0] CTS	CTS Signal When this bit is read it returns the level of the $\overline{\text{CTS}}$ signal. This signal is active Low.

UART Status 1 Register

This register contains multiprocessor control and status bits.

Bit	7	6	5	4	3	2	1	0
Field	Reserved NEWFRM MPRX							
RESET	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R/W	R/W	R	R
Address	F44H							

Bit	Description
[7:2]	Reserved These bits are reserved and must be programmed to 000000
[1] NEWFRM	 New Frame A status bit denoting the start of a new frame. Reading the UART Receive Data Register resets this bit to 0. 0 = The current byte is not the first data byte of a new frame. 1 = The current byte is the first data byte of a new frame.
[0] MPRX	Multiprocessor Receive Returns the value of the most recent multiprocessor bit received. Reading from the UART Receive Data Register resets this bit to 0.

UART Transmit Data Register

Data bytes written to the UART Transmit Data (UxTXD) Register, shown in Table 67, are shifted out on the TXDx pin. The Write-only UART Transmit Data Register shares a Register File address with the read-only UART Receive Data Register.

For the reserved values, all input switches are disabled to avoid leakage or other undesirable operation. ADC samples taken with reserved bit settings are undefined.

SINGLE-ENDED Mode:

0000 = ANA0 (transimpedance amp output when enabled) 0001 = ANA1 (transimpedance amp inverting input) 0010 = ANA2 (transimpedance amp noninverting input) 0011 = ANA3 0100 = ANA4 0101 = ANA5 0110 = ANA6 0111 = ANA7 1000 = Reserved 1001 = Reserved 1010 = Reserved 1011 = Reserved 1100 = Hold transimpedance input nodes (ANA1 and ANA2) to ground. 1101 = Reserved 1110 = Temperature Sensor.

1111 = Reserved.

DIFFERENTIAL Mode (noninverting input and inverting input respectively):

- 0000 = ANA0 and ANA1 0001 = ANA2 and ANA3 0010 = ANA4 and ANA5 0011 = ANA4 and ANA5 0011 = ANA1 and ANA0 0100 = ANA3 and ANA2 0101 = ANA5 and ANA4 0110 = ANA6 and ANA5 0111 = ANA0 and ANA5 1001 = ANA0 and ANA3 1001 = ANA0 and ANA4 1010 = ANA0 and ANA5 1011 = Reserved 1100 = Reserved 1101 = Reserved 1101 = Reserved1110 = Reserved
- 1111 = Manual Offset Calibration Mode

ADC Control/Status Register 1

The ADC Control/Status Register 1 (ADCCTL1) configures the input buffer stage, enables the threshold interrupts and contains the status of both threshold triggers. It is also used to select the voltage reference configuration.

Bit	7	6	5	4	3	2	1	0
Field	REFSELH		Rese	erved		BUFMODE[2:0]		
RESET	1	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address				F7	1H			
Bit	Des	cription						
[7] REFSELH	Voit In cc the lo REF 00= 01= 10= 11=	Voltage Reference Level Select High Bit In conjunction with the Low bit (REFSELL) in ADC Control Register 0, this determines the level of the internal voltage reference; the following details the effects of {REFSELF REFSELL}; this reference is independent of the Comparator reference. 00= Internal Reference Disabled, reference comes from external pin. 01= Internal Reference set to 1.0V. 10= Internal Reference set to 2.0V (default). 11= Reserved.						
[6:3]	Reserved These bits are reserved and must be programmed to 0000.							
[2:0] Input Buffer Mode Select BUFMODE[2:0] 000 = Single-ended, unbuffered input. 001 = Single-ended, buffered input with unity gain. 010 = Reserved. 011 = Reserved.								

Table 74. ADC Control/Status Register 1 (ADCCTL1)

100 = Differential, unbuffered input.101 = Differential, buffered input with unity gain.

110 = Reserved. 111 = Reserved.

ADC Data High Byte Register

The ADC Data High Byte (ADCD_H) Register contains the upper eight bits of the ADC output. The output is an 13-bit two's complement value. During a single-shot conversion, this value is invalid. Access to the ADC Data High Byte Register is read-only. Reading the ADC Data High Byte Register latches data in the ADC Low Bits Register.

Bit	Description (Continued)
[5:4] OSC_SEL[1:0]	 Oscillator Mode Selection 00 = On-chip oscillator configured for use with external RC networks (<4MHz). 01 = Minimum power for use with very low frequency crystals (32kHz to 1.0MHz). 10 = Medium power for use with medium frequency crystals or ceramic resonators (0.5MHz to 5.0MHz). 11 = Maximum power for use with high frequency crystals (5.0MHz to 20.0MHz). This setting is the default for unprogrammed (erased) Flash.
[3] VBO_AO	 Voltage Brown-Out Protection Always On 0 = Voltage Brown-Out Protection can be disabled in STOP Mode to reduce total power consumption. For the block to be disabled, the power control register bit must also be written (see the <u>Power Control Register Definitions</u> section on page 33). 1 = Voltage Brown-Out Protection is always enabled including during STOP Mode. This setting is the default for unprogrammed (erased) Flash.
[2] FRP	 Flash Read Protect 0 = User program code is inaccessible. Limited control features are available through the On-Chip Debugger. 1 = User program code is accessible. All On-Chip Debugger commands are enabled. This setting is the default for unprogrammed (erased) Flash.
[1]	Reserved This bit is reserved and must be programmed to 1.
[0] FWP	 Flash Write Protect This Option Bit provides Flash Program Memory protection: 0 = Programming and erasure disabled for all of Flash Program Memory. Programming, Page Erase and Mass Erase through User Code is disabled. Mass Erase is available using the On-Chip Debugger. 1 = Programming, Page Erase and Mass Erase are enabled for all of Flash program memory.

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LVD_TRIM	LVD Threshold (V) Typical	Description
00000	3.60	Maximum LVD threshold
00001	3.55	
00010	3.50	
00011	3.45	
00100	3.40	
00101	3.35	
00110	3.30	
00111	3.25	
01000	3.20	
01001	3.15	
01010	3.10	Default on Reset
01011	3.05	
01100	3.00	
01101	2.95	
01110	2.90	
01111	2.85	
10000	2.80	
10001	2.75	
10010	2.70	
10011	2.70	
to	to	
11111	1.65	Minimum LVD threshold

Table 94. LVD Trim Values

Trim Bit Address 0004H

Table 95. Trim Option Bits at 0004H

Bit	7	6	5	4	3	2	1	0		
Field	Reserved									
RESET	U	U	U	U	U	U	U	U		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Address	Information Page Memory 0024H									
Note: U =	Note: U = Unchanged by Reset. R/W = Read/Write.									

Bit Description

[7:0] Reserved

These bits are reserved; altering this register may result in incorrect device operation.

Zilog Calibration Data

This section briefly describes the features of the following Flash option bit calibration registers.

ADC Calibration Data: see page 169

Temperature Sensor Calibration Data: see page 171

Watchdog Timer Calibration Data: see page 172

Serialization Data: see page 173

Randomized Lot Identifier: see page 174

ADC Calibration Data

Table 96. ADC Calibration Bits

Bit	7	6	5	4	3	2	1	0	
Field	ADC_CAL								
RESET	U	U	U	U	U	U	U	U	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address	Information Page Memory 0060H–007DH								
Noto: II -	Note: U. Unshanged by Depart DAM								

Note: U = Unchanged by Reset. R/W = Read/Write.

Bit Description

[7:0] Analog-to-Digital Converter Calibration Values
 ADC_CAL Contains factory-calibrated values for ADC gain and offset compensation. Each of the ten supported modes has one byte of offset calibration and two bytes of gain calibration. These values are read by the software to compensate ADC measurements as described in the Software Compensation Procedure Using Factory Calibration Data section on page 129. The location of each calibration byte is provided in Table 97.

Info Page	Memory			
Address	Address	Compensation Usage	ADC Mode	Reference Type
60	FE60	Offset	Single-Ended Unbuffered	Internal 2.0 V
08	FE08	Gain High Byte	Single-Ended Unbuffered	Internal 2.0 V
09	FE09	Gain Low Byte	Single-Ended Unbuffered	Internal 2.0 V
63	FE63	Offset	Single-Ended Unbuffered	Internal 1.0 V
0A	FE0A	Gain High Byte	Single-Ended Unbuffered	Internal 1.0 V
0B	FE0B	Gain Low Byte	Single-Ended Unbuffered	Internal 1.0 V
66	FE66	Offset	Single-Ended Unbuffered	External 2.0 V
0C	FE0C	Gain High Byte	Single-Ended Unbuffered	External 2.0 V
0D	FE0D	Gain Low Byte	Single-Ended Unbuffered	External 2.0 V
69	FE69	Offset	Single-Ended 1x Buffered	Internal 2.0 V
0E	FE0E	Gain High Byte	Single-Ended 1x Buffered	Internal 2.0 V
0F	FE0F	Gain Low Byte	Single-Ended 1x Buffered	Internal 2.0 V
6C	FE6C	Offset	Single-Ended 1x Buffered	External 2.0 V
10	FE10	Gain High Byte	Single-Ended 1x Buffered	External 2.0 V
11	FE11	Gain Low Byte	Single-Ended 1x Buffered	External 2.0 V
6F	FE6F	Offset	Differential Unbuffered	Internal 2.0 V

Table 97. ADC Calibration Data Location

Nonvolatile Data Storage

The Z8 Encore! XP F082A Series devices contain a nonvolatile data storage (NVDS) element of up to 128 bytes. This memory can perform over 100,000 write cycles.

Operation

The NVDS is implemented by special purpose Zilog software stored in areas of program memory, which are not user-accessible. These special-purpose routines use the Flash memory to store the data. The routines incorporate a dynamic addressing scheme to maximize the write/erase endurance of the Flash.

Note: Different members of the Z8 Encore! XP F082A Series feature multiple NVDS array sizes; see the <u>Part Selection Guide</u> section on page 2 for details. Devices containing 8KB of Flash memory do not include the NVDS feature.

NVDS Code Interface

Two routines are required to access the NVDS: a write routine and a read routine. Both of these routines are accessed with a CALL instruction to a predefined address outside of the user-accessible program memory. Both the NVDS address and data are single-byte values. Because these routines disturb the working register set, user code must ensure that any required working register values are preserved by pushing them onto the stack or by changing the working register pointer just prior to NVDS execution.

During both read and write accesses to the NVDS, interrupt service is NOT disabled. Any interrupts that occur during the NVDS execution must take care not to disturb the working register and existing stack contents or else the array may become corrupted. Disabling interrupts before executing NVDS operations is recommended.

Use of the NVDS requires 15 bytes of available stack space. Also, the contents of the working register set are overwritten.

For correct NVDS operation, the Flash Frequency registers must be programmed based on the system clock frequency (see **the** <u>Flash Operation Timing Using the Flash Frequency</u> <u>Registers</u> **section on page 149**).

Debug Command	Command Byte	Enabled when Not in DEBUG Mode?	Disabled by Flash Read Protect Option Bit
Write Program Counter	06H	_	Disabled.
Read Program Counter	07H	_	Disabled.
Write Register	08H	_	Only writes of the Flash Memory Control registers are allowed. Additionally, only the Mass Erase command is allowed to be written to the Flash Control Register.
Read Register	09H	-	Disabled.
Write Program Memory	0AH	-	Disabled.
Read Program Memory	0BH	-	Disabled.
Write Data Memory	0CH	-	Yes.
Read Data Memory	0DH	-	-
Read Program Memory CRC	0EH	-	-
Reserved	0FH	-	-
Step Instruction	10H	-	Disabled.
Stuff Instruction	11H	-	Disabled.
Execute Instruction	12H	_	Disabled.
Reserved	13H–FFH	_	-

Table 109. Debug Command Enable/Disable (Continued)

In the list of OCD commands that follows, data and commands sent from the host to the On-Chip Debugger are identified by DBG \leftarrow Command/Data. Data sent from the On-Chip Debugger back to the host is identified by DBG \rightarrow Data.

Read OCD Revision (00H). The Read OCD Revision command determines the version of the On-Chip Debugger. If OCD commands are added, removed, or changed, this revision number changes.

```
DBG \leftarrow 00H
DBG \rightarrow OCDRev[15:8] (Major revision number)
DBG \rightarrow OCDRev[7:0] (Minor revision number)
```

Read OCD Status Register (02H). The Read OCD Status Register command reads the OCDSTAT Register.

DBG \leftarrow 02H DBG \rightarrow OCDSTAT[7:0]

Read Runtime Counter (03H). The Runtime Counter counts system clock cycles in between Breakpoints. The 16-bit Runtime Counter counts up from 0000H and stops at the maximum count of FFFFH. The Runtime Counter is overwritten during the Write Memory,

Read Register (09H). The Read Register command reads data from the Register File. Data can be read 1–256 bytes at a time (256 bytes can be read by setting size to 0). If the device is not in DEBUG Mode or if the Flash Read Protect Option bit is enabled, this command returns FFH for all the data values.

DBG \leftarrow 09H DBG \leftarrow {4'h0,Register Address[11:8] DBG \leftarrow Register Address[7:0] DBG \leftarrow Size[7:0] DBG \rightarrow 1-256 data bytes

Write Program Memory (0AH). The Write Program Memory command writes data to Program Memory. This command is equivalent to the LDC and LDCI instructions. Data can be written 1–65536 bytes at a time (65536 bytes can be written by setting size to 0). The on-chip Flash Controller must be written to and unlocked for the programming operation to occur. If the Flash Controller is not unlocked, the data is discarded. If the device is not in DEBUG Mode or if the Flash Read Protect Option bit is enabled, the data is discarded.

```
DBG \leftarrow 0AH
DBG \leftarrow Program Memory Address[15:8]
DBG \leftarrow Program Memory Address[7:0]
DBG \leftarrow Size[15:8]
DBG \leftarrow Size[7:0]
DBG \leftarrow 1-65536 data bytes
```

Read Program Memory (0BH). The Read Program Memory command reads data from Program Memory. This command is equivalent to the LDC and LDCI instructions. Data can be read 1–65536 bytes at a time (65536 bytes can be read by setting size to 0). If the device is not in DEBUG Mode or if the Flash Read Protect Option bit is enabled, this command returns FFH for the data.

```
DBG \leftarrow 0BH

DBG \leftarrow Program Memory Address[15:8]

DBG \leftarrow Program Memory Address[7:0]

DBG \leftarrow Size[15:8]

DBG \leftarrow Size[7:0]

DBG \rightarrow 1-65536 data bytes
```

Write Data Memory (0CH). The Write Data Memory command writes data to Data Memory. This command is equivalent to the LDE and LDEI instructions. Data can be written 1–65536 bytes at a time (65536 bytes can be written by setting size to 0). If the device is not in DEBUG Mode or if the Flash Read Protect Option bit is enabled, the data is discarded.

DBG \leftarrow 0CH DBG \leftarrow Data Memory Address[15:8] DBG \leftarrow Data Memory Address[7:0]

Packaging

Zilog's Product Line of MCUs includes the Z8F011A, Z8F012A, Z8F021A, Z8F022A, Z8F041A, Z8F042A, Z8F081A and Z8F082A devices, which are available in the following packages:

- 8-pin Plastic Dual-Inline Package (PDIP)
- 8-Pin Quad Flat No-Lead Package (QFN)/MLF-S¹
- 8-pin Small Outline Integrated Circuit Package (SOIC)
- 20-pin Small Outline Integrated Circuit Package (SOIC)
- 20-pin Small Shrink Outline Package (SSOP)
- 20-pin Plastic Dual-Inline Package (PDIP)
- 28-pin Small Outline Integrated Circuit Package (SOIC)
- 28-pin Small Shrink Outline Package (SSOP)
- 28-pin Plastic Dual-Inline Package (PDIP)

Current diagrams for each of these packages are published in Zilog's <u>Packaging Product</u> <u>Specification (PS0072)</u>, which is available free for download from the Zilog website.

^{1.} The footprint of the QFN)/MLF-S package is identical to that of the 8-pin SOIC package, but with a lower profile.