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Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, Temp Sensor, WDT
Number of I/O	23
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f042asj020eg

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Table 5. Z8 Encore! XP F082A Series Program Memory Maps (Continued)

Program Memory Address (Hex)	Function
0002–0003	Reset Vector
0004–0005	WDT Interrupt Vector
0006–0007	Illegal Instruction Trap
0008–0037	Interrupt Vectors*
0038–0039	Reserved
003A–003D	Oscillator Fail Trap Vectors
003E–03FF	Program Memory

Note: *See Table 32 on page 56 for a list of the interrupt vectors.

Data Memory

The Z8 Encore! XP F082A Series does not use the eZ8 CPU's 64 KB Data Memory address space.

Flash Information Area

Table 6 describes the Z8 Encore! XP F082A Series Flash Information Area. This 128B Information Area is accessed by setting bit 7 of the Flash Page Select Register to 1. When access is enabled, the Flash Information Area is mapped into the Program Memory and overlays the 128 bytes at addresses FE00H to FF7FH. When the Information Area access is enabled, all reads from these Program Memory addresses return the Information Area data rather than the Program Memory data. Access to the Flash Information Area is read-only.

Table 6. Z8 Encore! XP F082A Series Flash Memory Information Area Map

Program Memory Address (Hex)	Function
FE00–FE3F	Zilog Option Bits/Calibration Data
FE40–FE53	Part Number 20-character ASCII alphanumeric code Left-justified and filled with FFH
FE54–FE5F	Reserved
FE60–FE7F	Zilog Calibration Data
FE80–FFFF	Reserved

without initiating an interrupt (if enabled for that pin).

Stop Mode Recovery Using the External $\overline{\text{RESET}}$ Pin

When the Z8 Encore! XP F082A Series device is in STOP Mode and the external $\overline{\text{RESET}}$ pin is driven Low, a system reset occurs. Because of a glitch filter operating on the $\overline{\text{RESET}}$ pin, the Low pulse must be greater than the minimum width specified, or it is ignored. See the [Electrical Characteristics](#) chapter on page 226 for details.

Low Voltage Detection

In addition to the Voltage Brown-Out (VBO) Reset described above, it is also possible to generate an interrupt when the supply voltage drops below a user-selected value. For details about configuring the Low Voltage Detection (LVD) and the threshold levels available, see the [Trim Option Bits at Address 0003H \(TLVD\) Register](#) on page 166. The LVD function is available on the 8-pin product versions only.

When the supply voltage drops below the LVD threshold, the LVD bit of the Reset Status (RSTSTAT) Register is set to one. This bit remains one until the low-voltage condition goes away. Reading or writing this bit does not clear it. The LVD circuit can also generate an interrupt when so enabled, see the [GPIO Mode Interrupt Controller](#) chapter on page 55. The LVD bit is not latched; therefore, enabling the interrupt is the only way to guarantee detection of a transient low voltage event.

The LVD functionality depends on circuitry shared with the VBO block; therefore, disabling the VBO also disables the LVD.

Reset Register Definitions

The following sections define the Reset registers.

Reset Status Register

The read-only Reset Status (RSTSTAT) Register, shown in Table 11, indicates the source of the most recent Reset event, indicates a Stop Mode Recovery event and indicates a Watchdog Timer time-out. Reading this register resets the upper four bits to 0. This register shares its address with the write-only Watchdog Timer Control Register.

Table 12 lists the bit settings for Reset and Stop Mode Recovery events.

Architecture

Figure 7 displays a simplified block diagram of a GPIO port pin. In this figure, the ability to accommodate alternate functions and variable port current drive strength is not displayed.

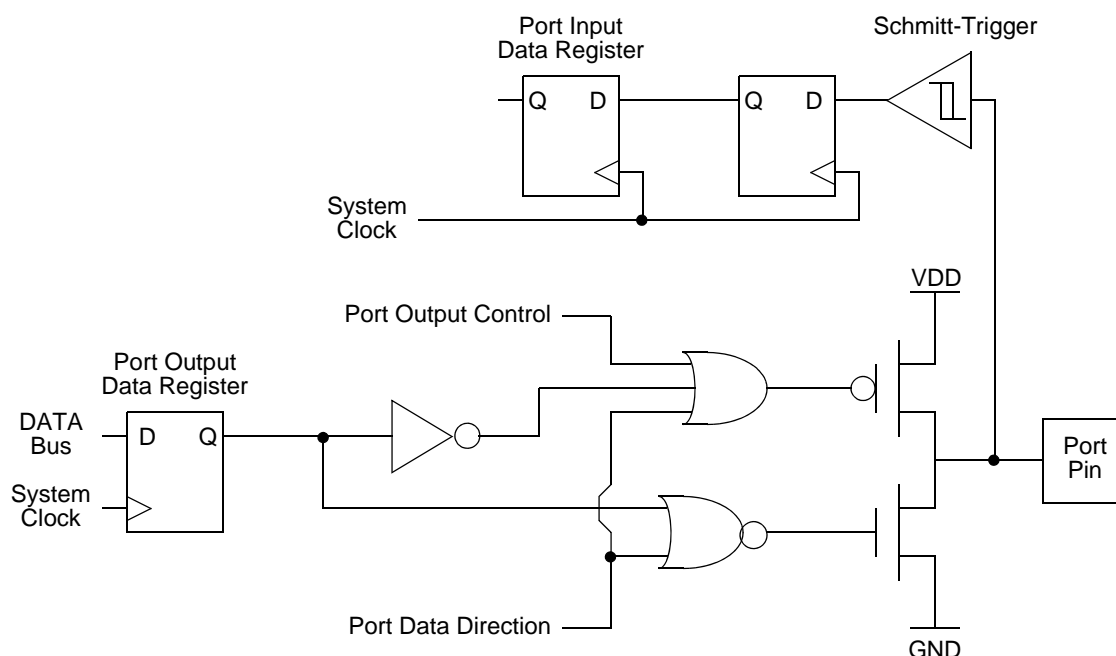


Figure 7. GPIO Port Pin Block Diagram

GPIO Alternate Functions

Many of the GPIO port pins can be used for general-purpose I/O and access to on-chip peripheral functions such as the timers and serial communication devices. The Port A–D Alternate Function subregisters configure these pins for either General-Purpose I/O or alternate function operation. When a pin is configured for alternate function, control of the port pin direction (input/output) is passed from the Port A–D Data Direction registers to the alternate function assigned to this pin. [Table 15](#) on page 40 lists the alternate functions possible with each port pin. For those pins with more one alternate function, the alternate function is defined through Alternate Function Sets subregisters AFS1 and AFS2.

The crystal oscillator functionality is not controlled by the GPIO block. When the crystal oscillator is enabled in the oscillator control block, the GPIO functionality of PA0 and PA1 is overridden. In that case, those pins function as input and output for the crystal oscillator.

Table 15. Port Alternate Function Mapping (Non 8-Pin Parts) (Continued)

Port	Pin	Mnemonic	Alternate Function Description	Alternate Function Set Register AFS1
Port C ⁵	PC0	Reserved		AFS1[0]: 0
		ANA4/CINP	ADC or Comparator Input	AFS1[0]: 1
	PC1	Reserved		AFS1[1]: 0
		ANA5/CINN	ADC or Comparator Input	AFS1[1]: 1
	PC2	Reserved		AFS1[2]: 0
		ANA6/V _{REF} ⁴	ADC Analog Input or ADC Voltage Reference	AFS1[2]: 1
	PC3	COUT	Comparator Output	AFS1[3]: 0
		Reserved		AFS1[3]: 1
	PC4	Reserved		AFS1[4]: 0
				AFS1[4]: 1
	PC5	Reserved		AFS1[5]: 0
				AFS1[5]: 1
	PC6	Reserved		AFS1[6]: 0
				AFS1[6]: 1
	PC7	Reserved		AFS1[7]: 0
				AFS1[7]: 1
Port D ⁶	PD0	RESET	External Reset	N/A

Notes:

1. Because there is only a single alternate function for each Port A pin, the Alternate Function Set registers are not implemented for Port A. Enabling alternate function selections automatically enables the associated alternate function. See the [Port A–D Alternate Function Subregisters \(PxAF\)](#) section on page 47 for details.
2. Whether PA0/PA6 takes on the timer input or timer output complement function depends on the timer configuration. See the [Timer Pin Signal Operation](#) section on page 84 for details.
3. Because there are at most two choices of alternate function for any pin of Port B, the Alternate Function Set Register AFS2 is not used to select the function. Alternate function selection must also be enabled. See the [Port A–D Alternate Function Subregisters \(PxAF\)](#) section on page 47 for details.
4. V_{REF} is available on PB5 in 28-pin products and on PC2 in 20-pin parts.
5. Because there are at most two choices of alternate function for any pin of Port C, the Alternate Function Set Register AFS2 is not used to select the function. Alternate function selection must also be enabled. See the [Port A–D Alternate Function Subregisters \(PxAF\)](#) section on page 47 for details.
6. Because there is only a single alternate function for the Port PD0 pin, the Alternate Function Set registers are not implemented for Port D. Enabling alternate function selections automatically enables the associated alternate function. See the [Port A–D Alternate Function Subregisters \(PxAF\)](#) section on page 47 for details.

Table 46. IRQ2 Enable Low Bit Register (IRQ2ENL)

Bit	7	6	5	4	3	2	1	0
Field	Reserved				C3ENL	C2ENL	C1ENL	C0ENL
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC8H							

Bit	Description
[7:4]	Reserved These bits are reserved and must be programmed to 0000.
[3] C3ENL	Port C3 Interrupt Request Enable Low Bit
[2] C2ENL	Port C2 Interrupt Request Enable Low Bit
[1] C1ENL	Port C1 Interrupt Request Enable Low Bit
[0] C0ENL	Port C0 Interrupt Request Enable Low Bit

Interrupt Edge Select Register

The Interrupt Edge Select (IRQES) Register, shown in Table 47, determines whether an interrupt is generated for the rising edge or falling edge on the selected GPIO Port A input pin.

Table 47. Interrupt Edge Select Register (IRQES)

Bit	7	6	5	4	3	2	1	0
Field	IES7	IES6	IES5	IES4	IES3	IES2	IES1	IES0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FCDH							

Bit	Description
[7:0] IESx	Interrupt Edge Select x 0 = An interrupt request is generated on the falling edge of the PAX input. 1 = An interrupt request is generated on the rising edge of the PAX input.
Note: x indicates the specific GPIO port pin number (0–7).	

Bit	Description (Continued)
[6:5] TICONFIG	Timer Interrupt Configuration This field configures timer interrupt definition. 0x = Timer Interrupt occurs on all defined Reload, Compare and Input Events. 10 = Timer Interrupt only on defined Input Capture/Deassertion Events. 11 = Timer Interrupt only on defined Reload/Compare Events.
[4]	Reserved This bit is reserved and must be programmed to 0.
[3:1] PWMD	PWM Delay Value This field is a programmable delay to control the number of system clock cycles delay before the Timer Output and the Timer Output Complement are forced to their active state. 000 = No delay. 001 = 2 cycles delay. 010 = 4 cycles delay. 011 = 8 cycles delay. 100 = 16 cycles delay. 101 = 32 cycles delay. 110 = 64 cycles delay. 111 = 128 cycles delay.
[0] INPCAP	Input Capture Event This bit indicates if the most recent timer interrupt is caused by a Timer Input Capture Event. 0 = Previous timer interrupt is not a result of Timer Input Capture Event. 1 = Previous timer interrupt is a result of Timer Input Capture Event.

Timer 0–1 Control Register 1

The Timer 0–1 Control (TxCTL1) registers, shown in Table 51, enable and disable the timers, set the prescaler value and determine the timer operating mode.

Table 51. Timer 0–1 Control Register 1 (TxCTL1)

Bit	7	6	5	4	3	2	1	0
Field	TEN	TPOL	PRES			TMODE		
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F07H, F0FH							

Bit	Description
[7] TEN	Timer Enable 0 = Timer is disabled. 1 = Timer enabled to count.

Bit	Description (Continued)
[6] TPOL	<p>Timer Input/Output Polarity Operation of this bit is a function of the current operating mode of the timer.</p> <p>ONE-SHOT Mode When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer Reload.</p> <p>CONTINUOUS Mode When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer Reload.</p> <p>COUNTER Mode If the timer is enabled the Timer Output signal is complemented after timer reload. 0 = Count occurs on the rising edge of the Timer Input signal. 1 = Count occurs on the falling edge of the Timer Input signal.</p> <p>PWM SINGLE OUTPUT Mode 0 = Timer Output is forced Low (0) when the timer is disabled. When enabled, the Timer Output is forced High (1) upon PWM count match and forced Low (0) upon reload. 1 = Timer Output is forced High (1) when the timer is disabled. When enabled, the Timer Output is forced Low (0) upon PWM count match and forced High (1) upon reload.</p> <p>CAPTURE Mode 0 = Count is captured on the rising edge of the Timer Input signal. 1 = Count is captured on the falling edge of the Timer Input signal.</p> <p>COMPARE Mode When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer Reload.</p>

Watchdog Timer Refresh

When first enabled, the Watchdog Timer is loaded with the value in the Watchdog Timer Reload registers. The Watchdog Timer counts down to 000000H unless a WDT instruction is executed by the eZ8 CPU. Execution of the WDT instruction causes the downcounter to be reloaded with the WDT reload value stored in the Watchdog Timer Reload registers. Counting resumes following the reload operation.

When the Z8 Encore! XP F082A Series devices are operating in DEBUG Mode (using the on-chip debugger), the Watchdog Timer is continuously refreshed to prevent any Watchdog Timer time-outs.

Watchdog Timer Time-Out Response

The Watchdog Timer times out when the counter reaches 000000H. A time-out of the Watchdog Timer generates either an interrupt or a system reset. The WDT_RES Flash option bit determines the time-out response of the Watchdog Timer. For information about programming the WDT_RES Flash option bit, see the [Flash Option Bits](#) chapter on page 159.

WDT Interrupt in Normal Operation

If configured to generate an interrupt when a time-out occurs, the Watchdog Timer issues an interrupt request to the interrupt controller and sets the WDT status bit in the Reset Status (RSTSTAT) Register; see the [Reset Status Register](#) on page 29. If interrupts are enabled, the eZ8 CPU responds to the interrupt request by fetching the Watchdog Timer interrupt vector and executing code from the vector address. After time-out and interrupt generation, the Watchdog Timer counter rolls over to its maximum value of FFFFFH and continues counting. The Watchdog Timer counter is not automatically returned to its reload value.

The Reset Status (RSTSTAT) Register must be read before clearing the WDT interrupt. This read clears the WDT time-out Flag and prevents further WDT interrupts from immediately occurring.

WDT Interrupt in STOP Mode

If configured to generate an interrupt when a time-out occurs and the Z8 Encore! XP F082A Series devices are in STOP Mode, the Watchdog Timer automatically initiates a Stop Mode Recovery and generates an interrupt request. Both the WDT status bit and the STOP bit in the Reset Status (RSTSTAT) Register are set to 1 following a WDT time-out in STOP Mode. For more information about Stop Mode Recovery, see the [Reset, Stop Mode Recovery and Low Voltage Detection](#) chapter on page 22.

If interrupts are enabled, following completion of the Stop Mode Recovery the eZ8 CPU responds to the interrupt request by fetching the Watchdog Timer interrupt vector and executing code from the vector address.

UART Interrupts

The UART features separate interrupts for the transmitter and the receiver. In addition, when the UART primary functionality is disabled, the Baud Rate Generator can also function as a basic timer with interrupt capability.

Transmitter Interrupts

The transmitter generates a single interrupt when the Transmit Data Register Empty bit (TDRE) is set to 1. This indicates that the transmitter is ready to accept new data for transmission. The TDRE interrupt occurs after the Transmit Shift Register has shifted the first bit of data out. The Transmit Data Register can now be written with the next character to send. This action provides 7 bit periods of latency to load the Transmit Data Register before the Transmit Shift Register completes shifting the current character. Writing to the UART Transmit Data Register clears the TDRE bit to 0.

Receiver Interrupts

The receiver generates an interrupt when any of the following actions occur:

- A data byte is received and is available in the UART Receive Data Register. This interrupt can be disabled independently of the other receiver interrupt sources. The received data interrupt occurs after the receive character has been received and placed in the Receive Data Register. To avoid an overrun error, software must respond to this received data available condition before the next character is completely received.

► **Note:** In MULTIPROCESSOR Mode ($MPEN = 1$), the receive data interrupts are dependent on the multiprocessor configuration and the most recent address byte.

- A break is received.
- An overrun is detected.
- A data framing error is detected.

UART Overrun Errors

When an overrun error condition occurs the UART prevents overwriting of the valid data currently in the Receive Data Register. The Break Detect and Overrun status bits are not displayed until after the valid data has been read.

After the valid data has been read, the UART Status 0 Register is updated to indicate the overrun condition (and Break Detect, if applicable). The RDA bit is set to 1 to indicate that the Receive Data Register contains a data byte. However, because the overrun error occurred, this byte may not contain valid data and must be ignored. The BRKD bit indicates if the overrun was caused by a break condition on the line. After reading the status

#3	#3	#3	#3
----	----	----	----

4. Round the result and discard the least significant two bytes (equivalent to dividing by 2^{16}).

#3	#3	#3	#3
----	----	----	----

–

0x00	0x00	0x80	0x00
------	------	------	------

=

#4 MSB	#4 LSB
--------	--------

5. Determine the sign of the gain correction factor using the sign bits from Step 2. If the offset-corrected ADC value *and* the gain correction word both have the same sign, then the factor is positive and remains unchanged. If they have differing signs, then the factor is negative and must be multiplied by –1.

#5 MSB	#5 LSB
--------	--------

6. Add the gain correction factor to the original offset corrected value.

#5 MSB	#5 LSB
--------	--------

+

#1 MSB	#1 LSB
--------	--------

=

#6 MSB	#6 LSB
--------	--------

7. Shift the result to the right, using the sign bit determined in Step 1, to allow for the detection of computational overflow.

S →	#6 MSB	#6 LSB
-----	--------	--------

When selecting a new clock source, the system clock oscillator failure detection circuitry and the Watchdog Timer oscillator failure circuitry must be disabled. If SOFEN and WOFEN are not disabled prior to a clock switch-over, it is possible to generate an interrupt for a failure of either oscillator. The Failure detection circuitry can be enabled any-time after a successful write of OSCSEL in the OSCCTL Register.

The internal precision oscillator is enabled by default. If the user code changes to a different oscillator, it may be appropriate to disable the IPO for power savings. Disabling the IPO does not occur automatically.

Clock Failure Detection and Recovery

Should an oscillator or timer fail, there are methods of recovery, as this section describes.

System Clock Oscillator Failure

The Z8F04xA family devices can generate nonmaskable interrupt-like events when the primary oscillator fails. To maintain system function in this situation, the clock failure recovery circuitry automatically forces the Watchdog Timer oscillator to drive the system clock. The Watchdog Timer oscillator must be enabled to allow the recovery. Although this oscillator runs at a much slower speed than the original system clock, the CPU continues to operate, allowing execution of a clock failure vector and software routines that either remedy the oscillator failure or issue a failure alert. This automatic switch-over is not available if the Watchdog Timer is selected as the system clock oscillator. It is also unavailable if the Watchdog Timer oscillator is disabled, though it is not necessary to enable the Watchdog Timer reset function (see the [Watchdog Timer](#) chapter on page 93).

The primary oscillator failure detection circuitry asserts if the system clock frequency drops below 1 kHz \pm 50%. If an external signal is selected as the system oscillator, it is possible that a very slow but nonfailing clock can generate a failure condition. Under these conditions, do not enable the clock failure circuitry (SOFEN must be deasserted in the OSCCTL Register).

Watchdog Timer Failure

In the event of a Watchdog Timer oscillator failure, a similar nonmaskable interrupt-like event is issued. This event does not trigger an attendant clock switch-over, but alerts the CPU of the failure. After a Watchdog Timer failure, it is no longer possible to detect a primary oscillator failure. The failure detection circuitry does not function if the Watchdog Timer is used as the system clock oscillator or if the Watchdog Timer oscillator has been disabled. For either of these cases, it is necessary to disable the detection circuitry by deasserting the WDFEN bit of the OSCCTL Register.

The Watchdog Timer oscillator failure detection circuit counts system clocks while looking for a Watchdog Timer clock. The logic counts 8004 system clock cycles before determining that a failure has occurred. The system clock rate determines the speed at which

Crystal Oscillator

The products in the Z8 Encore! XP F082A Series contain an on-chip crystal oscillator for use with external crystals with 32kHz to 20MHz frequencies. In addition, the oscillator supports external RC networks with oscillation frequencies up to 4MHz or ceramic resonators with frequencies up to 8MHz. The on-chip crystal oscillator can be used to generate the primary system clock for the internal eZ8 CPU and the majority of the on-chip peripherals. Alternatively, the X_{IN} input pin can also accept a CMOS-level clock input signal (32kHz–20MHz). If an external clock generator is used, the X_{OUT} pin must be left unconnected. The Z8 Encore! XP F082A Series products do not contain an internal clock divider. The frequency of the signal on the X_{IN} input pin determines the frequency of the system clock.

► **Note:** Although the X_{IN} pin can be used as an input for an external clock generator, the CLKIN pin is better suited for such use (see the [System Clock Selection](#) section on page 193).

Operating Modes

The Z8 Encore! XP F082A Series products support four oscillator modes:

- Minimum power for use with very low frequency crystals (32kHz–1 MHz)
- Medium power for use with medium frequency crystals or ceramic resonators (0.5 MHz to 8 MHz)
- Maximum power for use with high frequency crystals (8 MHz to 20 MHz)
- On-chip oscillator configured for use with external RC networks (<4 MHz)

The oscillator mode is selected via user-programmable Flash option bits. See [the Flash Option Bits](#) chapter on page 159 for information.

Crystal Oscillator Operation

The XTLDIS Flash option bit controls whether the crystal oscillator is enabled during reset. The crystal may later be disabled after reset if a new oscillator has been selected as the system clock. If the crystal is manually enabled after reset through the OSCCTL Register, the user code must wait at least 1000 crystal oscillator cycles for the crystal to stabilize. After this, the crystal oscillator may be selected as the system clock.

Oscillator Operation with an External RC Network

Figure 28 displays a recommended configuration for connection with an external resistor-capacitor (RC) network.

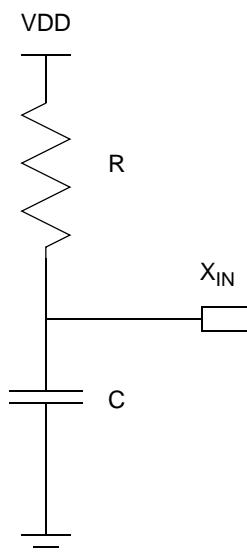


Figure 28. Connecting the On-Chip Oscillator to an External RC Network

An external resistance value of 45 k Ω is recommended for oscillator operation with an external RC network. The minimum resistance value to ensure operation is 40 k Ω . The typical oscillator frequency can be estimated from the values of the resistor (R in k Ω) and capacitor (C in pF) elements using the following equation:

$$\text{Oscillator Frequency (kHz)} = \frac{1 \times 10^6}{(0.4 \times R \times C) + (4 \times C)}$$

Figure 29 displays the typical (3.3 V and 25°C) oscillator frequency as a function of the capacitor (C , in pF) employed in the RC network assuming a 45 K Ω external resistor. For very small values of C , the parasitic capacitance of the oscillator X_{IN} pin and the printed circuit board must be included in the estimation of the oscillator frequency.

It is possible to operate the RC oscillator using only the parasitic capacitance of the package and printed circuit board. To minimize sensitivity to external parasitics, external capacitance values in excess of 20 pF are recommended.

Internal Precision Oscillator

The internal precision oscillator (IPO) is designed for use without external components. You can either manually trim the oscillator for a nonstandard frequency or use the automatic factory-trimmed version to achieve a 5.53MHz frequency. IPO features include:

- On-chip RC oscillator that does not require external components
- Output frequency of either 5.53MHz or 32.8kHz (contains both a fast and a slow mode)
- Trimmed through Flash option bits with user override
- Elimination of crystals or ceramic resonators in applications where very high timing accuracy is not required

Operation

An 8-bit trimming register, incorporated into the design, compensates for absolute variation of oscillator frequency. Once trimmed the oscillator frequency is stable and does not require subsequent calibration. Trimming is performed during manufacturing and is not necessary for you to repeat unless a frequency other than 5.53MHz (fast mode) or 32.8kHz (slow mode) is required. This trimming is done at +30°C and a supply voltage of 3.3V, so accuracy of this operating point is optimal.

If not used, the IPO can be disabled by the Oscillator Control Register (see the [Oscillator Control Register Definitions](#) section on page 196).

By default, the oscillator frequency is set by the factory trim value stored in the write-protected Flash information page. However, the user code can override these trim values as described in the [Trim Bit Address Space](#) section on page 165.

Select one of two frequencies for the oscillator (5.53MHz and 32.8kHz) using the OSC-SEL bits in the the [Oscillator Control](#) chapter on page 193.

Table 128. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode		Opcode(s) (Hex)	Flags						Fetch Cycle s	Instr. Cycle s
		dst	src		C	Z	S	V	D	H		
AND dst, src	dst ← dst AND src	r	r	52	–	*	*	0	–	–	2	3
		r	lr	53							2	4
		R	R	54							3	3
		R	IR	55							3	4
		R	IM	56							3	3
		IR	IM	57							3	4
ANDX dst, src	dst ← dst AND src	ER	ER	58	–	*	*	0	–	–	4	3
		ER	IM	59							4	3
ATM	Block all interrupt and DMA requests during execution of the next 3 instructions			2F	–	–	–	–	–	–	1	2
BCLR bit, dst	dst[bit] ← 0	r		E2	–	–	–	–	–	–	2	2
BIT p, bit, dst	dst[bit] ← p	r		E2	–	–	–	–	–	–	2	2
BRK	Debugger Break			00	–	–	–	–	–	–	1	1
BSET bit, dst	dst[bit] ← 1	r		E2	–	–	–	–	–	–	2	2
BSWAP dst	dst[7:0] ← dst[0:7]	R		D5	X	*	*	0	–	–	2	2
BTJ p, bit, src, dst	if src[bit] = p PC ← PC + X		r	F6	–	–	–	–	–	–	3	3
			lr	F7							3	4
BTJNZ bit, src, dst	if src[bit] = 1 PC ← PC + X		r	F6	–	–	–	–	–	–	3	3
			lr	F7							3	4
BTJZ bit, src, dst	if src[bit] = 0 PC ← PC + X		r	F6	–	–	–	–	–	–	3	3
			lr	F7							3	4

Note: Flags Notation:

* = Value is a function of the result of the operation.

– = Unaffected.

X = Undefined.

0 = Reset to 0.

1 = Set to 1.

Table 128. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode		Opcode(s) (Hex)	Flags						Fetch Cycle s	Instr. Cycle s
		dst	src		C	Z	S	V	D	H		
DA dst	dst ← DA(dst)	R		40	*	*	*	X	–	–	2	2
		IR		41							2	3
DEC dst	dst ← dst - 1	R		30	–	*	*	*	–	–	2	2
		IR		31							2	3
DECW dst	dst ← dst - 1	RR		80	–	*	*	*	–	–	2	5
		IRR		81							2	6
DI	IRQCTL[7] ← 0			8F	–	–	–	–	–	–	1	2
DJNZ dst, RA	dst ← dst - 1 if dst ≠ 0 PC ← PC + X	r		0A-FA	–	–	–	–	–	–	2	3
EI	IRQCTL[7] ← 1			9F	–	–	–	–	–	–	1	2
HALT	Halt Mode			7F	–	–	–	–	–	–	1	2
INC dst	dst ← dst + 1	R		20	–	*	*	–	–	–	2	2
		IR		21							2	3
		r		0E-FE							1	2
INCW dst	dst ← dst + 1	RR		A0	–	*	*	*	–	–	2	5
		IRR		A1							2	6
IRET	FLAGS ← @SP SP ← SP + 1 PC ← @SP SP ← SP + 2 IRQCTL[7] ← 1			BF	*	*	*	*	*	*	1	5
JP dst	PC ← dst	DA		8D	–	–	–	–	–	–	3	2
		IRR		C4							2	3
JP cc, dst	if cc is true PC ← dst	DA		0D-FD	–	–	–	–	–	–	3	2

Note: Flags Notation:

* = Value is a function of the result of the operation.

– = Unaffected.

X = Undefined.

0 = Reset to 0.

1 = Set to 1.

Table 139. Analog-to-Digital Converter Electrical Characteristics and Timing

$V_{DD} = 3.0\text{ V to }3.6\text{ V}$ $T_A = 0^{\circ}\text{C to }+70^{\circ}\text{C}$ (unless otherwise stated)						
Symbol	Parameter	Minimum	Typical	Maximum	Units	Conditions
	Resolution	10		–	bits	
	Differential Nonlinearity (DNL)	–1.0	–	1.0	LSB ³	External $V_{REF} = 2.0\text{ V}$; $R_S \leftarrow 3.0\text{ k}\Omega$
	Integral Nonlinearity (INL)	–3.0	–	3.0	LSB ³	External $V_{REF} = 2.0\text{ V}$; $R_S \leftarrow 3.0\text{ k}\Omega$
	Offset Error with Calibration		± 1		LSB ³	
	Absolute Accuracy with Calibration		± 3		LSB ³	
V_{REF}	Internal Reference Voltage	1.0 2.0	1.1 2.2	1.2 2.4	V	REFSEL=01 REFSEL=10
V_{REF}	Internal Reference Variation with Temperature		± 1.0		%	Temperature variation with $V_{DD} = 3.0$
V_{REF}	Internal Reference Voltage Variation with V_{DD}		± 0.5		%	Supply voltage variation with $T_A = 30^{\circ}\text{C}$
R_{REFOUT}	Reference Buffer Output Impedance		850		W	When the internal reference is buffered and driven out to the VREF pin (REFOUT = 1)
	Single-Shot Conversion Time	–	5129	–	System clock cycles	All measurements but temperature sensor
			10258			Temperature sensor measurement

Notes:

1. Analog source impedance affects the ADC offset voltage (because of pin leakage) and input settling time.
2. Devices are factory calibrated at $V_{DD} = 3.3\text{ V}$ and $T_A = +30^{\circ}\text{C}$, so the ADC is maximally accurate under these conditions.
3. LSBs are defined assuming 10-bit resolution.
4. This is the maximum recommended resistance seen by the ADC input pin.
5. The input impedance is inversely proportional to the system clock frequency.

Table 148. Z8 Encore! XP F082A Series Ordering Matrix

Part Number	Flash	RAM	NVDS	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description
Z8 Encore! XP F082A Series with 4 KB Flash											
Standard Temperature: 0°C to 70°C											
Z8F041APB020SG	4 KB	1KB	128 B	6	13	2	0	1	1	0	PDIP 8-pin package
Z8F041AQB020SG	4 KB	1KB	128 B	6	13	2	0	1	1	0	QFN 8-pin package
Z8F041ASB020SG	4 KB	1KB	128 B	6	13	2	0	1	1	0	SOIC 8-pin package
Z8F041ASH020SG	4 KB	1KB	128 B	17	19	2	0	1	1	0	SOIC 20-pin package
Z8F041AHH020SG	4 KB	1KB	128 B	17	19	2	0	1	1	0	SSOP 20-pin package
Z8F041APH020SG	4 KB	1KB	128 B	17	19	2	0	1	1	0	PDIP 20-pin package
Z8F041ASJ020SG	4 KB	1KB	128 B	25	19	2	0	1	1	0	SOIC 28-pin package
Z8F041AHJ020SG	4 KB	1KB	128 B	25	19	2	0	1	1	0	SSOP 28-pin package
Z8F041APJ020SG	4 KB	1KB	128 B	25	19	2	0	1	1	0	PDIP 28-pin package
Extended Temperature: -40°C to 105°C											
Z8F041APB020EG	4 KB	1KB	128 B	6	13	2	0	1	1	0	PDIP 8-pin package
Z8F041AQB020EG	4 KB	1KB	128 B	6	13	2	0	1	1	0	QFN 8-pin package
Z8F041ASB020EG	4 KB	1KB	128 B	6	13	2	0	1	1	0	SOIC 8-pin package
Z8F041ASH020EG	4 KB	1KB	128 B	17	19	2	0	1	1	0	SOIC 20-pin package
Z8F041AHH020EG	4 KB	1KB	128 B	17	19	2	0	1	1	0	SSOP 20-pin package
Z8F041APH020EG	4 KB	1KB	128 B	17	19	2	0	1	1	0	PDIP 20-pin package
Z8F041ASJ020EG	4 KB	1KB	128 B	25	19	2	0	1	1	0	SOIC 28-pin package
Z8F041AHJ020EG	4 KB	1KB	128 B	25	19	2	0	1	1	0	SSOP 28-pin package
Z8F041APJ020EG	4 KB	1KB	128 B	25	19	2	0	1	1	0	PDIP 28-pin package

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