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### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/z8f081ahh020eg">https://www.e-xfl.com/product-detail/zilog/z8f081ahh020eg</a>

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**⚡ Warning:** DO NOT USE THIS PRODUCT IN LIFE SUPPORT SYSTEMS.

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- Up to 8 ports capable of direct LED drive with no current limit resistor required
- On-Chip Debugger (OCD)
- Voltage Brown-Out (VBO) protection
- Programmable low battery detection (LVD) (8-pin devices only)
- Bandgap generated precision voltage references available for the ADC, comparator, VBO and LVD
- Power-On Reset (POR)
- 2.7V to 3.6V operating voltage
- 8-, 20- and 28-pin packages
- 0°C to +70°C and –40°C to +105°C for operating temperature ranges

## Part Selection Guide

Table 1 identifies the basic features and package styles available for each device within the Z8 Encore! XP F082A Series product line.

**Table 1. Z8 Encore! XP F082A Series Family Part Selection Guide**

Part Number	Flash (KB)	RAM (B)	NVDS <sup>1</sup> (B)	I/O	Comparator	Advanced Analog <sup>2</sup>	ADC Inputs	Packages
Z8F082A	8	1024	0	6–23	Yes	Yes	4–8	8-, 20- and 28-pin
Z8F081A	8	1024	0	6–25	Yes	No	0	8-, 20- and 28-pin
Z8F042A	4	1024	128	6–23	Yes	Yes	4–8	8-, 20- and 28-pin
Z8F041A	4	1024	128	6–25	Yes	No	0	8-, 20- and 28-pin
Z8F022A	2	512	64	6–23	Yes	Yes	4–8	8-, 20- and 28-pin
Z8F021A	2	512	64	6–25	Yes	No	0	8-, 20- and 28-pin
Z8F012A	1	256	16	6–23	Yes	Yes	4–8	8-, 20- and 28-pin
Z8F011A	1	256	16	6–25	Yes	No	0	8-, 20- and 28-pin

Notes:

1. Non-volatile data storage.

2. Advanced Analog includes ADC, temperature sensor and low-power operational amplifier.

Table 7. Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page
FD9	Port C Control	PCCTL	00	<a href="#">46</a>
FDA	Port C Input Data	PCIN	XX	<a href="#">46</a>
FDB	Port C Output Data	PCOUT	00	<a href="#">46</a>
<b>GPIO Port D</b>				
FDC	Port D Address	PDADDR	00	<a href="#">44</a>
FDD	Port D Control	PDCTL	00	<a href="#">46</a>
FDE	Reserved	—	XX	
FDF	Port D Output Data	PDOUT	00	<a href="#">46</a>
FE0–FEF	Reserved	—	XX	
<b>Watchdog Timer (WDT)</b>				
FF0	Reset Status (Read-only)	RSTSTAT	X0	<a href="#">29</a>
	Watchdog Timer Control (Write-only)	WDTCTL	N/A	<a href="#">96</a>
FF1	Watchdog Timer Reload Upper Byte	WDTU	00	<a href="#">97</a>
FF2	Watchdog Timer Reload High Byte	WDTH	04	<a href="#">97</a>
FF3	Watchdog Timer Reload Low Byte	WDTL	00	<a href="#">98</a>
FF4–FF5	Reserved	—	XX	
<b>Trim Bit Control</b>				
FF6	Trim Bit Address	TRMADR	00	<a href="#">161</a>
FF7	Trim Bit Data	TRMDR	00	<a href="#">162</a>
<b>Flash Memory Controller</b>				
FF8	Flash Control	FCTL	00	<a href="#">155</a>
FF8	Flash Status	FSTAT	00	<a href="#">155</a>
FF9	Flash Page Select	FPS	00	<a href="#">156</a>
	Flash Sector Protect	FPROT	00	<a href="#">157</a>
FFA	Flash Programming Frequency High Byte	FFREQH	00	<a href="#">158</a>
FFB	Flash Programming Frequency Low Byte	FFREQL	00	<a href="#">158</a>
<b>eZ8 CPU</b>				
FFC	Flags	—	XX	See foot-note 2.
FFD	Register Pointer	RP	XX	
FFE	Stack Pointer High Byte	SPH	XX	
FFF	Stack Pointer Low Byte	SPL	XX	

Notes:

1. XX = Undefined.
2. Refer to the [eZ8 CPU Core User Manual \(UM0128\)](#).

## General-Purpose Input/Output

The Z8 Encore! XP F082A Series products support a maximum of 25 port pins (Ports A–D) for general-purpose input/output (GPIO) operations. Each port contains control and data registers. The GPIO control registers determine data direction, open-drain, output drive current, programmable pull-ups, Stop Mode Recovery functionality and alternate pin functions. Each port pin is individually programmable. In addition, the Port C pins are capable of direct LED drive at programmable drive strengths.

### GPIO Port Availability By Device

Table 14 lists the port pins available with each device and package type.

**Table 14. Port Availability by Device and Package Type**

Devices	Package	ADC	Port A	Port B	Port C	Port D	Total I/O
Z8F082ASB, Z8F082APB, Z8F082AQB Z8F042ASB, Z8F042APB, Z8F042AQB Z8F022ASB, Z8F022APB, Z8F022AQB Z8F012ASB, Z8F012APB, Z8F012AQB	8-pin	Yes	[5:0]	No	No	No	6
Z8F081ASB, Z8F081APB, Z8F081AQB Z8F041ASB, Z8F041APB, Z8F041AQB Z8F021ASB, Z8F021APB, Z8F021AQB Z8F011ASB, Z8F011APB, Z8F011AQB	8-pin	No	[5:0]	No	No	No	6
Z8F082APH, Z8F082AHH, Z8F082ASH Z8F042APH, Z8F042AHH, Z8F042ASH Z8F022APH, Z8F022AHH, Z8F022ASH Z8F012APH, Z8F012AHH, Z8F012ASH	20-pin	Yes	[7:0]	[3:0]	[3:0]	[0]	17
Z8F081APH, Z8F081AHH, Z8F081ASH Z8F041APH, Z8F041AHH, Z8F041ASH Z8F021APH, Z8F021AHH, Z8F021ASH Z8F011APH, Z8F011AHH, Z8F011ASH	20-pin	No	[7:0]	[3:0]	[3:0]	[0]	17
Z8F082APJ, Z8F082ASJ, Z8F082AHJ Z8F042APJ, Z8F042ASJ, Z8F042AHJ Z8F022APJ, Z8F022ASJ, Z8F022AHJ Z8F012APJ, Z8F012ASJ, Z8F012AHJ	28-pin	Yes	[7:0]	[5:0]	[7:0]	[0]	23
Z8F081APJ, Z8F081ASJ, Z8F081AHJ Z8F041APJ, Z8F041ASJ, Z8F041AHJ Z8F021APJ, Z8F021ASJ, Z8F021AHJ Z8F011APJ, Z8F011ASJ, Z8F011AHJ	28-pin	No	[7:0]	[7:0]	[7:0]	[0]	25

- Set the initial logic level (High or Low) for the Timer Output alternate function, if appropriate
2. Write to the Timer High and Low Byte registers to set the starting count value.
  3. Write to the Timer Reload High and Low Byte registers to set the Compare value.
  4. Enable the timer interrupt, if appropriate and set the timer interrupt priority by writing to the relevant interrupt registers.
  5. If using the Timer Output function, configure the associated GPIO port pin for the Timer Output alternate function.
  6. Write to the Timer Control Register to enable the timer and initiate counting.

In COMPARE Mode, the system clock always provides the timer input. The Compare time can be calculated by the following equation:

$$\text{COMPARE Mode Time (s)} = \frac{(\text{Compare Value} - \text{Start Value}) \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

## GATED Mode

In GATED Mode, the timer counts only when the Timer Input signal is in its active state (asserted), as determined by the TPOL bit in the Timer Control Register. When the Timer Input signal is asserted, counting begins. A timer interrupt is generated when the Timer Input signal is deasserted or a timer reload occurs. To determine if a Timer Input signal deassertion generated the interrupt, read the associated GPIO input value and compare to the value stored in the TPOL bit.

The timer counts up to the 16-bit reload value stored in the Timer Reload High and Low Byte registers. The timer input is the system clock. When reaching the reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes (assuming the Timer Input signal remains asserted). Also, if the Timer Output alternate function is enabled, the Timer Output pin changes state (from Low to High or from High to Low) at timer reset.

Observe the following steps for configuring a timer for GATED Mode and initiating the count:

1. Write to the Timer Control Register to:
  - Disable the timer



Bit	Description (Continued)
[5:3] PRES	<b>Prescale value</b> The timer input clock is divided by $2^{\text{PRES}}$ , where PRES can be set from 0 to 7. The prescaler is reset each time the Timer is disabled. This reset ensures proper clock division each time the Timer is restarted. 000 = Divide by 1. 001 = Divide by 2. 010 = Divide by 4. 011 = Divide by 8. 100 = Divide by 16. 101 = Divide by 32. 110 = Divide by 64. 111 = Divide by 128.
[2:0] TMODE	<b>Timer Mode</b> This field, along with the TMODEHI bit in the TxCTL0 Register, determines the operating mode of the timer. TMODEHI is the most significant bit of the Timer mode selection value. The entire operating mode bits are expressed as {TMODEHI, TMODE[2:0]}. The TMODEHI is bit 7 of the TxCTL0 Register while TMODE[2:0] is the lower 3 bits of the TxCTL1 Register. 0000 = ONE-SHOT Mode. 0001 = CONTINUOUS Mode. 0010 = COUNTER Mode. 0011 = PWM SINGLE OUTPUT Mode. 0100 = CAPTURE Mode. 0101 = COMPARE Mode. 0110 = GATED Mode. 0111 = CAPTURE/COMPARE Mode. 1000 = PWM DUAL OUTPUT Mode. 1001 = CAPTURE RESTART Mode. 1010 = COMPARATOR COUNTER Mode.

## Timer 0–1 High and Low Byte Registers

The Timer 0–1 High and Low Byte (TxH and TxL) registers, shown in Tables 52 and 53, contain the current 16-bit timer count value. When the timer is enabled, a read from TxH causes the value in TxL to be stored in a temporary holding register. A read from TxL always returns this temporary register when the timers are enabled. When the timer is disabled, reads from TxL read the register directly.

Writing to the Timer High and Low Byte registers while the timer is enabled is not recommended. There are no temporary holding registers available for write operations, so simultaneous 16-bit writes are not possible. If either the Timer High or Low Byte registers are written during counting, the 8-bit written value is placed in the counter (High or Low Byte) at the next clock edge. The counter continues counting from the new value.

Table 94. LVD Trim Values

LVD_TRIM	LVD Threshold (V)		Description
	Typical		
00000	3.60		Maximum LVD threshold
00001	3.55		
00010	3.50		
00011	3.45		
00100	3.40		
00101	3.35		
00110	3.30		
00111	3.25		
01000	3.20		
01001	3.15		
01010	3.10		Default on Reset
01011	3.05		
01100	3.00		
01101	2.95		
01110	2.90		
01111	2.85		
10000	2.80		
10001	2.75		
10010	2.70		
10011	2.70		
to	to		
11111	1.65		Minimum LVD threshold

## ADC Calibration Data

Table 96. ADC Calibration Bits

Bit	7	6	5	4	3	2	1	0
Field	ADC_CAL							
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Information Page Memory 0060H–007DH							
Note: U = Unchanged by Reset. R/W = Read/Write.								

Bit	Description
[7:0] ADC_CAL	<b>Analog-to-Digital Converter Calibration Values</b> Contains factory-calibrated values for ADC gain and offset compensation. Each of the ten supported modes has one byte of offset calibration and two bytes of gain calibration. These values are read by the software to compensate ADC measurements as described in the <a href="#">Software Compensation Procedure Using Factory Calibration Data</a> section on page 129. The location of each calibration byte is provided in Table 97.

Table 97. ADC Calibration Data Location

Info Page Address	Memory Address	Compensation Usage	ADC Mode	Reference Type
60	FE60	Offset	Single-Ended Unbuffered	Internal 2.0 V
08	FE08	Gain High Byte	Single-Ended Unbuffered	Internal 2.0 V
09	FE09	Gain Low Byte	Single-Ended Unbuffered	Internal 2.0 V
63	FE63	Offset	Single-Ended Unbuffered	Internal 1.0 V
0A	FE0A	Gain High Byte	Single-Ended Unbuffered	Internal 1.0 V
0B	FE0B	Gain Low Byte	Single-Ended Unbuffered	Internal 1.0 V
66	FE66	Offset	Single-Ended Unbuffered	External 2.0 V
0C	FE0C	Gain High Byte	Single-Ended Unbuffered	External 2.0 V
0D	FE0D	Gain Low Byte	Single-Ended Unbuffered	External 2.0 V
69	FE69	Offset	Single-Ended 1x Buffered	Internal 2.0 V
0E	FE0E	Gain High Byte	Single-Ended 1x Buffered	Internal 2.0 V
0F	FE0F	Gain Low Byte	Single-Ended 1x Buffered	Internal 2.0 V
6C	FE6C	Offset	Single-Ended 1x Buffered	External 2.0 V
10	FE10	Gain High Byte	Single-Ended 1x Buffered	External 2.0 V
11	FE11	Gain Low Byte	Single-Ended 1x Buffered	External 2.0 V
6F	FE6F	Offset	Differential Unbuffered	Internal 2.0 V

When selecting a new clock source, the system clock oscillator failure detection circuitry and the Watchdog Timer oscillator failure circuitry must be disabled. If SOFEN and WOFEN are not disabled prior to a clock switch-over, it is possible to generate an interrupt for a failure of either oscillator. The Failure detection circuitry can be enabled any-time after a successful write of OSCSEL in the OSCCTL Register.

The internal precision oscillator is enabled by default. If the user code changes to a different oscillator, it may be appropriate to disable the IPO for power savings. Disabling the IPO does not occur automatically.

## Clock Failure Detection and Recovery

Should an oscillator or timer fail, there are methods of recovery, as this section describes.

### System Clock Oscillator Failure

The Z8F04xA family devices can generate nonmaskable interrupt-like events when the primary oscillator fails. To maintain system function in this situation, the clock failure recovery circuitry automatically forces the Watchdog Timer oscillator to drive the system clock. The Watchdog Timer oscillator must be enabled to allow the recovery. Although this oscillator runs at a much slower speed than the original system clock, the CPU continues to operate, allowing execution of a clock failure vector and software routines that either remedy the oscillator failure or issue a failure alert. This automatic switch-over is not available if the Watchdog Timer is selected as the system clock oscillator. It is also unavailable if the Watchdog Timer oscillator is disabled, though it is not necessary to enable the Watchdog Timer reset function (see the [Watchdog Timer](#) chapter on page 93).

The primary oscillator failure detection circuitry asserts if the system clock frequency drops below 1 kHz  $\pm$ 50%. If an external signal is selected as the system oscillator, it is possible that a very slow but nonfailing clock can generate a failure condition. Under these conditions, do not enable the clock failure circuitry (SOFEN must be deasserted in the OSCCTL Register).

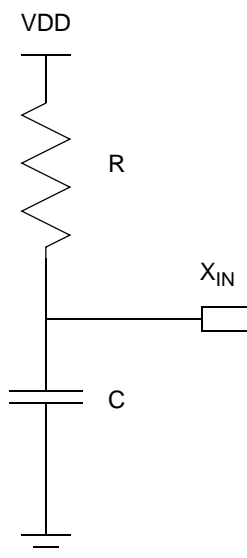
### Watchdog Timer Failure

In the event of a Watchdog Timer oscillator failure, a similar nonmaskable interrupt-like event is issued. This event does not trigger an attendant clock switch-over, but alerts the CPU of the failure. After a Watchdog Timer failure, it is no longer possible to detect a primary oscillator failure. The failure detection circuitry does not function if the Watchdog Timer is used as the system clock oscillator or if the Watchdog Timer oscillator has been disabled. For either of these cases, it is necessary to disable the detection circuitry by deasserting the WDFEN bit of the OSCCTL Register.

The Watchdog Timer oscillator failure detection circuit counts system clocks while looking for a Watchdog Timer clock. The logic counts 8004 system clock cycles before determining that a failure has occurred. The system clock rate determines the speed at which

## Oscillator Operation with an External RC Network

Figure 28 displays a recommended configuration for connection with an external resistor-capacitor (RC) network.



**Figure 28. Connecting the On-Chip Oscillator to an External RC Network**

An external resistance value of 45 k $\Omega$  is recommended for oscillator operation with an external RC network. The minimum resistance value to ensure operation is 40 k $\Omega$ . The typical oscillator frequency can be estimated from the values of the resistor ( $R$  in k $\Omega$ ) and capacitor ( $C$  in pF) elements using the following equation:

$$\text{Oscillator Frequency (kHz)} = \frac{1 \times 10^6}{(0.4 \times R \times C) + (4 \times C)}$$

Figure 29 displays the typical (3.3 V and 25°C) oscillator frequency as a function of the capacitor ( $C$ , in pF) employed in the RC network assuming a 45 K $\Omega$  external resistor. For very small values of  $C$ , the parasitic capacitance of the oscillator  $X_{IN}$  pin and the printed circuit board must be included in the estimation of the oscillator frequency.

It is possible to operate the RC oscillator using only the parasitic capacitance of the package and printed circuit board. To minimize sensitivity to external parasitics, external capacitance values in excess of 20 pF are recommended.

Register file size varies depending on the device type. See the device-specific Z8 Encore! XP Product Specification to determine the exact register file range available.

## eZ8 CPU Instruction Notation

In the eZ8 CPU Instruction Summary and Description sections, the operands, condition codes, status flags and address modes are represented by a notational shorthand that is described in Table 118.

**Table 118. Notational Shorthand**

Notation	Description	Operand	Range
b	Bit	b	b represents a value from 0 to 7 (000B to 111B).
cc	Condition code	—	Refer to the Condition Codes section in the <a href="#">eZ8 CPU Core User Manual (UM0128)</a> .
DA	Direct address	AddrS	Represents a number in the range 0000H to FFFFH.
ER	Extended addressing register	Reg	Reg. represents a number in the range of 000H to FFFH.
IM	Immediate data	#Data	Data is a number between 00H to FFH.
Ir	Indirect working register	@Rn	n = 0–15.
IR	Indirect register	@Reg	Reg. represents a number in the range of 00H to FFH.
Irr	Indirect working register pair	@RRp	p = 0, 2, 4, 6, 8, 10, 12, or 14.
IRR	Indirect register pair	@Reg	Reg. represents an even number in the range 00H to FEH.
p	Polarity	p	Polarity is a single bit binary value of either 0B or 1B.
r	Working register	Rn	n = 0 – 15.
R	Register	Reg	Reg. represents a number in the range of 00H to FFH.
RA	Relative address	X	X represents an index in the range of +127 to –128 which is an offset relative to the address of the next instruction.
rr	Working register pair	RRp	p = 0, 2, 4, 6, 8, 10, 12, or 14.
RR	Register pair	Reg	Reg. represents an even number in the range of 00H to FEH.

Table 126. Program Control Instructions

Mnemonic	Operands	Instruction
BRK	—	On-Chip Debugger Break
BTJ	p, bit, src, DA	Bit Test and Jump
BTJNZ	bit, src, DA	Bit Test and Jump if Non-Zero
BTJZ	bit, src, DA	Bit Test and Jump if Zero
CALL	dst	Call Procedure
DJNZ	dst, src, RA	Decrement and Jump Non-Zero
IRET	—	Interrupt Return
JP	dst	Jump
JP cc	dst	Jump Conditional
JR	DA	Jump Relative
JR cc	DA	Jump Relative Conditional
RET	—	Return
TRAP	vector	Software Trap

Table 127. Rotate and Shift Instructions

Mnemonic	Operands	Instruction
BSWAP	dst	Bit Swap
RL	dst	Rotate Left
RLC	dst	Rotate Left through Carry
RR	dst	Rotate Right
RRC	dst	Rotate Right through Carry
SRA	dst	Shift Right Arithmetic
SRL	dst	Shift Right Logical
SWAP	dst	Swap Nibbles

**Table 139. Analog-to-Digital Converter Electrical Characteristics and Timing**

$V_{DD} = 3.0\text{ V to }3.6\text{ V}$ $T_A = 0^{\circ}\text{C to }+70^{\circ}\text{C}$ (unless otherwise stated)						
Symbol	Parameter	Minimum	Typical	Maximum	Units	Conditions
	Resolution	10		–	bits	
	Differential Nonlinearity (DNL)	–1.0	–	1.0	LSB <sup>3</sup>	External $V_{REF} = 2.0\text{ V}$ ; $R_S \leftarrow 3.0\text{ k}\Omega$
	Integral Nonlinearity (INL)	–3.0	–	3.0	LSB <sup>3</sup>	External $V_{REF} = 2.0\text{ V}$ ; $R_S \leftarrow 3.0\text{ k}\Omega$
	Offset Error with Calibration		$\pm 1$		LSB <sup>3</sup>	
	Absolute Accuracy with Calibration		$\pm 3$		LSB <sup>3</sup>	
$V_{REF}$	Internal Reference Voltage	1.0 2.0	1.1 2.2	1.2 2.4	V	REFSEL=01 REFSEL=10
$V_{REF}$	Internal Reference Variation with Temperature		$\pm 1.0$		%	Temperature variation with $V_{DD} = 3.0$
$V_{REF}$	Internal Reference Voltage Variation with $V_{DD}$		$\pm 0.5$		%	Supply voltage variation with $T_A = 30^{\circ}\text{C}$
$R_{REFOUT}$	Reference Buffer Output Impedance		850		W	When the internal reference is buffered and driven out to the VREF pin (REFOUT = 1)
	Single-Shot Conversion Time	–	5129	–	System clock cycles	All measurements but temperature sensor
			10258			Temperature sensor measurement

**Notes:**

1. Analog source impedance affects the ADC offset voltage (because of pin leakage) and input settling time.
2. Devices are factory calibrated at  $V_{DD} = 3.3\text{ V}$  and  $T_A = +30^{\circ}\text{C}$ , so the ADC is maximally accurate under these conditions.
3. LSBs are defined assuming 10-bit resolution.
4. This is the maximum recommended resistance seen by the ADC input pin.
5. The input impedance is inversely proportional to the system clock frequency.



## UART Timing

Figure 37 and Table 146 provide timing information for UART pins for the case where CTS is used for flow control. The CTS to DE assertion delay (T1) assumes the Transmit Data Register has been loaded with data prior to CTS assertion.

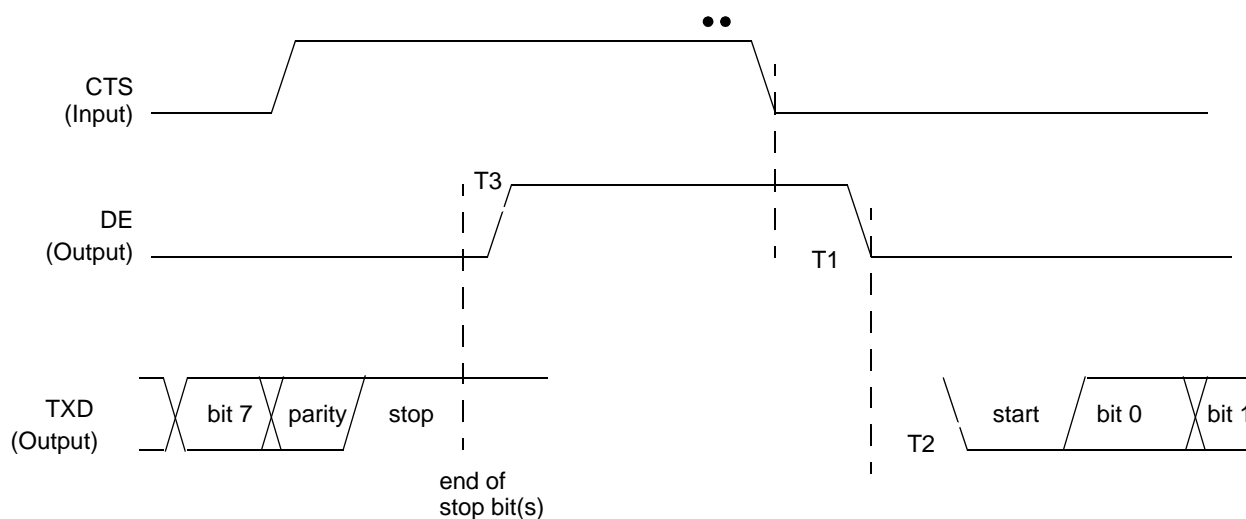


Figure 37. UART Timing With CTS

Table 146. UART Timing With CTS

Parameter	Abbreviation	Delay (ns)	
		Minimum	Maximum
UART			
T <sub>1</sub>	CTS Fall to DE output delay	2 * X <sub>IN</sub> period	2 * X <sub>IN</sub> period + 1 bit time
T <sub>2</sub>	DE assertion to TXD falling edge (start bit) delay		± 5
T <sub>3</sub>	End of Stop Bit(s) to DE deassertion delay		± 5

Table 148. Z8 Encore! XP F082A Series Ordering Matrix

Part Number	Flash	RAM	NVDS	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description
<b>Z8 Encore! XP F082A Series with 4 KB Flash, 10-Bit Analog-to-Digital Converter</b>											
<b>Standard Temperature: 0°C to 70°C</b>											
Z8F042APB020SG	4 KB	1KB	128 B	6	14	2	4	1	1	1	PDIP 8-pin package
Z8F042AQB020SG	4 KB	1KB	128 B	6	14	2	4	1	1	1	QFN 8-pin package
Z8F042ASB020SG	4 KB	1KB	128 B	6	14	2	4	1	1	1	SOIC 8-pin package
Z8F042ASH020SG	4 KB	1KB	128 B	17	20	2	7	1	1	1	SOIC 20-pin package
Z8F042AHH020SG	4 KB	1KB	128 B	17	20	2	7	1	1	1	SSOP 20-pin package
Z8F042APH020SG	4 KB	1KB	128 B	17	20	2	7	1	1	1	PDIP 20-pin package
Z8F042ASJ020SG	4 KB	1KB	128 B	23	20	2	8	1	1	1	SOIC 28-pin package
Z8F042AHJ020SG	4 KB	1KB	128 B	23	20	2	8	1	1	1	SSOP 28-pin package
Z8F042APJ020SG	4 KB	1KB	128 B	23	20	2	8	1	1	1	PDIP 28-pin package
<b>Extended Temperature: -40°C to 105°C</b>											
Z8F042APB020EG	4 KB	1KB	128 B	6	14	2	4	1	1	1	PDIP 8-pin package
Z8F042AQB020EG	4 KB	1KB	128 B	6	14	2	4	1	1	1	QFN 8-pin package
Z8F042ASB020EG	4 KB	1KB	128 B	6	14	2	4	1	1	1	SOIC 8-pin package
Z8F042ASH020EG	4 KB	1KB	128 B	17	20	2	7	1	1	1	SOIC 20-pin package
Z8F042AHH020EG	4 KB	1KB	128 B	17	20	2	7	1	1	1	SSOP 20-pin package
Z8F042APH020EG	4 KB	1KB	128 B	17	20	2	7	1	1	1	PDIP 20-pin package
Z8F042ASJ020EG	4 KB	1KB	128 B	23	20	2	8	1	1	1	SOIC 28-pin package
Z8F042AHJ020EG	4 KB	1KB	128 B	23	20	2	8	1	1	1	SSOP 28-pin package
Z8F042APJ020EG	4 KB	1KB	128 B	23	20	2	8	1	1	1	PDIP 28-pin package

**Table 148. Z8 Encore! XP F082A Series Ordering Matrix**

Part Number	Flash	RAM	NVDS	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description
<b>Z8 Encore! XP F082A Series with 2 KB Flash</b>											
<b>Standard Temperature: 0°C to 70°C</b>											
Z8F021APB020SG	2 KB	512 B	64 B	6	13	2	0	1	1	0	PDIP 8-pin package
Z8F021AQB020SG	2 KB	512 B	64 B	6	13	2	0	1	1	0	QFN 8-pin package
Z8F021ASB020SG	2 KB	512 B	64 B	6	13	2	0	1	1	0	SOIC 8-pin package
Z8F021ASH020SG	2 KB	512 B	64 B	17	19	2	0	1	1	0	SOIC 20-pin package
Z8F021AHH020SG	2 KB	512 B	64 B	17	19	2	0	1	1	0	SSOP 20-pin package
Z8F021APH020SG	2 KB	512 B	64 B	17	19	2	0	1	1	0	PDIP 20-pin package
Z8F021ASJ020SG	2 KB	512 B	64 B	25	19	2	0	1	1	0	SOIC 28-pin package
Z8F021AHJ020SG	2 KB	512 B	64 B	25	19	2	0	1	1	0	SSOP 28-pin package
Z8F021APJ020SG	2 KB	512 B	64 B	25	19	2	0	1	1	0	PDIP 28-pin package
<b>Extended Temperature: -40°C to 105°C</b>											
Z8F021APB020EG	2 KB	512 B	64 B	6	13	2	0	1	1	0	PDIP 8-pin package
Z8F021AQB020EG	2 KB	512 B	64 B	6	13	2	0	1	1	0	QFN 8-pin package
Z8F021ASB020EG	2 KB	512 B	64 B	6	13	2	0	1	1	0	SOIC 8-pin package
Z8F021ASH020EG	2 KB	512 B	64 B	17	19	2	0	1	1	0	SOIC 20-pin package
Z8F021AHH020EG	2 KB	512 B	64 B	17	19	2	0	1	1	0	SSOP 20-pin package
Z8F021APH020EG	2 KB	512 B	64 B	17	19	2	0	1	1	0	PDIP 20-pin package
Z8F021ASJ020EG	2 KB	512 B	64 B	25	19	2	0	1	1	0	SOIC 28-pin package
Z8F021AHJ020EG	2 KB	512 B	64 B	25	19	2	0	1	1	0	SSOP 28-pin package
Z8F021APJ020EG	2 KB	512 B	64 B	25	19	2	0	1	1	0	PDIP 28-pin package

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