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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f081apj020eg

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Signal Mnemonic	I/O	Description
Analog		
ANA[7:0]	Ι	Analog Port. These signals are used as inputs to the analog-to-digital converter (ADC).
VREF	I/O	Analog-to-digital converter reference voltage input, or buffered output for internal reference.
Low-Power Operati	ional Ar	nplifier (LPO)
AMPINP/AMPINN	Ι	LPO inputs. If enabled, these pins drive the positive and negative amplifier inputs respectively.
AMPOUT	0	LPO output. If enabled, this pin is driven by the on-chip LPO.
Oscillators		
XIN	I	External Crystal Input. This is the input pin to the crystal oscillator. A crystal can be connected between it and the X_{OUT} pin to form the oscillator. In addition, this pin is used with external RC networks or external clock drivers to provide the system clock.
X _{OUT}	0	External Crystal Output. This pin is the output of the crystal oscillator. A crystal can be connected between it and the XIN pin to form the oscillator.
Clock Input		
CLKIN	Ι	Clock Input Signal. This pin may be used to input a TTL-level signal to be used as the system clock.
LED Drivers		
LED	0	Direct LED drive capability. All port C pins have the capability to drive an LED without any other external components. These pins have programmable drive strengths set by the GPIO block.
On-Chip Debugger		
DBG	I/O	Debug. This signal is the control and data input and output to and from the On-Chip Debugger.
		Caution: The DBG pin is open-drain and requires a pull-up resistor to ensure proper operation.
Notes: 1. PB6 and PB7 are	only ava	ensure proper operation.

Table 2. Signal Descriptions (Continued)

replaced by AV_{DD} and AV_{SS} . 2. The AV_{DD} and AV_{SS} signals are available only in 28-pin packages with ADC. They are replaced by PB6 and PB7 on 28-pin packages without ADC.



Figure 5. Power-On Reset Operation

Voltage Brown-Out Reset

The devices in the Z8 Encore! XP F082A Series provide low Voltage Brown-Out (VBO) protection. The VBO circuit senses when the supply voltage drops to an unsafe level (below the VBO threshold voltage) and forces the device into the Reset state. While the supply voltage remains below the Power-On Reset voltage threshold (V_{POR}), the VBO block holds the device in the Reset.

After the supply voltage again exceeds the Power-On Reset voltage threshold, the device progresses through a full System Reset sequence, as described in the Power-On Reset section. Following Power-On Reset, the POR status bit in the Reset Status (RSTSTAT) Register is set to 1. Figure 6 displays Voltage Brown-Out operation. See the <u>Electrical</u> <u>Characteristics</u> chapter on page 226 for the VBO and POR threshold voltages (V_{VBO} and V_{POR}).

The Voltage Brown-Out circuit can be either enabled or disabled during STOP Mode. Operation during STOP Mode is set by the VBO_AO Flash option bit. See the <u>Flash</u> <u>Option Bits</u> chapter on page 159 for information about configuring VBO_AO. tor address. Following Stop Mode Recovery, the STOP bit in the Reset Status (RSTSTAT) Register is set to 1. Table 10 lists the Stop Mode Recovery sources and resulting actions. The text following provides more detailed information about each of the Stop Mode Recovery sources.

Operating Mode	Stop Mode Recovery Source	Action		
STOP Mode	Watchdog Timer time-out when configured for Reset	Stop Mode Recovery		
	Watchdog Timer time-out when configured for interrupt	Stop Mode Recovery followed by interrupt (if interrupts are enabled)		
	Data transition on any GPIO port pin enabled as a Stop Mode Recovery source	Stop Mode Recovery		
	Assertion of external RESET Pin	System Reset		
	Debug Pin driven Low	System Reset		

Table 10. Stop Mode Recovery Sources and Resulting Action

Stop Mode Recovery Using Watchdog Timer Time-Out

If the Watchdog Timer times out during STOP Mode, the device undergoes a Stop Mode Recovery sequence. In the Reset Status (RSTSTAT) Register, the WDT and STOP bits are set to 1. If the Watchdog Timer is configured to generate an interrupt upon time-out and the Z8 Encore! XP F082A Series device is configured to respond to interrupts, the eZ8 CPU services the Watchdog Timer interrupt request following the normal Stop Mode Recovery sequence.

Stop Mode Recovery Using a GPIO Port Pin Transition

Each of the GPIO port pins may be configured as a Stop Mode Recovery input source. On any GPIO pin enabled as a Stop Mode Recovery source, a change in the input pin value (from High to Low or from Low to High) initiates Stop Mode Recovery.

• Note: SMR pulses shorter than specified do not trigger a recovery (see <u>Table 135</u> on page 233). In this instance, the STOP bit in the Reset Status (RSTSTAT) Register is set to 1.

Caution: In STOP Mode, the GPIO Port Input Data registers (PxIN) are disabled. The Port Input Data registers record the Port transition only if the signal stays on the Port pin through the end of the Stop Mode Recovery delay. As a result, short pulses on the Port pin can initiate Stop Mode Recovery without being written to the Port Input Data Register or

Shared Debug Pin

On the 8-pin version of this device only, the Debug pin shares function with the PA0 GPIO pin. This pin performs as a general purpose input pin on power-up, but the debug logic monitors this pin during the reset sequence to determine if the unlock sequence occurs. If the unlock sequence is present, the debug function is unlocked and the pin no longer functions as a GPIO pin. If it is not present, the debug feature is disabled until/unless another reset event occurs. For more details, see the <u>On-Chip Debugger</u> chapter on page 180.

Crystal Oscillator Override

For systems using a crystal oscillator, PA0 and PA1 are used to connect the crystal. When the crystal oscillator is enabled, the GPIO settings are overridden and PA0 and PA1 are disabled. See the <u>Oscillator Control Register Definitions section on page 196</u> for details.

5V Tolerance

All six I/O pins on the 8-pin devices are 5V-tolerant, unless the programmable pull-ups are enabled. If the pull-ups are enabled and inputs higher than V_{DD} are applied to these parts, excessive current flows through those pull-up devices and can damage the chip.

Note: In the 20- and 28-pin versions of this device, any pin which shares functionality with an ADC, crystal or comparator port is not 5 V-tolerant, including PA[1:0], PB[5:0] and PC[2:0]. All other signal pins are 5 V-tolerant and can safely handle inputs higher than V_{DD} except when the programmable pull-ups are enabled.

External Clock Setup

For systems using an external TTL drive, PB3 is the clock source for 20- and 28-pin devices. In this case, configure PB3 for alternate function CLKIN. Write the Oscillator Control (OSCCTL) Register such that the external oscillator is selected as the system clock. See the <u>Oscillator Control Register Definitions section on page 196</u> for details. For 8-pin devices, use PA1 instead of PB3.

Port	Pin	Mnemonic	Alternate Function Description	Alternate Function Set Register AFS1
Port B ³	PB0	Reserved		AFS1[0]: 0
		ANA0/AMPOUT	ADC Analog Input/LPO Output	AFS1[0]: 1
	PB1	Reserved		AFS1[1]: 0
		ANA1/AMPINN	ADC Analog Input/LPO Input (N)	AFS1[1]: 1
	PB2	Reserved		AFS1[2]: 0
		ANA2/AMPINP	ADC Analog Input/LPO Input (P)	AFS1[2]: 1
	PB3	CLKIN	External Clock Input	AFS1[3]: 0
		ANA3	ADC Analog Input	AFS1[3]: 1
	PB4	Reserved		AFS1[4]: 0
		ANA7	ADC Analog Input	AFS1[4]: 1
	PB5	Reserved		AFS1[5]: 0
		V _{REF} ⁴	ADC Voltage Reference	AFS1[5]: 1
	PB6	Reserved		AFS1[6]: 0
		Reserved		AFS1[6]: 1
	PB7	Reserved		AFS1[7]: 0
		Reserved		AFS1[7]: 1

Table 15. Port Alternate Function Mapping (Non 8-Pin Parts) (Continued)

Notes:

- Because there is only a single alternate function for each Port A pin, the Alternate Function Set registers are not implemented for Port A. Enabling alternate function selections automatically enables the associated alternate function. See the <u>Port A–D Alternate Function Subregisters (PxAF)</u> section on page 47 for details.
- 2. Whether PA0/PA6 takes on the timer input or timer output complement function depends on the timer configuration. See the <u>Timer Pin Signal Operation</u> section on page 84 for details.
- Because there are at most two choices of alternate function for any pin of Port B, the Alternate Function Set Register AFS2 is not used to select the function. Alternate function selection must also be enabled. See the <u>Port</u> <u>A–D Alternate Function Subregisters (PxAF)</u> section on page 47 for details.
- 4. V_{RFF} is available on PB5 in 28-pin products and on PC2 in 20-pin parts.
- Because there are at most two choices of alternate function for any pin of Port C, the Alternate Function Set Register AFS2 is not used to select the function. Alternate function selection must also be enabled. See the <u>Port</u> <u>A–D Alternate Function Subregisters (PxAF)</u> section on page 47 for details.
- Because there is only a single alternate function for the Port PD0 pin, the Alternate Function Set registers are not implemented for Port D. Enabling alternate function selections automatically enables the associated alternate function. See the <u>Port A–D Alternate Function Subregisters (PxAF)</u> section on page 47 for details.

Bit	7	6	5	4	3	2	1	0
Field	POC7	POC6	POC5	POC4	POC3	POC2	POC1	POC0
RESET		00H (Ports A-C); 01H (Port D)						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	If 03H ir	n Port A–D A	Address Reg	gister, acces	sible throug	h the Port A	–D Control F	Register

Table 23. Port A–D Output Control Subregisters (PxOC)

Bit	Description
[7:0]	Port Output Control
POC	K These bits function independently of the alternate function bit and always disable the drains if set to 1.
	0 = The source current is enabled for any output mode unless overridden by the alternate func- tion (push-pull output).
	1 = The source current for the associated pin is disabled (open-drain mode).
Note:	x indicates the specific GPIO port pin number (7–0).

Port A–D High Drive Enable Subregisters

The Port A–D High Drive Enable Subregister, shown in Table 24, is accessed through the port A–D Control Register by writing 04H to the Port A–D Address Register. Setting the bits in the Port A–D High Drive Enable subregisters to 1 configures the specified port pins for high current output drive operation. The Port A–D High Drive Enable subregister affects the pins directly and, as a result, alternate functions are also affected.

Bit	7	6	5	4	3	2	1	0
Field	PHDE7	PHDE6	PHDE5	PHDE4	PHDE3	PHDE2	PHDE1	PHDE0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	lf 04H ir	n Port A–D A	Address Reg	gister, acces	sible throug	h the Port A	–D Control F	Register

Table 24. Port A–D High Drive Enable Subregisters (PxHDE)

Bit	Description
[7:0] PHDEx	Port High Drive Enabled 0 = The port pin is configured for standard output current drive.
	1 = The port pin is configured for high output current drive.
Note: x inc	dicates the specific GPIO port pin number (7–0).

The PWM period is represented by the following equation:

 $PWM Period (s) = \frac{Reload Value \times Prescale}{System Clock Frequency (Hz)}$

If an initial starting value other than 0001H is loaded into the Timer High and Low Byte registers, use the ONE-SHOT Mode equation to determine the first PWM time-out period.

If TPOL is set to 0, the ratio of the PWM output High time to the total period is represented by:

PWM Output High Time Ratio (%) = $\frac{\text{Reload Value} - \text{PWM Value}}{\text{Reload Value}} \times 100$

If TPOL is set to 1, the ratio of the PWM output High time to the total period is represented by:

PWM Output High Time Ratio (%) = $\frac{PWM Value}{Reload Value} \times 100$

PWM DUAL OUTPUT Mode

In PWM DUAL OUTPUT Mode, the timer outputs a Pulse-Width Modulated (PWM) output signal pair (basic PWM signal and its complement) through two GPIO port pins. The timer input is the system clock. The timer first counts up to the 16-bit PWM match value stored in the Timer PWM High and Low Byte registers. When the timer count value matches the PWM value, the Timer Output toggles. The timer continues counting until it reaches the reload value stored in the Timer Reload High and Low Byte registers. Upon reaching the reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes.

If the TPOL bit in the Timer Control Register is set to 1, the Timer Output signal begins as a High (1) and transitions to a Low (0) when the timer value matches the PWM value. The Timer Output signal returns to a High (1) after the timer reaches the reload value and is reset to 0001H.

If the TPOL bit in the Timer Control Register is set to 0, the Timer Output signal begins as a Low (0) and transitions to a High (1) when the timer value matches the PWM value. The Timer Output signal returns to a Low (0) after the timer reaches the reload value and is reset to 0001H.

The timer also generates a second PWM output signal Timer Output Complement. The Timer Output Complement is the complement of the Timer Output PWM signal. A programmable deadband delay can be configured to time delay (0 to 128 system clock cycles) PWM output transitions on these two pins from a low to a high (inactive to active). This

Timer Reload High and Low Byte Registers

The Timer 0–1 Reload High and Low Byte (TxRH and TxRL) registers, shown in Tables 54 and 55, store a 16-bit reload value, {TRH[7:0], TRL[7:0]}. Values written to the Timer Reload High Byte Register are stored in a temporary holding register. When a write to the Timer Reload Low Byte Register occurs, the temporary holding register value is written to the Timer High Byte Register. This operation allows simultaneous updates of the 16-bit Timer reload value.

In COMPARE Mode, the Timer Reload High and Low Byte registers store the 16-bit Compare value.

Bit	7	6	5	4	3	2	1	0
Field				TF	RH			
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address				F02H,	F0AH			

Table 54. Timer 0–1 Reload High Byte Register (TxRH)

Bit	7	6	5	4	3	2	1	0
Field				TF	RL			
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address				F03H,	F0BH			

Bit	Description
[7:0]	Timer Reload Register High and Low
TRH, TRL	These two bytes form the 16-bit reload value, {TRH[7:0], TRL[7:0]}. This value sets the max- imum count value which initiates a timer reload to 0001H. In COMPARE Mode, these two bytes form the 16-bit Compare value.

Bit	7	6	5	4	3	2	1	0
Field				COMP	_ADDR			
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F45H							
	D							

Table 69. UART Address Compare Register (U0ADDR)

Bit	Description
[7:0]	Compare Address
COMP_ADDR	This 8-bit value is compared to incoming address bytes.

UART Baud Rate High and Low Byte Registers

The UART Baud Rate High (UxBRH) and Low Byte (UxBRL) registers, shown in Tables 70 and 71, combine to create a 16-bit baud rate divisor value (BRG[15:0]) that sets the data transmission rate (baud rate) of the UART.

Table 70	UART	Baud	Rate High	Byte	Register	(U0BRH)
----------	------	------	-----------	------	----------	---------

Bit	7	6	5	4	3	2	1	0
Field		BRH						
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F46H							

Bit Description

[7:0]	UART Baud Rate High Byte
BRH	

Table 71. UART Baud Rate Low Byte Register (U0BRL)

Bit	7	6	5	4	3	2	1	0
Field		BRL						
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F47H							

Bit	Description
[7:0] BRL	UART Baud Rate Low Byte

For the reserved values, all input switches are disabled to avoid leakage or other undesirable operation. ADC samples taken with reserved bit settings are undefined.

SINGLE-ENDED Mode:

0000 = ANA0 (transimpedance amp output when enabled) 0001 = ANA1 (transimpedance amp inverting input) 0010 = ANA2 (transimpedance amp noninverting input) 0011 = ANA3 0100 = ANA4 0101 = ANA5 0110 = ANA6 0111 = ANA7 1000 = Reserved 1001 = Reserved 1010 = Reserved 1011 = Reserved 1100 = Hold transimpedance input nodes (ANA1 and ANA2) to ground. 1101 = Reserved 1110 = Temperature Sensor.

1111 = Reserved.

DIFFERENTIAL Mode (noninverting input and inverting input respectively):

- 0000 = ANA0 and ANA1 0001 = ANA2 and ANA3 0010 = ANA4 and ANA5 0011 = ANA4 and ANA5 0011 = ANA1 and ANA0 0100 = ANA3 and ANA2 0101 = ANA5 and ANA4 0110 = ANA6 and ANA5 0111 = ANA0 and ANA5 1001 = ANA0 and ANA3 1001 = ANA0 and ANA4 1010 = ANA0 and ANA5 1011 = Reserved 1100 = Reserved 1101 = Reserved 1101 = Reserved1110 = Reserved
- 1111 = Manual Offset Calibration Mode

ADC Control/Status Register 1

The ADC Control/Status Register 1 (ADCCTL1) configures the input buffer stage, enables the threshold interrupts and contains the status of both threshold triggers. It is also used to select the voltage reference configuration. The following code example illustrates how to safely enable the comparator:

Comparator Control Register Definition

The Comparator Control Register (CMP0) configures the comparator inputs and sets the value of the internal voltage reference.

Bit	7	6	5	4	3	2	1	0
Field	INPSEL	INNSEL	REFLVL			Reserved (20-/28-pin) REFLVL (8-pin)		
RESET	0	0	0	1	0	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F90H							

Table 77. Comparator Control Register (CMP0)

Bit	Description
[7] INPSEL	Signal Select for Positive Input 0 = GPIO pin used as positive comparator input. 1 = Temperature sensor used as positive comparator input.
[6] INNSEL	Signal Select for Negative Input 0 = Internal reference disabled, GPIO pin used as negative comparator input. 1 = Internal reference enabled as negative comparator input.

150

Table 79. Flash Code Protection Using the Flash Option Bits

FWP	Flash Code Protection Description
0	Programming and erasing disabled for all of Flash Program Mem- ory. In user code programming, Page Erase and Mass Erase are all
	disabled. Mass Erase is available through the On-Chip Debugger.
1	Programming, Page Erase and Mass Erase are enabled for all of Flash Program Memory.

Flash Code Protection Using the Flash Controller

At Reset, the Flash Controller locks to prevent accidental program or erasure of the Flash memory. To program or erase the Flash memory, first write the Page Select Register with the target page. Unlock the Flash Controller by making two consecutive writes to the Flash Control Register with the values 73H and 8CH, sequentially. The Page Select Register must be rewritten with the target page. If the two Page Select writes do not match, the controller reverts to a locked state. If the two writes match, the selected page becomes active. See Figure 22 on page 148 for details.

After unlocking a specific page, you can enable either Page Program or Erase. Writing the value 95H causes a Page Erase only if the active page resides in a sector that is not protected. Any other value written to the Flash Control Register locks the Flash Controller. Mass Erase is not allowed in the user code but only in through the Debug Port.

After unlocking a specific page, you can also write to any byte on that page. After a byte is written, the page remains unlocked, allowing for subsequent writes to other bytes on the same page. Further writes to the Flash Control Register cause the active page to revert to a locked state.

Sector-Based Flash Protection

The final protection mechanism is implemented on a per-sector basis. The Flash memories of Z8 Encore! XP devices are divided into maximum number of 8 sectors. A sector is 1/8 of the total Flash memory size unless this value is smaller than the page size – in which case, the sector and page sizes are equal. On Z8 Encore! F082A Series devices, the sector size is varied according to the Flash memory configuration shown in <u>Table 78</u> on page 146.

The Flash Sector Protect Register can be configured to prevent sectors from being programmed or erased. After a sector is protected, it cannot be unprotected by user code. The Flash Sector Protect Register is cleared after reset, and any previously-written protection values are lost. User code must write this register in their initialization routine if they prefer to enable sector protection.

The Flash Sector Protect Register shares its Register File address with the Page Select Register. The Flash Sector Protect Register is accessed by writing the Flash Control Regis-

Flash Controller Behavior in DEBUG Mode

The following changes in behavior of the Flash Controller occur when the Flash Controller is accessed using the On-Chip Debugger:

- The Flash Write Protect option bit is ignored.
- The Flash Sector Protect Register is ignored for programming and erase operations.
- Programming operations are not limited to the page selected in the Page Select Register.
- Bits in the Flash Sector Protect Register can be written to one or zero.
- The second write of the Page Select Register to unlock the Flash Controller is not necessary.
- The Page Select Register can be written when the Flash Controller is unlocked.
- The Mass Erase command is enabled through the Flash Control Register.

Caution: For security reasons, the Flash controller allows only a single page to be opened for write/ erase. When writing multiple Flash pages, the flash controller must go through the unlock sequence again to select another page.

Flash Control Register Definitions

This section defines the features of the following Flash Control registers.

Flash Control Register: see page 153

Flash Status Register: see page 155

Flash Page Select Register: see page 156

Flash Sector Protect Register: see page 157

Flash Frequency High and Low Byte Registers: see page 157

Flash Control Register

The Flash Controller must be unlocked using the Flash Control (FCTL) Register before programming or erasing the Flash memory. Writing the sequence 73H 8CH, sequentially, to the Flash Control Register unlocks the Flash Controller. When the Flash Controller is unlocked, the Flash memory can be enabled for Mass Erase or Page Erase by writing the appropriate enable command to the FCTL. Page Erase applies only to the active page selected in Flash Page Select Register. Mass Erase is enabled only through the On-Chip

Operation	Minimum Latency	Maximum Latency
Read (16 byte array)	875	9961
Read (64 byte array)	876	8952
Read (128 byte array)	883	7609
Write (16 byte array)	4973	5009
Write (64 byte array)	4971	5013
Write (128 byte array)	4984	5023
Illegal Read	43	43
Illegal Write	31	31

Table 107. NVDS Read Time

If NVDS read performance is critical to your software architecture, you can optimize your code for speed. Try the first suggestion below before attempting the second.

- 1. Periodically refresh all addresses that are used. The optimal use of NVDS in terms of speed is to rotate the writes evenly among all addresses planned to use, bringing all reads closer to the minimum read time. Because the minimum read time is much less than the write time, however, actual speed benefits are not always realized.
- 2. Use as few unique addresses as possible to optimize the impact of refreshing, plus minimize the requirement for it.

host is the character 80H. The character 80H has eight continuous bits Low (one Start bit plus 7 data bits), framed between High bits. The Auto-Baud Detector measures this period and sets the OCD Baud Rate Generator accordingly.

The Auto-Baud Detector/Generator is clocked by the system clock. The minimum baud rate is the system clock frequency divided by 512. For optimal operation with asynchronous datastreams, the maximum recommended baud rate is the system clock frequency divided by 8. The maximum possible baud rate for asynchronous datastreams is the system clock frequency divided by 4, but this theoretical maximum is possible only for low noise designs with clean signals. Table 108 lists minimum and recommended maximum baud rates for sample crystal frequencies.

System Clock Frequency (MHz)	Recommended Maximum Baud Rate (Kbps)	Recommended Standard PC Baud Rate (bps)	Minimum Baud Rate (Kbps)
20.0	2500.0	1,843,200	39
1.0	125.0	115,200	1.95
0.032768 (32kHz)	4.096	2,400	0.064

Table 108. OCD Baud-Rate Limits

If the OCD receives a Serial Break (nine or more continuous bits Low) the Auto-Baud Detector/Generator resets. Reconfigure the Auto-Baud Detector/Generator by sending 80H.

OCD Serial Errors

The On-Chip Debugger can detect any of the following error conditions on the DBG pin:

- Serial Break (a minimum of nine continuous bits Low)
- Framing Error (received Stop bit is Low)
- Transmit Collision (OCD and host simultaneous transmission detected by the OCD)

When the OCD detects one of these errors, it aborts any command currently in progress, transmits a four character long Serial Break back to the host and resets the Auto-Baud Detector/Generator. A Framing Error or Transmit Collision may be caused by the host sending a Serial Break to the OCD. Because of the open-drain nature of the interface, returning a Serial Break break back to the host only extends the length of the Serial Break if the host releases the Serial Break early.

The host transmits a Serial Break on the DBG pin when first connecting to the Z8 Encore! XP F082A Series devices or when recovering from an error. A Serial Break from the host resets the Auto-Baud Generator/Detector but does not reset the OCD Control Register. A

Mnemonic	Operands	Instruction
BCLR	bit, dst	Bit Clear
BIT	p, bit, dst	Bit Set or Clear
BSET	bit, dst	Bit Set
BSWAP	dst	Bit Swap
CCF	—	Complement Carry Flag
RCF	_	Reset Carry Flag
SCF	—	Set Carry Flag
ТСМ	dst, src	Test Complement Under Mask
ТСМХ	dst, src	Test Complement Under Mask using Extended Addressing
ТМ	dst, src	Test Under Mask
TMX	dst, src	Test Under Mask using Extended Addressing

Table 121. Bit Manipulation Instructions

Table 122. Block Transfer Instructions

Mnemonic	Operands	Instruction
LDCI	dst, src	Load Constant to/from Program Memory and Auto- Increment Addresses
LDEI	dst, src	Load External Data to/from Data Memory and Auto- Increment Addresses

Table 123. CPU Control Instructions

Mnemonic	Operands	Instruction
ATM		Atomic Execution
CCF		Complement Carry Flag
DI	_	Disable Interrupts
EI	_	Enable Interrupts
HALT	_	Halt Mode
NOP		No Operation

221

Assembly		Ade M	dress ode	Oncode(s)			Fla	ags			Fetch	Instr.
Mnemonic	Symbolic Operation	dst	src	(Hex)	С	Ζ	S	۷	D	Н	S	s
TMX dst, src	dst AND src	ER	ER	78	_	*	*	0	_	_	4	3
		ER	IM	79	-						4	3
TRAP Vector	$SP \leftarrow SP - 2$ @SP \leftarrow PC $SP \leftarrow SP - 1$ @SP \leftarrow FLAGS PC \leftarrow @Vector		Vector	F2	-	-	-	-	-	-	2	6
WDT				5F	_	_	_	_	_	_	1	2
XOR dst, src	$dst \gets dst \ XOR \ src$	r	r	B2	_	*	*	0	_	_	2	3
		r	lr	B3	-						2	4
		R	R	B4	-						3	3
		R	IR	B5	-						3	4
		R	IM	B6	-						3	3
		IR	IM	B7	-						3	4
XORX dst, src	$dst \gets dst \ XOR \ src$	ER	ER	B8	_	*	*	0	_	_	4	3
		ER	IM	B9	-						4	3

Table 128. eZ8 CPU Instruction Summary (Continued)

Note: Flags Notation:

* = Value is a function of the result of the operation.

– = Unaffected.

X = Undefined.

0 = Reset to 0.

1 =Set to 1.

227

Table 130. Absolute Maximum Ratings (Continued)

Parameter	Minimum	Maximum	Units	Notes
Maximum current into V _{DD} or out of V _{SS}		120	mA	
28-pin Packages Maximum Ratings at 0°C to 70°C				
Total power dissipation		450	mW	
Maximum current into V _{DD} or out of V _{SS}		125	mA	

Notes: Operating temperature is specified in DC Characteristics.

This voltage applies to all pins except the following: V_{DD}, AV_{DD}, pins supporting analog input (Port B[5:0], Port C[2:0]) and pins supporting the crystal oscillator (PA0 and PA1). On the 8-pin packages, this applies to all pins but V_{DD}.

2. This voltage applies to pins on the 20-/28-pin packages supporting analog input (Port B[5:0], Port C[2:0]) and pins supporting the crystal oscillator (PA0 and PA1).

DC Characteristics

Table 131 lists the DC characteristics of the Z8 Encore! XP F082A Series products. All voltages are referenced to V_{SS} , the primary system ground.

		T _A = -40°C to +105°C (unless otherwise specified)				
Symbol	Parameter	Minimum	Typical	Maximum	Units	Conditions
V _{DD}	Supply Voltage	2.7	-	3.6	V	
V _{IL1}	Low Level Input Voltage	-0.3	-	0.3*V _{DD}	V	
V _{IH1}	High Level Input Voltage	0.7*V _{DD}	-	5.5	V	For all input pins without analog or oscillator function. For all sig- nal pins on the 8-pin devices. Programmable pull-ups must also be disabled.
V _{IH2}	High Level Input Voltage	0.7*V _{DD}	-	V _{DD} +0.3	V	For those pins with analog or oscillator function (20-/28-pin devices only), or when pro- grammable pull-ups are enabled.
V _{OL1}	Low Level Output Voltage	-	-	0.4	V	$I_{OL} = 2 \text{ mA}; V_{DD} = 3.0 \text{ V}$ High Output Drive disabled.

Table 131. DC Characteristics

Notes:

1. This condition excludes all pins that have on-chip pull-ups, when driven Low.

2. These values are provided for design guidance only and are not tested in production.

UART Timing

Figure 37 and Table 146 provide timing information for UART pins for the case where CTS is used for flow control. The CTS to DE assertion delay (T1) assumes the Transmit Data Register has been loaded with data prior to CTS assertion.



Figure 3	37. U	ART	Timing	With	CTS
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		Delay (ns)		
Parameter	Abbreviation	Minimum	Maximum	
UART				
T ₁	CTS Fall to DE output delay	2 * X _{IN} period	2 * X _{IN} period + 1 bit time	
T ₂	DE assertion to TXD falling edge (start bit) delay	±	: 5	
T ₃	End of Stop Bit(s) to DE deassertion delay	±	: 5	

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Packaging

Zilog's Product Line of MCUs includes the Z8F011A, Z8F012A, Z8F021A, Z8F022A, Z8F041A, Z8F042A, Z8F081A and Z8F082A devices, which are available in the following packages:

- 8-pin Plastic Dual-Inline Package (PDIP)
- 8-Pin Quad Flat No-Lead Package (QFN)/MLF-S¹
- 8-pin Small Outline Integrated Circuit Package (SOIC)
- 20-pin Small Outline Integrated Circuit Package (SOIC)
- 20-pin Small Shrink Outline Package (SSOP)
- 20-pin Plastic Dual-Inline Package (PDIP)
- 28-pin Small Outline Integrated Circuit Package (SOIC)
- 28-pin Small Shrink Outline Package (SSOP)
- 28-pin Plastic Dual-Inline Package (PDIP)

Current diagrams for each of these packages are published in Zilog's <u>Packaging Product</u> <u>Specification (PS0072)</u>, which is available free for download from the Zilog website.

^{1.} The footprint of the QFN)/MLF-S package is identical to that of the 8-pin SOIC package, but with a lower profile.